行政院國家科學委員會補助專題研究計畫成果報告

※※※※※※※※※※※※※※※※※※※※※※※※※※

※　　　隨機摻雜在次20奈米矽場效應電晶體特性擾動之研究　　　※

※※※※※※※※※※※※※※※※※※※※※※※※※※

計畫類別：■個別型計畫　　□整合型計畫

計畫編號：NSC96－2221－E－009－210－

執行期間：　96 年　8 月　1 日至 97 年　7 月　31 日

計畫主持人：李義明

計畫參與人員：博士生：余紹銘、黃至鴻；碩士生：葉大慶、黃宣銘

執行單位：國立交通大學電信工程學系

中　華　民　國　97 年 9 月 30 日

隨機摻雜在次 20 奈米矽場效應電晶體特性擾動之研究

"**Random-Dopant-Induced Electrical Characteristics Fluctuation in Sub-20nm Field Effect Transistors**"

計畫編號：NSC96－2221－E－009－210－

執行期間：96 年 8 月 1 日 至 97 年 7 月 31 日

主持人：國立交通大學電信工程學系李義明副教授

一、中文摘要

本研究實驗證實對於二十奈米 CMOS 元件其臨界電壓受到離散摻雜的影響會有高達四十毫伏特的變異。為了分析此一問題我們產生統計不偏的隨機通道然後映射到分析的元件中，這種做法可以同時分析到隨機摻雜物數目與隨機摻雜物位置效應在 CMOS 元件特性的影響。研究上同時分析十五奈米 CMOS 元件的特性偏移問題，同時分析金屬閘極以及薄氧化層的擾動壓抑效果。

英文摘要

We have, for the first time, experimentally quantified the random dopant distribution induced threshold voltage (V_t) standard deviation up to 40 mV for 20 nm-gate planar complementary metal-oxide-semiconductor field effect transistors (CMOS). Discrete dopants have been statistically positioned in the three-dimensional (3D) channel region to examine associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation". As gate length further scales down to 15 nm, the newly developed discrete-dopant scheme features an effective solution to suppress 3-sigma-edge single digit dopant induced V_t variation by gate work function modulation. The results of this study may postpone the scaling limit projected for planar CMOS.

關鍵字

Random dopant distribution, Threshold voltage fluctuation, Dopant concentration variation, Dopant position fluctuation, 3D modeling and simulation, CMOS device.

二、計畫的緣由與目的

It is known that gate length scaling is still the most effective way to continue Moore's Law for transistor density increase and chip performance enhancement [1-3]. However, as planar complementary metal-oxide- semiconductor field effect transistor (CMOS) advances to sub-20 nm gates, double-digit channel dopants make transistor behaviors more complicated to be characterized with conventional "continuum modeling", due to every "discrete" dopant has its significant weight to impact the resulted transistor performance. Random nature of discrete dopant distribution results in significantly random fluctuations, such as the deviation of threshold voltage (V_t), drive current mismatch, and so on [3-14]. The fluctuation budget has to be controlled even tighter due to doubly increased transistor number along with technology node moving ahead. But unfortunately, the fluctuation is intrinsically increased with the scaling of transistor feature size, even not considering worsened short channel control [3].

Without loss of generality, the fluctuation can be decomposed into three components, one is resulting from the random dopant distribution (RDD) [3-8, 10-14] and the others are due to the mean gate

length deviation (GLD) and the line edge roughness (LER) [3-4, 6, 8-9]. The mean gate-length deviation and the line-edge roughness are mainly resulted from issues associated with resolution and granularity of lithography. The random dopant distribution induced fluctuation is due to the random nature of ion implantation. Various random dopant effects have been recently studied in both experimental and theoretical approaches [4-8, 10-14]. These studies have shown that the fluctuation of electrical characteristics are not purely a result of a variation in average doping density associated with a fluctuation in the number of dopants, but also the particular random distribution of dopants in the channel region. In this work, we are absorbed in the random dopant effect, and herein developed a systematic method to experimentally extract the random dopant distribution induced V_t fluctuation. We have, for the first time, experimentally quantified RDD induced threshold voltage standard deviation up to 40 mV for 20 nm-gate planar CMOS. Discrete dopants have been statistically positioned in the 3D channel region to examine associated carrier transportation characteristics, concurrently capturing “dopant concentration variation” and “dopant position fluctuation”. Therefore, a three-dimensional (3D) “atomistic” device simulation, in good agreement with the experimental data, has been carried out to realize statistical analysis and to feature solutions for reducing the RDD induced V_t variation upon gate length (L_g) scaling. As gate length of CMOS devices further scaling down to 15nm, the developed approach also suggests a solution to suppress 3-sigma-edge single digit dopants induced V_t variation by gate work function modulation. We believe that the study may postpone the scaling limit projected for nanoscale CMOS devices.

This report is organized as follows. In Sec. III, we state the experiment and simulation. We show the results and discuss comparison between the measurement and simulation. Finally, we draw conclusions.

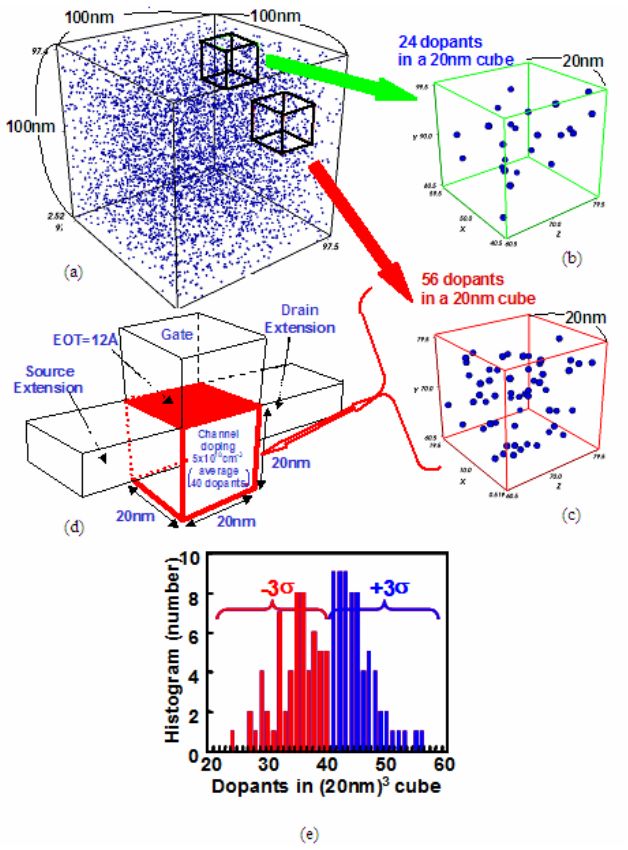


Figure 1. (a) Discrete dopants randomly distributed in $(100\ nm)^3$ cube with an average concentration of 5E18 cm^{-3}. There will be 5000 dopants within the $(100\ nm)^3$ cube, but dopants vary from 24 to 56 (the average number is 40 and the standard deviation is 6.3) within its 125 sub-cubes of $(20\ nm)^3$, (the figures 1(b), 1(c), and 1(e)). These 125 sub-cubes are then equivalently mapped into channel region for dopant-position- and dopant-number-sensitive simulation, as shown in the figure 1(d).

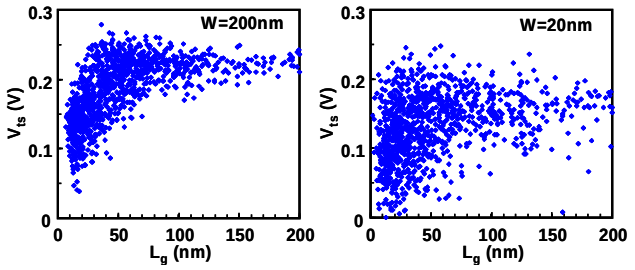
三、研究方法及成果

Threshold voltage is one of key device parameters in the characteristics of nanoscale metal-oxide-semiconductor field effect transistors (MOSFETs). As mean gate length deviation, line edge roughness [3-4, 6, 8-9] and random dopant

distribution [3-8, 10-14] are the major variation sources of threshold voltage, we thus can extract RDD induced standard V_t deviation, $\sigma V_{t,RDD}$, from the following approximated equation as $\sigma V_{t,total}$ and $\sigma V_{t,GLD\&LER}$ can be directly measured from experimental data [3]:

$$(\sigma V_{t,total})^2 \approx (\sigma V_{t,GLD\&LER})^2 + (\sigma V_{t,RDD})^2, \qquad (1)$$

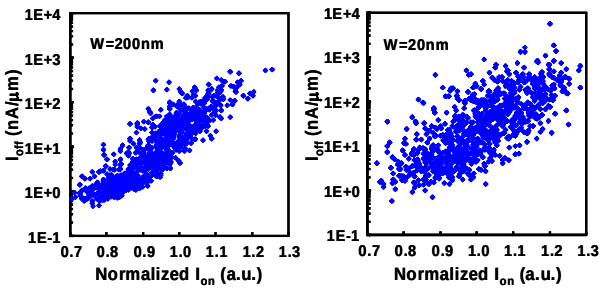
where $\sigma V_{t,total}$ is the total standard V_t deviation and $\sigma V_{t,GLD\&LER}$ is V_t fluctuation contributed from mean gate length deviation and line edge roughness. Using the V_t roll-off relation [15], $\sigma V_{t,GLD\&LER} = \frac{dV_t}{dL_g} \times \sigma L_g$, $\sigma V_{t,GLD\&LER}$ can be extracted with the experimental data of V_t roll-off and standard gate length deviation, σL_g. Thus from the experimentally measured $\sigma V_{t,total}$ and extracted $\sigma V_{t,GLD\&LER}$, we can calculate $\sigma V_{t,RDD}$ according to Eq. (1). We notice that for data with large σVt, the Ion-Ioff distribution is scattering. However, it still can be analyzed and well fitted by Eq. (1). σLg is obtained from SEM critical dimension measurements.



(a) (b)

Figure 2. Experimental saturation threshold voltage, V_t, of N-MOSFETs with L_g down to 20 nm for the (a) width = 200 nm and (b) width = 20 nm at V_d = 1.0 V.

In this work, excellent short-channel-effect control down to 20 nm-gate has been experimentally realized with advanced shallow junction technology. We achieve junction depth around one half of gate length to maintain subthreshold leakage at 100 nA/μm with channel doping ≈5E18 cm^{-3} and gate dielectric of 12A° EOT (equivalent oxide thickness). Furthermore, to have the insights of random-dopants-distribution effects, quantum mechanical transport simulation is performed and compared with experimental data by solving a set of calibrated 3D density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations [11, 15-17]. The 3D device simulation was calibrated against the non-equilibrium green's function simulation for planar MOSFETs [17-19]. All statistically generated discrete dopants, as shown in Fig. 1 (details in next paragraph), are advanced and incorporated into the 3D device simulation under our parallel computing system [16]. Such large-scale simulation approach allows us to explore the electrical characteristic fluctuations induced by randomness of dopant number and position in the channel region concurrently. The mobility model used in the device simulation, according to Mathiessen's rule [20, 21], can be expressed as:



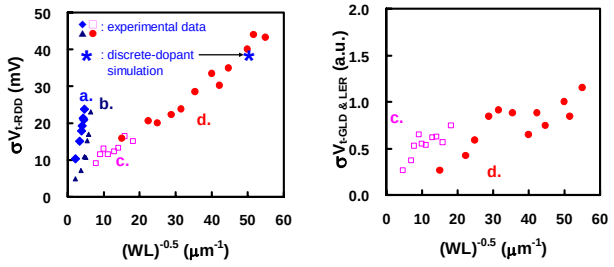
(a) (b)

Figure 3. Experimental I_{on}-I_{off} characteristics of N-MOSFETs with L_g down to 20 nm for the (a) width = 200 nm and (b) width = 20 nm at V_d = 1.0V. The I_{on} was normalized against the on-current of nominal Lg case, i.e. the 20 nm Lg case.

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk}}, \qquad (2)$$

where D = exp(x / l_{crit}), x is the distance from the interface and l_{crit} is a fitting parameter. The mobility consists of three parts: (1) the surface contribution due to acoustic phonon scattering $\mu_{surf\_aps} = \frac{B}{\mathbf{E}} + \frac{C(N_i/N_0)^\tau}{\mathbf{E}^{1/3}(T/T_0)^K}$, where $N_i = N_A + N_D$, N_A is the acceptor impurity density and N_D is the donor impurity density, T_0 = 300 K, **E** is the transverse electric field normal to the interface of

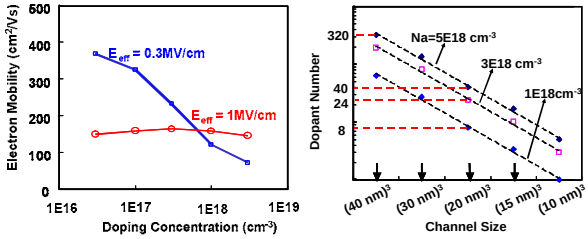
semiconductor and insulator, B and C are parameters which based on physically derived quantities, N_0 and τ are fitting parameters, T is lattice temperature, and K is the temperature dependence of the probability of surface phonon scattering; (2) the contribution attributed to surface roughness scattering is $\mu_{surf\_rs} = \left(\frac{(\mathbf{E}/\mathbf{E}_{ref})^{\Xi}}{\delta} + \frac{\mathbf{E}^3}{\eta} \right)^{-1}$, where $\Xi = A + \frac{\alpha \cdot (n+p) N_{ref}^{\nu}}{(N_i + N_1)^{\nu}}$, $\mathbf{E}_{ref}$ = 1 V/cm is a reference electric field to ensure a unitless numerator in μ_{surf_rs}, N_{ref} = 1 cm^{-3} is a reference doping concentration to cancel the unit of the term raised to the power ν in the denominator of Ξ, δ is a constant that depends on the details of the technology, such as oxide growth conditions, N_1 = 1 cm^{-3}, A, α and η are fitting parameters; (3) and the bulk mobility is $\mu_{bulk} = \mu_L (\frac{T}{T_0})^{-\xi}$, where μ_L is the mobility due to bulk phonon scattering and ξ is a fitting parameter. The mobility model is quantified with our device measurements for the best accuracy.



(a) (b)

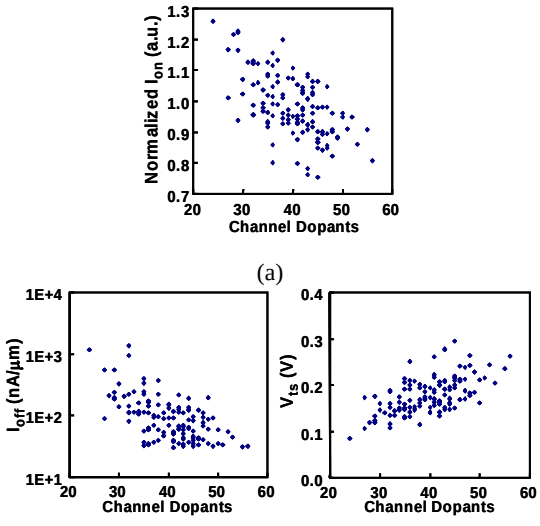
Figure 4. (a) Experimentally extracted $\sigma V_{t,RDD}$, and discrete-dopant simulation (*, L_g = W = 20 nm, EOT = 12 A^o) for various devices with nominal L_g from 55 nm down to 20 nm. The width is fixed and the length is varying to give the range of values of (WL)$^{-0.5}$. The sample size for each data point of σV_t is around 100 points. (b) The extracted $\sigma V_{t,GLD\&LER}$ for c and d conditions. The value was normalized against the $\sigma V_{t,GLD\&LER}$ of nominal Lg case in d condition.

First the doping profile is analytical approximated to the device measured, and we then apply the method to be described below, shown in Fig. 1, to generate discrete dopants in the channel region. Figure 1 briefly illustrates how to generate discrete-dopant channel for aforementioned simulation, concurrently capturing randomness of dopant number and dopant position. Figure 1(a) shows the discrete dopants randomly distributed in the cube of volume (100 nm)^3 with an average concentration of 5E18 cm^{-3} which is the same as the fabricated device. There will be 5000 dopants within the (100 nm)^3 cube, but dopants vary from 24 to 56 (the average number is 40 and the standard deviation is 6.3) within its 125 sub-cubes of (20 nm)^3, as shown in Figs. 1(b), 1(c), and 1(e), respectively. These 125 sub-cubes are then equivalently mapped into channel region for the discrete dopant simulation, as shown in Fig. 1(d). In principle, 3D device simulation with the 125 channel structures almost covers $\pm 3\sigma$ cases, shown in Fig. 1(e), and thus will be fairly meaningful to reflect statistical randomness of dopant number and dopand position in channel region.



(a) (b)

Figure 5. (a) Extracted non-strain mobility versus doping concentration at 0.3 and 1 MV/cm vertical field, and (b) scaling of average channel dopant numbers versus channel size.



(a)

(b) (c)

Figure 6. Distributions of (a) I_{on}, (b) I_{off}, and (c) V_t versus channel dopants for the 125 discrete-dopant 20nm-gate transistors (L_g = W = 20 nm) shown in Fig. 5(e).

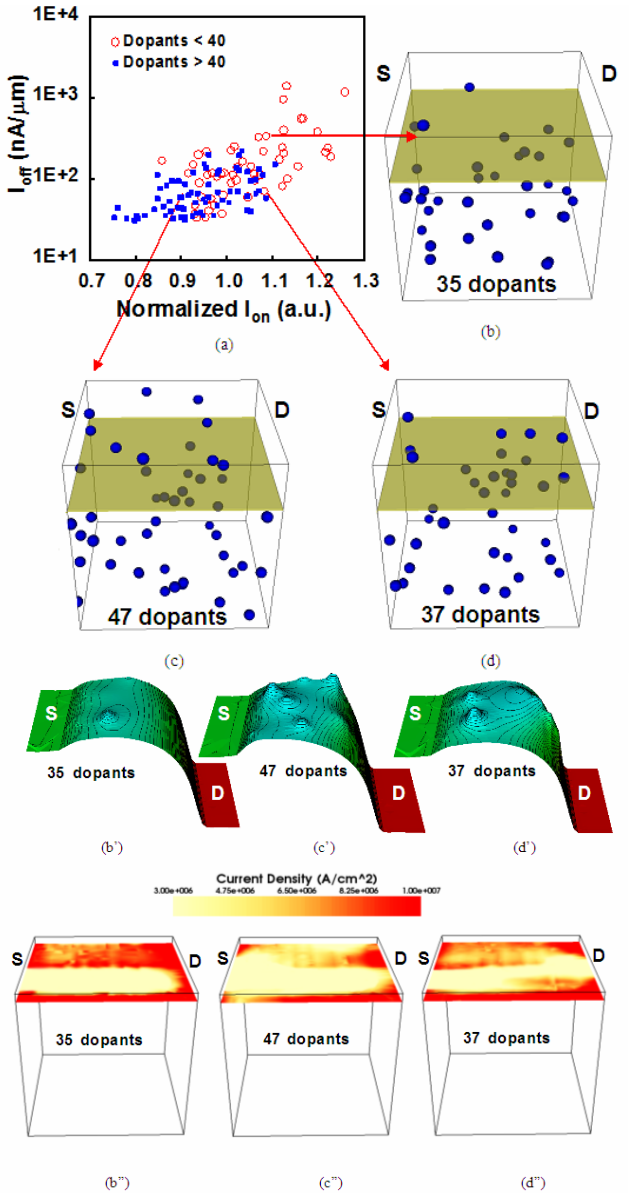


Figure 7. (a) I_{on}-I_{off} characteristics of the 125 discrete-dopant 20nm-gate transistors (L_g = W = 20 nm). (b) and (d) represent two cases of channel doping with similar I_{on} but different I_{off}; (c) and (d) represent two cases of channel doping with similar I_{off} but different I_{on}. The corresponding off-state (V_d = 1.0 V, V_g = 0.0 V) potential contours and on-state (V_d = 1.0 V, V_g = 1.0 V) current density of (b), (c), and (d) are shown in the figures 7(b'), 7(c'), 7(d') and 7(b"), 7(c"), 7(d"), respectively. All cross-sectional figures of off-state potential contours and on-state current density distributions are extracted at 1nm below 12A° EOT gate oxide.

Figures 2 and 3 show the experimental V_t fluctuation and the on- and off-state currents' (I_{on}-I_{off}) characteristics of the n-typed MOSFETs (N-MOSFETs) down to 20nm gates. The Lg values in Fig. 2 are estimated from the gate capacitances in analysis data, and we presume the widths of all samples are 200 and 20 nm for 2(a) and 2(b), respectively. As expected, the V_t roll-off characteristics of 20 nm-wide devices are much more scattered than that of 200 nm-wide devices. The RDD induced V_t's standard deviation, $\sigma V_{t,RDD}$, has then been experimentally extracted, as shown in Fig. 4(a). Discrete-dopant simulation for L_g = width (W) = 20 nm (data represented with symbol *, as shown in Fig. 4(a)) is in good agreement with the experimental data, which confirms the channel doping is randomly distributed as statistically modeled. As shown in figure 1, more than 100 cases are required for a set of Lg and width; we notice that each 3D simulation case may take about 3-7 days for final convergent result. Without loss of generality, due to the heavy computing resource, we select the most critical case (i.e., length = width = 20 nm) for comparison between simulation and measurement. Figure 4(b) shows the extracted $\sigma V_{t,GLD\&LER}$ of c and d conditions. The $\sigma V_{t,GLD\&LER}$ contains the contribution from the mean gate length deviation and the line edge roughness. In our experimental data, the $\sigma V_{t,GLD\&LER}$ increases as the $(WL)^{-0.5}$ increased, and it has similar trend, compared with $\sigma V_{t,RDD}$. Table I summaries the corresponding parameters for all cases in Fig. 4. Figure 5(a) shows the extracted mobility versus the doping concentration from samples of the cases (a) and (b), as shown in Fig. 4(a). The used mobility model can generate mobility that is in good agreement with the extracted mobility, as shown in Fig. 5(a). The low-field electron mobility at 0.3 MV/cm is greatly reduced with increasing doping concentration. That is why we limit our channel doping concentration at 5E18 cm^{-3}, which corresponding to average 40 dopants in $(20\ nm)^3$ cubes and 17 dopants in $(15\ nm)^3$ cubes, as shown in Figs. 1 and 8, respectively. Less channel doping concentration may reduce $\sigma V_{t,RDD}$, but channel dopants will quickly approach to single-digit number, as shown in Fig. 5(b). Figures 6(a), 6(b), and 6(c) show I_{on}, I_{off}, and V_t distributions versus channel dopants of these 125 cases. From the random-dopant-number point of view, the equivalent channel doping concentration increases when the dopant number increases, this substantially alters the threshold voltage and the on- and off-state currents, as shown in Figs. 6(a), 6(b), and 6(c), respectively. The random-dopant-position induced different fluctuation of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. Figure 7(a) shows the I_{on}-I_{off} characteristics of the 125 cases from Fig. 1. Figures 7(b), 7(c), and 7(d) disclose 3 different

discrete-dopant channels which have similar values of I_{on} or I_{off} but with various dopant distributions. Their corresponding cross-sectional off-state electrostatic potential and on-state current density at 1nm below the gate oxide are also presented, shown in Figs. 7(b'), 7(c'), and 7(d'), and 7(b"), 7(c''), and 7(d"), which clearly shows that distributions of the electrostatic potential and current density are closely related to the dopant arrangements within the cross-sectional area beside source side, as shown Figs. 7(b), 7(c), and 7(d).

Table I The corresponding parameters for all cases in the figure 4. It presents the trend of σVt for technology scaling. The nominal Lg cases in table are nominal gate lengths for each technology node respectively.

	EOT (A°)	Channel Doping (cm^{-3})	Nominal L_g (nm)	Width (nm)
a	24	≈1E18	55	1000
b	18	≈3E18	35	1000
c	12	≈5E18	20	200
d	12	≈5E18	20	20

Table II. Summary of discrete dopant fluctuated 20nm- and 15nm-gate planar CMOS transistors.

L_g	Width	Data Source	Gate Work Function	Channel Doping (cm^{-3})	EOT	$\sigma V_{t,RDD}$
20 nm	200 nm	experimental	band-edge	5E+18	12 A°	17 mV
	20 nm	experimental		5E+18	12 A°	40 mV
	20 nm	Simulation		5E+18	12 A°	39 mV
15 nm	15 nm	Simulation	ϕ_N = 4.22 eV	5E+18	12 A°	54 mV
	15 nm	Simulation	ϕ_P = 4.98 eV	5E+18	8 A°	41 mV

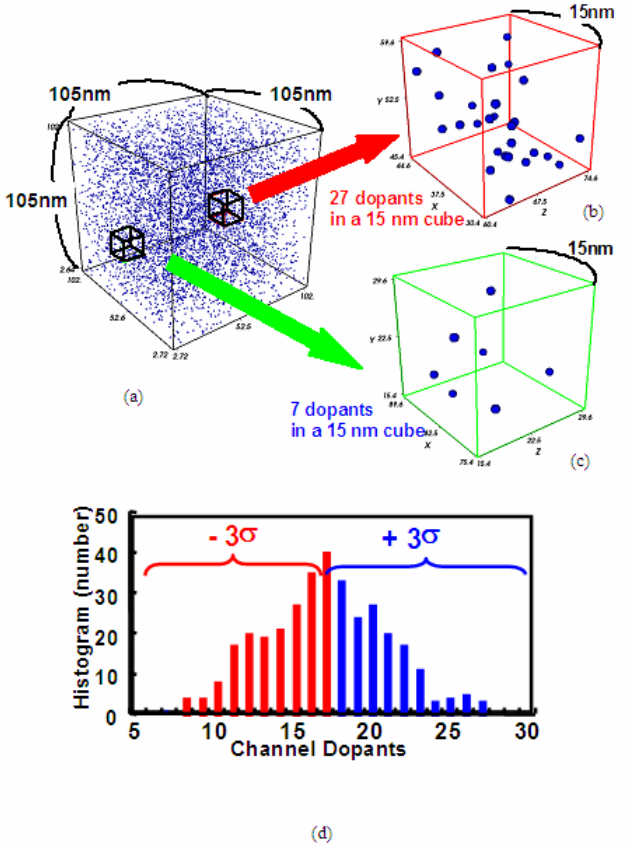
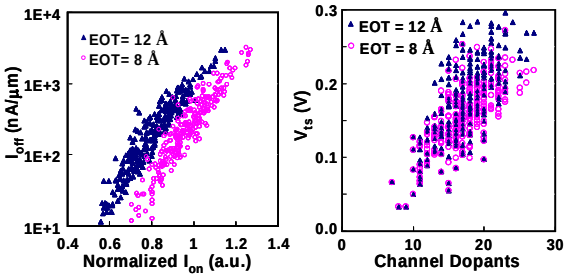


Figure 8. The 5E18 cm^{-3} doped $(105\ nm)^3$ cube, (a), with 343 sub-cubes of $(15\ nm)^3$. Dopants inside the sub-cubes range from 7, (c), to 27, (b), with the average number of 17 and one standard deviation of 4, (d).



(a) (b)

Figure 9. The (a) I_{on}-I_{off} characteristics and (b) V_t versus channel dopants of discrete doped 15 nm-gates with EOT = 12 A° (solid triangle) and 8 A° (open circle). Gate work function is 4.22 eV in the simulation.

Based on experimental data and discrete modeling of 20 nm gate with 12 A° EOT, 8 A° EOT seems an effective way for 15nm-gate CMOS to mitigate the increase of the RDD induced V_t variation. With the same approach, shown in Fig. 1, for generating discrete-dopant channels, Fig. 8(a) shows 343 sub-cubes of $(15\ nm)^3$ derived from $(105\ nm)^3$ cube with 5E18cm^{-3} doping. Figure 9 shows the I_{on}-I_{off} characteristics and V_t distribution of these cases with 12A° and 8A° EOT. The case of 8A° EOT shows tighter V_t scattering. Furthermore, as channel dopants could be only 7 at 3σ edge, shown in Fig. 8(c), we herein propose using higher work-function gate to increase its intrinsic electrostatic potential barrier height, shown in Fig. 10(c), to prevent source-to-drain punchthrough at off-state, as shown in Fig. 10(b). Thus $\sigma V_{t,RDD}$ can be maintained while L_g scaling down to 15 nm from 20 nm, as summarized in Table II. It has been known that the σV_t is proportional to the oxide thickness [5, 15]; that is $\sigma V_t = \frac{qtox}{\varepsilon_{ox}}\sqrt{\frac{N_A W_d}{4LW}}$, where ε_{ox} is the permittivity of the gate oxide and W_d is the width of the depletion layer under the gate. In the examination for 15nm-gate CMOS, when the EOT changed from 12 A° to 8 A° (1.5 times smaller), the $\sigma V_{t,RDD}$ was reduced from 54 mV to 41 mV (1.32 times smaller), which conformed to the expression of σV_t. Although the advanced devices, such as double-gate or surrounding-gate structures [3, 10], or epitaxial channels [13, 14] can reduce the fluctuation, these approaches are much more complicated and still require EOT's improvement to some degree for well suppression of σV_t.

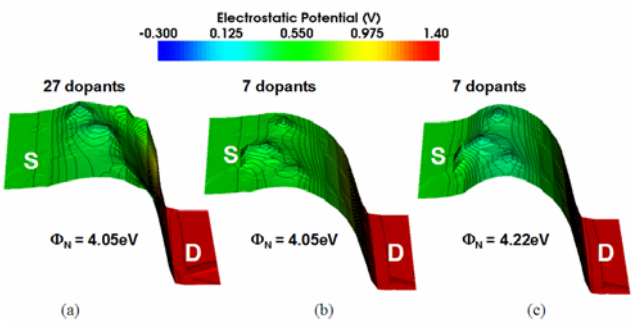


Figure 10. Cross-sectional off-state electrostatic potential contours of two extreme cases in 15 nm channels (W = 15 nm and EOT = 8 A^o) with (a) 27 dopants and Φ_N = 4.05 eV, (b) 7 dopants and Φ_N = 4.05 eV, and (c) 7 dopants and Φ_N = 4.22 eV; all at 1 nm below the gate oxide.

四、結論與討論

Random dopant distribution induced σV_t for 20 nm-gate planar CMOS devices has been experimentally extracted and in good agreement with newly developed 3D discrete-dopant characterization. Average 40 dopants randomly distributed in the channel region give rise to $\sigma V_{t,RDD}$ of 40 mV. The developed scheme outlooks that 7 dopants under 15 nm gate at 3σ edge will occur and 8A^o EOT in addition to work-function-modulated metal gate can suppress the increase of the $\sigma V_{t,RDD}$ for realizing manufacture with such gate length scaling.

This work was supported in part by National Science Council of Taiwan under Contract NSC-96-2221-E-009-210, Contract NSC-95-2221-E-009-336, Contract NSC-95-2752-E-009-003-PAE, by the MoE ATU Program under a 2006-2007 grant, and by the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan under a 2006-2008 grant. The principal investigator gratefully acknowledges the managerial and instrumental supervision to deploy the development work at Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

五、參考文獻

1. F.-L. Yang, D.-H. Lee, H.-Y Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," in *VLSI Tech. Digest*, 2004, pp. 196-197.
2. F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, and C. Hu, "25 nm CMOS Omega FETs," in *IEDM Tech. Digest*, 2002, pp. 255-258.
3. F.-L. Yang, J-R. Hwang and Y. Li, "Electrical Characteristic Fluctuations in Sub-45nm CMOS Devices," in *Proc. of IEEE CICC*, 2006, pp. 691-694.
4. H. Fukutome, Y. Momiyama, T. Kubo, E. Yoshida, H. Morioka, M. Tajima, and T. Aoyama, "Suppression of Poly-Gate-Induced Fluctuations in Carrier Profiles of Sub-50nm MOSFETs," in *IEDM Tech. Digest*, 2006, pp. 281-284.
5. A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505-2513, 1998.
6. A. Asenov, A.R. Brown, J.H. Davies, S. Kaya and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1837-1852, 2003.
7. D. J. Frank, Y. Taur, M. Ieong and H.-S.P. Wong, "Monte Carlo modeling of threshold variation due to dopant fluctuations," in *VLSI Tech. Digest*, 1999, pp. 169-170.
8. G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation Study of Individual and Combined Sources of Intrinsic Parameter Fluctuations in Conventional Nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, pp. 3063-3070, 2006.
9. S. Xiong and J. Bokor, "A simulation study of gate line edge roughness effects on doping profiles of short-channel MOSFET devices," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 228-232, 2004.
10. Y. Li and S.-M. Yu, "Comparison of Random-Dopant-Induced Threshold Voltage Fluctuation in Nanoscale Single-, Double-, and Surrounding-Gate Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 45, pp. 6860-6865, 2006.
11. Y. Li and S.-M. Yu, "Study of Threshold Voltage Fluctuations of Nanoscale Double Gate Metal-Oxide-Semiconductor Field Effect Transistors Using Quantum Correction Simulation," *J. Comput. Electronics*, vol. 5, no. 2-3, pp. 125-129, 2006.
12. Y. Li, S.-M. Yu, and H.-M. Chen, "Process-variation- and random-dopants-induced threshold voltage

fluctuations in nanoscale CMOS and SOI devices," *Microelectronic Engineering*, in press.

13. Y. Li and S.-M. Yu, "Quantum correction simulation of random dopant-induced threshold voltage fluctuations in nanoscale metal-oxide-semiconductor structures," in *Proc. 5th IEEE NANO*, 2005, 527-530.
14. A. Asenov and S. Saini, "Suppression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1-μm MOSFET's with Epitaxial and δ-Doped Channels," *IEEE Trans. Elec. Dev.*, Vol. 46, no. 8, pp. 1718-1724, 1999.
15. T. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.
16. Y. Li, S. M. Sze, and T.-S. Chao, "A Practical Implementation of Parallel Dynamic Load Balancing for Adaptive Computing in VLSI Device Simulation," *Engineering with Computers*, vol. 18, no. 2, pp. 124-137, 2002.
17. Y. Li, H.-M. Chou, and J.-W. Lee, "Investigation of electrical characteristics on surrounding-gate and omega-shaped-gate nanowire FinFETs," *IEEE Trans. Nanotech.*, vol. 4, no. 5, pp. 510-516, 2005.
18. A. Martinez, J. R. Barker, M. P. Anantram, A. Svizhenko and A. Asenov, "Developing a full 3D NEGF simulator with random dopant and interface roughness," in *Proc. 11th International Workshop on Computational Electronics*, 2006, 275.
19. J. R. Watling, A. R. Brown, A. Asenov, A. Svizhenko and M. P. Anantram, "Simulation of Direct Source-to-Drain Tunnelling Using the Density Gradient Formalism: Non-equilibrium Green's Function Calibration", in *Proc. SISPAD 2002*, 2002, 267-270.
20. S. Selberherr, *Analysis and Simulation of Semiconductor Devices*, New York, Springer-Verlag, 1984.
21. M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, "An Improved Electron and Hole Mobility Model for General Purpose Device Simulation," *IEEE Trans. Elec. Dev.*, vol. 44, pp. 1529-1538, 1997.