Materials Chemistry and Physics 127 (2011) 85–90

Contents lists available at ScienceDirect

Materials Chemistry and Physics

journal homepage: www.elsevier.com/locate/matchemphys

Effect of Si-die dimensions on electromigration failure time of flip-chip solder joints

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ARTICLE INFO

Article history:
Received 17 April 2010
Received in revised form 7 December 2010
Accepted 10 January 2011

Keywords:
Thermal conductivity
Diffusion
Electrical properties
Thermal properties

ABSTRACT

Electromigration tests were performed for solder joints with various Si dies thickness and area. For the electro-migration in flip-chip solder joints with a 60, 100, 250 and 760 μm thick Si die, it is found that Si-die thickness has profound influence on electro-migration lifetime. The average failure time was 1608.0 h for joints with a 760-μm-thick die when they are stressed by 1.0 A at 100 °C. However, it decreased significantly to 0.6 h for joints with a 60-μm-thick die. According to the temperature measured by infrared microscopy, solder joints with a thinner die has a higher Joule heating effect, which results in a shorter electromigration lifetime. In addition, the die area has a considerable influence on the electromigration failure time. The electromigration failure time decreases as the die area decreases. The average failure time is 1608.0, 28.0, 10.6, 5.0 and 0.3 h for the solder joints with die area of $5350 \times 4350\ \mu m^2$, $5350 \times 3600\ \mu m^2$, $5350 \times 3000\ \mu m^2$, $5350 \times 2000\ \mu m^2$ and $5350 \times 1000\ \mu m^2$, respectively. The Joule heating effect becomes more serious in smaller dies, which causes a shorter electromigration lifetime.

1. Introduction

To keep pace with the trend of miniaturization and high performance in microelectronic devices, thousands of solder bumps are fabricated onto one chip. Subsequently, the size of solder bumps has progressively diminished and they now have a diameter of approximately 100 μm or less. The design rule of packaging requires that each bump carries 0.2 to 0.4 A, which resulted a current density of approximately 2×10^3 to 2×10^4 A cm^{-2}. The damage of electromigration occurs prevalently in solder joints is due to these current densities and such phenomenon has become an important reliability issue for flip-chip solder joints [1–4]. Several critical factors that may influence electro-migration lifetime have been investigated. They are the dimension of wiring traces on the chip [5], thickness of under-bump-metallization (UBM) [6–8] and UBM materials [9].

In addition, three-dimensional (3D) packaging and stacked die have become promising methods for increasing packaging density of high-performance devices [10,11]. Towards these means, silicon dies, which are typically over 700 μm thick, must be thinned down to approximately 200–300 μm before stacking and reducing more than half of the original thickness. Owing to the drastic change in thickness, the effect of die thickness on electromigration has become an important issue. In addition, the chip size for electromigration may vary from group to group. However, no study has been carried out to address this concern so far.

In this study, failure times are measured by electromigration tests performed in solder joints of different Si-die thicknesses and dimensions. It is found that Si-die thickness and dimensions affect the electro-migration failure time strongly in solder joints. To understand the trends and to investigate the reasons for changes in failure time, thermal infrared (IR) microscopy was employed to measure the temperature distribution in the Al trace above the solder joints that underwent current stressing.

2. Experimental

Electromigration tests are conducted in flip-chip solder joints with various dimensions of test carriers. For the study of effect of Si-die thickness on electromigration, flip-chip SnPb solder joints with Si-die of 60, 100, 250 and 760 μm thick are employed to investigate the effect of die thickness on electro-migration lifetime. The dimensions of the as-fabricated Si die are 5350 μm long, 4350 μm wide and 760 μm thick, while those of the FR4 substrate are 26.5 mm long, 26.5 mm wide, and 1 mm thick. The as-fabricated samples were ground and polished from the Si side down to the desired thicknesses. For the investigation of effect of Si-die area on electro-migration, the test carrier was ground laterally to a desired area. Fig. 1(a) shows the plan-view schematic drawing for the as-fabricated test carrier. The Si die are 5350 μm long and 4350 μm wide. The four bumps to be stressed locate at the bottom of the chip, as labeled in the figure. The test carrier was ground parallel to the length direction, as shown by the dotted lines. Fig. 1(b) shows the cross-sectional view of the test carrier. Five samples were prepared for the area effect, which includes as-fabricated ($5350 \times 4350\ \mu m^2$), $5350 \times 3600\ \mu m^2$, $5350 \times 3000\ \mu m^2$, $5350 \times 2000\ \mu m^2$ and $5350 \times 1000\ \mu m^2$. The bumps to be stressed remained intact after the grinding process.

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doi:10.1016/j.matchemphys.2011.01.023

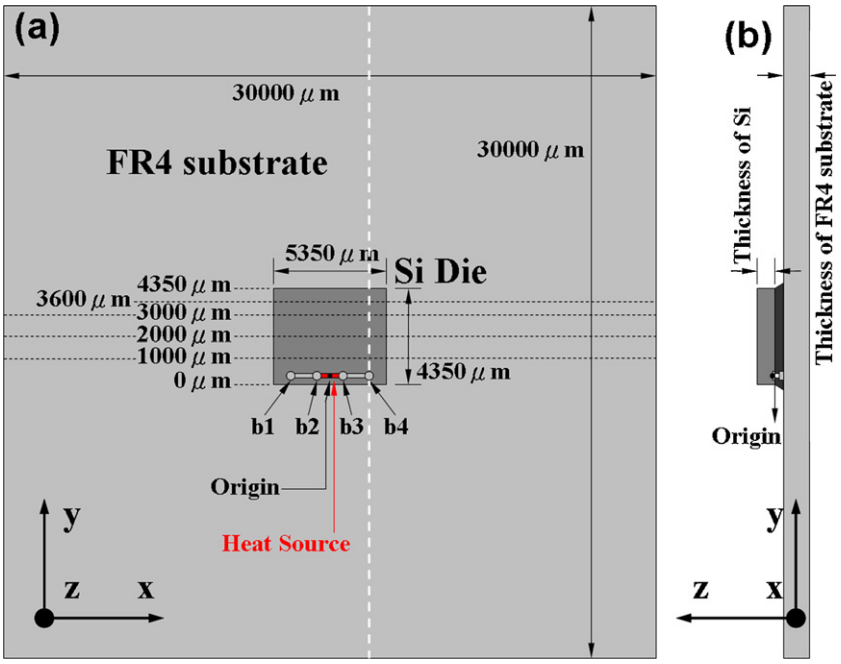

Fig. 1. (a) Plan-view schematic for test samples with different area. The chip was ground from the upper edge in the figure and stopped at a desired location. The solder bumps for electromigration test locate at the bottom of sample. (b) Cross-sectional view of the test samples.

A schematic representation of the flip-chip joints was adopted in this study which is shown in Fig. 2(a). The UBM which is used is 5-μm Cu/3-μm Ni. The diameter of the passivation and UBM openings are 85 μm and 120 μm, respectively. Electroplated eutectic SnPb was used as the solder. The diameter of the dimension of the pad opening on the substrate was 300 μm. Fig. 2(b) presents a cross-sectional schematic for the wiring layout of the joints, in which four bumps are connected by three segments of Al trace. The pitch for the bumps was 850 μm and the Al-trace was 100 μm wide and 1.5 μm thick. The four bumps in Fig. 2(b) are labeled B1 to B4. The current for electro-migration test was applied through bumps B1 and B4 as indicated in the figure. The test conditions were direct current of 1.0 A at 100 °C. In this study, the electromigration failure is defined as the stressing circuit becomes open.

Infrared microscopy (Infra-Scope II, Quantum Focus Instrument) was employed to examine the Joule heating effect of solder joints during electric current stressing. It plays as a function of changing Si-die thickness and area. The system which is used in this study has resolution of 0.1 °C in temperature sensitivity and 2.8 μm in spatial resolution. Prior to current stressing, the emissivity of the specimen was calibrated at 70 °C after the bumps were powered at a desired current. The temperature measurement was then performed to record the temperature distribution after the temperature had reached a steady state. Since the Si-die is transparent under infrared, the temperature distribution which is measured by the microscope is entirely within the Al trace and the contact opening. The temperatures on bump B1 for all test samples were measured. Electromigration failure occurs in bump 4. Yet, the temperature in bump 1 is very close to that of bump 4 during current stressing. The temperature difference is within 1 °C at 1.0 A. In addition, the measured temperature may be quite close to that of the bump temperature, since the Al pad locates directly solder bumps. Scanning electron microscopy (SEM) was used to observe the microstructure in the solder bumps after electromigration tests.

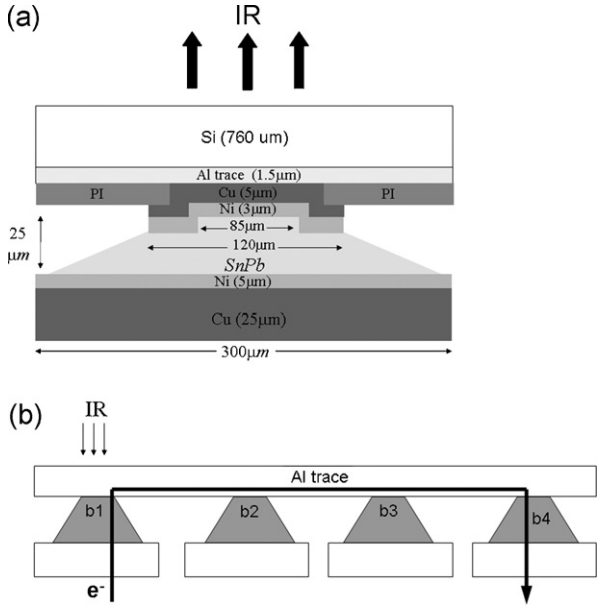

Fig. 2. Cross-sectional schematic diagram showing (a) the bump structure (b) the test layout used in this study. The current was applied through B1 and B4.

3. Results and discussion

Electromigration tests were performed for solder joints described above to examine and quantify the effect of Joule heating on the failure time due to the electromigration effect. It is found that Si-die thickness has profound influence on the electromigration lifetime of solder joints. The average failure time for the as-fabricated solder joints was 1608.0 h when they are stressed by 1.0 A at 100 °C, in which the Si die is 760 μm thick. However, it decreases significantly to 38.0 h when the Si die is thinned down to 250 μm. It is further reduced to 3.1 h and 0.6 h for solder joints with Si-die thickness of 100 μm and 60 μm, respectively. The values of failure times as a function of different silicon die dimensions are summarized in Table 1. Failure time can be decreased by three orders of magnitude when the die thickness reduced from 760 μm to 60 μm.

Fig. 3(a) through 3(d) shows the cross-sectional SEM images for the typical failure mode of after electromigration tests at 1 A. The solder joints were with a 760-μm-thick Si die. For bump 1 with upward electron flow, there was some tiny voids form in the

Table 1
Failure time of the flip-chip joints with various die thicknesses under current stressing of 1 A at 100 °C.

Die thickness (μm)	760	250	100	60
Failure time (h)	1608.0	38.0	3.1	0.6
ΔT (°C)	41.7	51.2	75.3	128.3

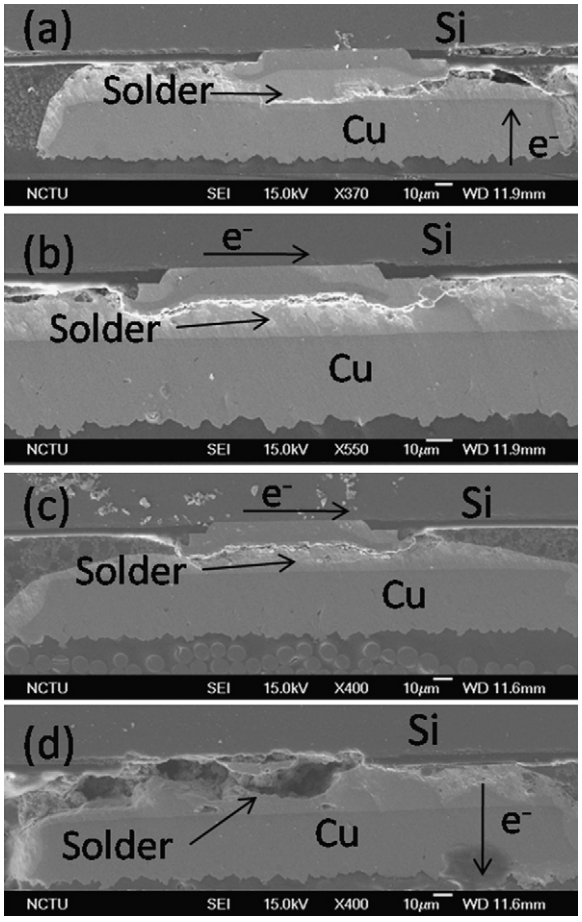

Fig. 3. Cross-sectional SEM images showing the microstructure of the failed solder joints with a 760-μm-thick Si die. (a) Bump 1 with upward electron flow. (b) Bump 2 with electron flow passing through the Al trace above the bump. (c) Bump 3 with electron flow passing through the Al trace above the bump. (d) Bump 4 with downward electron flow. Open failure occurred in the bump 4.

cathode end, as illustrated in Fig. 3(a). For both bump 2 and bump 3, the electrons passed through the Al trace above the bumps. However, some of the electrons may drift down to the bumps at the upper-left corner of the solder bump, flow in the solder bumps, and leave the solder bump from the upper-right corner of the bumps. Therefore, voids formed at the chip side, as depicted in Fig. 3(b) and 3(c) bump 3. Open failure occurred in the bump 4, as shown in Fig. 3(d), since the current crowding effect occurred seriously at the chip end [3]. The UBM layers were consumed completely and large voids formed in the chip end. Sometimes the solder may melt during the electromigration tests.

Two major factors, current density and temperature, may affect the mean-time-to-failure (MTTF) of solder joints as described by Black's equation [12]:

$$\mathrm{MTTF} = A\frac{1}{j^n}\exp\left(\frac{Q}{KT}\right) \tag{1}$$

where A is the constant, j is the current density, n is a model parameter for current density, Q is the activation energy, K is the Boltzmann's constant, and T is the real bump temperature. In this study, the current density was almost the same in solder joints with different die thicknesses, since the wiring traces on the chip, the Cu lines on the substrate and the bump size are almost the same. In addition, the ambient temperature was kept at 100 °C for all samples. Therefore, the difference in failure time should be attributed to the difference in Joule heating effect. According to Black's equation, the MTTF decreases exponentially with the stressing temperature. Likewise, the effect of Joule heating as a result of a different silicon die thicknesses would also decrease the MTTF in a similar manner.

The Joule heating effect plays a crucial role in accounting for the difference in failure time for joints with different die thicknesses. Fig. 4(a) through 4(d) shows the temperature map at 1 A on the Al pad for solder joints with die thickness of 60, 100, 250 and 760 μm, respectively. The average temperature in the Al pad was obtained by averaging the temperatures within a $40 \times 40\ \mu m^2$ area at the center of the pad, as illustrated by the dotted lines in Fig. 4(a). The passivation opening of solder joints is 85 μm in diameter and the diameter of the Al pad is 140 μm. Thus the outer periphery of the Al pad did not contact the solder joints directly. Thus we chose an area of $40 \times 40\ \mu m^2$, which is inside the passivation. The average temperature would be close to the bump temperature. The real temperatures in the pads were 228.3, 175.3, 151.2 and 141.7 °C for joints using Si-die thickness of 60, 100, 250, and 760 μm, respectively. Since the Al pad was located directly above the solder joint, the Al pad temperature was very close to the solder bump temperature. It is noteworthy that the eutectic SnPb solder may melt at the above stressing condition. For the solder joints with a 60 μm die, the temperature is 228.3 °C when the solder bump were stressed by 1.0 A. Thus, the failure mechanism may be different from the other joints. Furthermore, the average temperature increased due to the current stressing from 0.1 to 1.0 A, which was detected for all four samples, as shown in Fig. 5. At lower stressing currents (<0.2 A), there was no obvious difference in temperatures for the four samples. Yet, the difference became significant at higher stressing currents above 0.8 A. The real temperature in the bumps would therefore be significantly higher during testing than that at ambient due to Joule heating. Because all the four samples were placed on the hot plate maintained at 100 °C and the stressing circuits are identical, the difference in temperature is a clear indication that, by way of Joule heating, the Si-die thickness has significant effect on the pad temperature and subsequently the lifetime of a joint

To explain the observed interesting results, one-dimensional lumped model for thermal resistance was proposed. Fig. 6 shows the one-dimensional lumped model for the samples used in this study. The heat flow for this package system is as follows:

$$Q = k\frac{(\Delta T)}{L}A \tag{2}$$

where k is the thermal conductivity, ΔT is the temperature difference, L is the length and A is the area for heat dissipation. According to this equation, the heat dissipation becomes better as the die is thinned down. Since the thermal resistance is equal to L/KA and is smaller for a thin die if surface convection is not considered. On the other hand, the lateral thermal resistance of the die becomes larger as the die is thinned down.

The thermal resistance can be estimated using one-dimensional model. The definition of the x, y, and z axes is indicated in Fig. 1.The original was set at the center of the heat source shown in Fig. 1. The thermal resistance in the $+z$ direction, $R_{\mathrm{th},+z}$, can be expressed as follows: the heat was generated in the Al trace and it was dissipated through Si die ($R^{\mathrm{Si}}_{\mathrm{th},+z}$) and then through air convection ($R^{\mathrm{Air}}_{\mathrm{th},+z}$). Thus,

$$R_{\mathrm{th},+z} = R^{\mathrm{Si}}_{\mathrm{th},+z} + R^{\mathrm{Air}}_{\mathrm{th},+z} = \frac{t^{\mathrm{Si}}}{k^{\mathrm{Si}}A_z} + \frac{1}{h^{\mathrm{Air}}A_z} = 0.2 + 1718.8 = 1719.0 \tag{3}$$

Tables 2 and 3 list the parameters and dimensions needed for the estimation of the thermal resistance [13]. Similarly, the resistance in the $-z$ ($R_{\mathrm{th},-z}$), $+y$ ($R_{\mathrm{th},+y}$), $-$y ($R_{\mathrm{th},-y}$), $+x$ ($R_{\mathrm{th},+x}$) and $-x$ ($R_{\mathrm{th},-x}$)

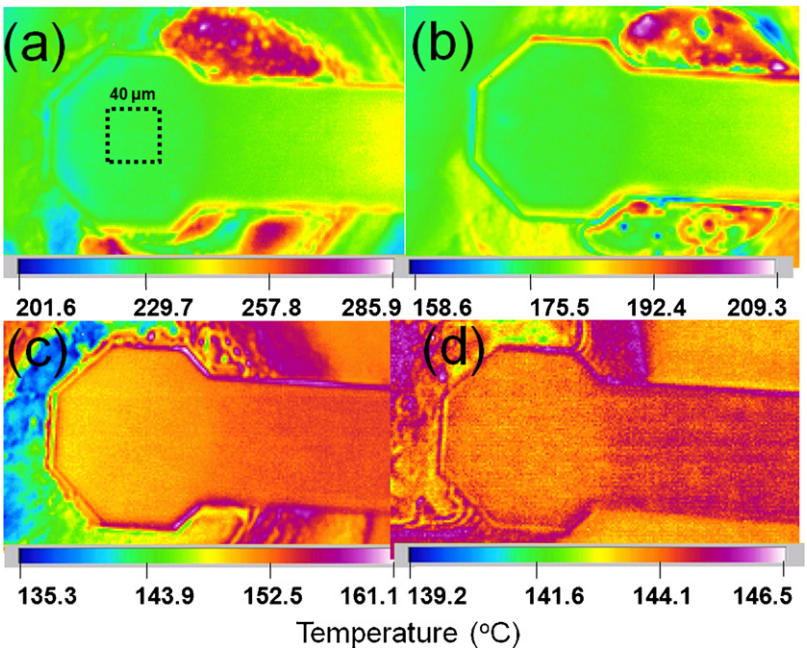

Fig. 4. Temperature map obtained by infrared microscopy on the Al-pad of bump B1 when a current of 1.0 A was applied in joints with a die of (a) 60 μm (b) 100 μm (c) 250 μm (d) 760 μm thick. The thinner the die is, the higher the Joule heating effect will be.

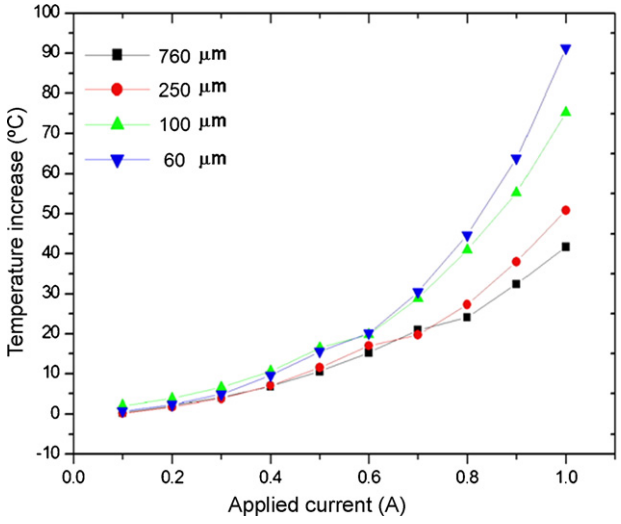

Fig. 5. The measured temperatures in the Al pad of bump B1 as a function of applied currents up to 1.0 A for the four sets of solder joints.

Fig. 6. One-dimensional lumped model for thermal resistance. The major heat generator is the Al trace and the Si die dissipates most of the heat.

Table 2
The thermal conductivities for the materials used in this study.

Material	Conductivity ($W\,m^{-1}\,K^{-1}$)
Si	147.00
Cu	260.00
Ni	76.00
SnPb	50.00
Underfill	0.50
FR4 substrate	0.55
Convection coefficient ($W\,m^{-2}\,K^{-1}$)	
Air	25

directions can be expressed as

$$R_{\mathrm{th},-z} = \left(\frac{1}{R^{\mathrm{Solder}}_{\mathrm{th},-z}} + \frac{1}{R^{\mathrm{Underfill}}_{\mathrm{th},-z}}\right)^{-1} + R^{\mathrm{Substrate}}_{\mathrm{th},-z}$$
$$= \frac{t^{\mathrm{Solder}}}{34 \times k^{\mathrm{Solder}} A_z^{\mathrm{Solder}} + k^{\mathrm{Underfill}} A_z^{\mathrm{Underfill}}} + \frac{t^{\mathrm{Substrate}}}{k^{\mathrm{Substrate}} A_z} \quad (4)$$
$$= 2.9 + 937.5 = 940.4$$

There are 34 solder bumps in the test chip.

$$R_{\mathrm{th},+y} = R^{\mathrm{Si}}_{\mathrm{th},+y} + R^{\mathrm{Air}}_{\mathrm{th},+y} = \frac{L^{\mathrm{Si}}_{+y}}{k^{\mathrm{Si}} A_y} + \frac{1}{h^{\mathrm{Air}} A_y} = 0.7 + 9837.7 = 9838.4 \quad (5)$$

Table 3
The dimensions used for the calculation of thermal resistance.

t^{Si}	760 μm
A_z	$2.33 \times 10^{-5}\ m^2$ (4.35 mm × 5.35 mm)
t^{Solder}	108 μm
A_z^{Solder}	$1.31 \times 10^{-8}\ m^2$ ($\pi \times 108^2\ \mu m^2$)
$A_z^{\mathrm{Underfill}}$	$=A_z - 34 \times A_z^{\mathrm{Solder}}$
$t^{\mathrm{Underfill}}$	$=T^{\mathrm{Solder}}$
A_y	$4.07 \times 10^{-6}\ m^2$ (760 μm × 5.35 mm)
L^{Si}_{+y}	3925 μm (4350–425 μm)
L^{Si}_{-y}	425 μm

Table 4
Calculated thermal resistance for flip-chip packages with different die thicknesses.

Thickness of Si die (μm)	Vertical direction		Horizontal direction				Effective thermal resistance ($K W^{-1}$)
	(+z)	(−z)	(−y)	(+y)	(+x)	(−x)	
760.0	1719.0	940.4	9838.4	9844.2	12104.7	12104.7	496.6
300.0	1718.9	940.4	24923.9	24938.8	30665.3	30665.3	558.5
100.0	1718.8	940.4	74771.8	74816.3	91995.9	91995.9	590.4
60.0	1718.8	940.4	124619.6	124693.8	153326.4	153326.4	597.3

Table 5
Failure time of the flip-chip joints with various die area under current stressing of 1 A at 100 °C.

Die area (μm^2)	5350 × 4350	5350 × 3600	5350 × 3000	5350 × 2000	5350 × 1000
Failure time (h)	1608.0	28.0	10.6	5.0	0.3
$\triangle T$ (°C)	41.7	57.3	70.3	89.5	171.2

$$R_{\text{th},-y} = R^{\text{Si}}_{\text{th},-y} + R^{\text{Air}}_{\text{th},-y} = \frac{L^{\text{Si}}_{-y}}{k^{\text{Si}}A_y} + \frac{1}{h^{\text{Air}}A_y} = 6.6 + 9837.7 = 9844.3 \quad (6)$$

$$R_{\text{th},+x} = R_{\text{th},-x} = R^{\text{Si}}_{\text{th},+x} + R^{\text{Air}}_{\text{th},+x} = \frac{L^{\text{Si}}_{+x}}{k^{\text{Si}}A_x} + \frac{1}{h^{\text{Air}}A_x} = 5.5 + 12099.2 = 12104.7 \quad (7)$$

Therefore, the effective thermal resistance, $R_{\text{th,total}}$, can be estimated as

$$R = \left(R^{-1}_{\text{th},+z} + R^{-1}_{\text{th},-z} + R^{-1}_{\text{th},+y} + R^{-1}_{\text{th},-y} + R^{-1}_{\text{th},+x} + R^{-1}_{\text{th},-x}\right)^{-1} \quad (8)$$

The calculated vertical, lateral and effective thermal resistances for the four packages are listed in Table 4. The effective thermal resistance is obtained by treating the thermal resistance in the six directions in parallel, as shown in Eq. (8). Although the thermal resistance is smaller for a thin die, the results in Table 4 show that the vertical thermal resistance through the Si die almost remains the same as the die is thinned down. This is because the air convection is considered on the top surface of the Si die and the air convection serves as the bottleneck for the heat dissipation in the +z direction. Thus, the calculated thermal resistance did not vary with the die thickness in this direction. However, the lateral thermal resistance increases dramatically as the die thickness decreases. The effective thermal resistance is 496.6, 558.5, 590.4, and 597.3 $K W^{-1}$ for the 760-, 250-, 100-, and 60-μm thick die, respectively. That is, the thermal dissipation is more difficult in flip-chip solder with a thinner die. Therefore, the Joule heating effect becomes more pronounced for a thin die, which results in a short electromigration lifetime.

Furthermore, Si-die area also makes a significant influence on the electromigration failure time of flip-chip solder joints. Table 5 summarizes the failure time and temperature increase for the solder joints with die area of 5350 × 4350 μm^2, 5350 × 3600 μm^2, 5350 × 3000 μm^2, 5350 × 2000 μm^2 and 5350 × 1000 μm^2. The failure time is 1608.0, 28.0, 10.6, 5.0 and 0.3 h for the five samples. As the die area decreases, the electromigration failure time decreases. Similar to the analysis above, Joule heating plays a key role in the dramatic differences in failure time, since the current distributions in the solder bumps are identical for the five samples. Fig. 7 shows the increasing temperature as a function of applied current for the five samples. The temperature increase is 41.7 °C for the as-fabricated sample stressed at 1.0 A at 100 °C. As the die area decrease to 5350 × 3000 μm^2, which is about 69% of the as-fabricated sample, the temperature increases to 70.3 °C. The temperature reaches the melting point of the eutectic SnPb solder (183 °C) when the die area further shrinks to 5350 × 2000 μm^2. As delineated in Eq. (1), three parameters may affect the EM lifetime of solder joints: temperature, current density, and activation. In the present study, the last two parameters were unchanged as the dies were thinned down or the area of the dies was decreased. Thus, only the temperature term can affect the EM lifetime. The temperature term is in the exponential term and thus the temperature increase due to Joule heating effect has profound influence on the electro-migration failure time.

The reason for the serious Joule heating effect in smaller dies may be attributed to smaller area for heat dissipation. One can also estimate the thermal resistance for the five samples using Eqs. (3) through (8). Table 6 tabulates the calculated thermal resistance for flip-chip joints with different die area. The thermal resistance becomes larger as the die area shrinks. The effective thermal resistance is 496.6, 587.6, 688.6, 965.0, and 1613.0 $K W^{-1}$ for the 5350 × 4350 μm^2, 5350 × 3600 μm^2, 5350 × 3000 μm^2, 5350 × 2000 μm^2 and 5350 × 1000 μm^2 die area, respectively. Therefore, the temperature increase turns out to be larger for a smaller die. It is noteworthy that the area of the FR4 substrate may also plays an important role on the heat dissipation, in addition to Si die. As the samples are ground laterally, both the area of the Si die and the substrate decreases. Yet, more studies needs to be done to understand the effect of substrate size on the electromigration of flip-chip solder joints.

The shrinkage of the dies may have a larger effect on the heat dissipation rate than the thinning of the dies in the present study. As shown in Tables 4 and 6, when the die thickness

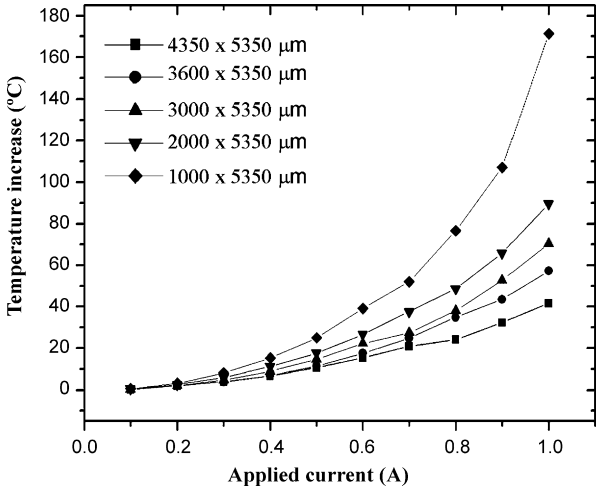

Fig. 7. The measured temperatures in the Al pad of bump B1 as a function of applied currents up to 1.0 A for the five samples with various area.

Table 6
Calculated thermal resistance for flip-chip packages with different die area.

Si-die length (μm)	Vertical direction		Horizontal direction				Effective thermal resistance ($K W^{-1}$)
	(+z)	(−z)	(−y)	(+y)	(+x)	(−x)	
4350.0	1719.0	940.4	9838.4	9844.2	12104.7	12104.7	496.6
3600.0	2077.1	1135.9	9838.4	9843.0	14626.5	14626.5	587.6
3000.0	2492.5	1362.6	9838.4	9842.0	17551.8	17551.8	688.6
2000.0	3738.8	2042.6	9838.4	9840.3	26327.8	26327.8	965.0
1000.0	7477.6	4082.0	9838.4	9838.6	52655.5	52655.5	1613.0

decreased to 40% of its original value (from 760 μm to 300 μm), the effective thermal resistance increased approximately 12.5%. However, as the die area reduced to 46% of its original area (from $5350 \times 4350\,\mu m^2$ to $5350 \times 2000\,\mu m^2$), the effect thermal resistance increase 94.3%. The experimental data on temperature increasing listed in Tables 1 and 5 also have the same trend with the calculated effective thermal resistance. Therefore, compared with the thinning of the dies, the shrinkage of the dies may have bigger effect on heat dissipation rate.

It is noteworthy that the above thermal resistance model may not be able to explain ability of dissipation of Joule heat unless the temperature differences in all directions are known. In addition, thermal contact resistance should be taken into consideration across different solid bodies. A more rigid model or finite element simulation should be carried out to explain the experimental results in details.

4. Conclusion

In summary, the electromigration lifetime depends strongly on the dimension of the silicon chip. It is found that the dimension of the silicon chip plays a crucial role in the Joule heating effect, because the silicon die has good thermal conductivity and heat dissipation. Under the same stressing current, the thinner Si die exhibited a higher increasing temperature, because the overall thermal resistance increases for the package with a thinner die. As a result, the thinner die makes a significantly increase in Joule heating effect. The results indicate that electro-migration would become a more important issue for devices with thin and small dies.

Acknowledgements

The authors would like to present a hearty thank to the National Science Council of R.O.C. for the financial support through grant No. 95-2221-E-009-088MY3. In addition, the assistance of Michael Tong on English editing is greatly appreciated.

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