行政院國家科學委員會補助專題研究計畫成果報告

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※　奈米 CMOS 通道背向散射實驗及其潛在性應用之研究(3/3) ※

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計畫類別：■個別型計畫　　□整合型計畫

計畫編號：NSC 96-2221-E-009-187-

執行期間：96/08/01 ~ 97/07/31

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執行單位：**國立交通大學電子工程學系及電子研究所**

中　華　民　國　97　年　10　月　30　日

行政院國家科學委員會補助專題研究計畫成果報告

奈米 CMOS 通道背向散射實驗及其潛在性應用之研究(3/3)

Nano-CMOS Channel Backscattering Experiment and Its Potential Applications

執行期限: 96/08/01 ~ 97/07/31
計畫編號: NSC 96-2221-E-009-187-

主持人：陳明哲教授　　國立交通大學電子工程學系及電子研究所

一、中文摘要

本計劃為期三年，進行通道背向散射實驗並找到在奈米場效電晶體上的應用。第一年建立通道背向散射實驗之核心：(1) 一維解薛丁格-浦以松方程式量子力學模擬器以從電容電壓數據萃取製程參數，藉由此得到在開始的 K_BT 層中的平均熱入射速度，等效閘電容和近似於平衡臨界電壓; (2) 次臨界 DIBL 量測以有效計入二維效應的影響; (3) 利用比例與位移方法估計源極/集極的串聯電阻和通道或閘極的長度; (4) 利用近似於平衡的遷移率量測， 去量化橫跨 K_BT 層的背向散射自由平均路徑; (5) 利用電流電壓擬似法決定 K_BT 層的寬度; 最後， (6) 利用機率和統計知識、微觀傳輸物理、解浦以松方程式和蒙地卡羅模擬，有系統的去處理與證明所萃取出來的 K_BT 層寬度和他們的物理意義及製程關鍵指引。據此實驗核心，我們進行：(1) 通道背向散射實驗應用於 Bulk 奈米場效電晶體測試晶片; (2) Bulk 奈米場效電晶體雜訊實驗並與通道背向散射數據相關性探討; 以及(3) Bulk 奈米場效電晶體介觀物理理解、特性分析（經由機率和統計處理）、簡潔元件模型、元件製造關鍵和設計規範之建立。

關鍵詞：奈米場效電晶體，通道背向散射，介觀物理，矽變形奈米場效電晶體，雙倍式閘極奈米場效電晶體，鍺通道奈米場效電晶體，雜訊。

英文摘要

This is a three-years project to perform channel backscattering experiment and find potential applications in nanoFETs. In the first year, the core of channel backscattering experiment to be established consists of the following key elements: (1) 1-D self-consistent Schrodinger-Poisson quantum simulator such as to assess process parameters from C-V data, which in turn can quantify average thermal injection velocity at the beginning of the K_BT layer, effective gate capacitance, and quasi-equilibrium threshold voltage; (2) subthreshold DIBL measurement to account for 2-D effect; (3) usage of ratio-and-shift method to measure source/drain series resistances and gate or channel length; (4) long-channel quasi-equilibrium mobility measurement in order to quantify mean-free-path for backscattering over the K_BT layer; (5) I-V fitting to determine the width of the K_BT layer; and finally (6) applying knowledge of probability and statistics, microscopic transport physics, solving of Poisson equation, and Monte Carlo simulation, in a systematical way to deal with and clarify the extracted K_BT layer width, as well as underlying physical meanings and key process guidelines. Based on this experimental set-up, we proceed with the following: (1) application of channel backscattering experiment to bulk nanoFET test devices; (2) noise measurement on bulk nanoFETs along with correlation with channel backscattering data; and (3) establishment of bulk nanoFETs mesoscopic physics and understanding, characteristics analysis (via probability and statistics), compact model, key for devices manufacturing, and design guidelines.

Key Words: NanoFETs, Channel Backscattering, Mesoscopic Physics, Strained-Silicon NanoFETs, Double-Gate NanoFETs, Germanium Channel NanoFETs.

二、緣由與目的

歐盟最近通過了為期至少 3 年的 Nano-CMOS 泛歐大計劃 (自 2004 年 3 月開始). 此重大事件意味著兩件事：一方面， Nano-CMOS 繼續為國際間重點研究題目；另方面，來自 Nano-CMOS 領域國際同儕的品質要求與日俱增，在此領域非得做出好的研究不可。在 Nano-CMOS 廣泛領域中，以 Channel Backscattering 為基礎的載子傳輸理論，國際上公認為描述下世代奈米元件物理行為特性的嶄新語言，理論創始人普渡大學 Mark Lundstrom 及 Supriyo Datta 兩位教授並因而獲得 2002 年 IEDM Cledo Brunetti 獎。 數年前我们就已進行 Channel Backscattering 理論及相關量測之研究並有一篇 IEDM 2002 年論文發表，日以繼夜研究到現在，以 2004 年 9 月產出一篇 IEEE TED 長文最有代表性. IEEE TED 兩位國際評審也高度肯定此論文

之嚴謹及有用性。此論文詳細報告如何適當的進行通道背向散射實驗（channel backscattering experiment)並找到在奈米場效電晶體上的應用。過去的經驗讓我們了解，透過關鍵地帶 (K_BT Layer) 的研究，可得到有相當建設性的介觀 (mesoscopic) 物理理解、特性分析（經由機率和統計處理），Compact 元件模型建立，和奈米場效電晶體元件的製造關鍵等等。通道背向散射實驗均適用於傳統的金氧半場效電晶體（Nano Bulk MOSFETs）、雙倍式閘極場效電晶體（double-gate Nano-FETs）、矽變形場效電晶體（strained-silicon Nano-FETs）和鍺通道場效電晶體（germanium-channel Nano-FETs）等。

因此我們草擬以 Nano-CMOS channel backscattering experiment 為主題的國科會 3 年計劃，此實驗的核心為:

(i) 一維的 self-consistent Schrodinger-Poisson solver 從 C-V data 粹取製程參數，藉由此製程參數可以得到在開始的 K_BT layer 中的平均熱入射速度(average thermal injection velocity)，等效閘電容(effective gate capacitance) 和近似於平衡臨界電壓(quasi-equilibrium threshold voltage);

(ii) Subthreshold DIBL(drain-induced barrier lowering)量測以有效計入二維效應的影響;

(iii) 利用比例與位移方法(ratio-and-shift method)去估計源極/集極(source/drain)的串聯電阻和通道或閘極(gate)的長度;

(iv) 利用近似於平衡(quasi-equilibrium)的遷移率(mobility)量測，去量化橫跨 layer 的背向散射自由平均路徑(mean-free-path for backscattering) ;

(v) 利用 I-V fitting 的方法去 K_BT layer 的寬度;

(vi) 然後利用機率和統計 Knowledge，微觀傳輸物理，解浦以松方程式(Poisson equation along the channel direction)和蒙地卡羅模擬(Monte Carlo simulation)，有系統的去處理與證明所粹取出來的 K_BT layer 寬度和他們的物理意義及製程關鍵指引。

三、研究方法與成果

已建立 channel backscattering 實驗核心:

1. 1-D self-consistent Schrodinger-Poisson solver 從 C-V data 粹取製程參數，藉由此製程參數以得到在開始的 K_BT layer 中的平均熱入射速度，等效閘電容和近似於平衡臨界電壓;
2. Subthreshold DIBL 量測以有效計入二維效應的影響;
3. 利用比例與位移方法去估計源極/集極的串聯電阻和通道或閘極的長度;
4. 利用近似於平衡的遷移率量測，去量化橫跨 layer 的背向散射自由平均路徑; 利用 I-V fitting 的方法去 K_BT layer 的寬度;
5. 然後利用機率和統計 Knowledge，微觀傳輸物理，解浦以松方程式和蒙地卡羅模擬，有系統的去處理與證明所萃取出來的 K_BT layer 寬度和他們的物理意義及製程關鍵指引。

四、結論與討論 (i)

在 Nano-CMOS 通道背向散射(即波動導向的下世代奈米元件物理)領域，本人研究群這幾年完成了大量的實驗工作,改進了原先的理論模式,發表了一系列相關論文，並被知名學術界及世界級研發機構引用:

- Stanford-MIT team in a 2004 *IEDM* paper “Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs”
- TSMC in a 2005 *Symposium on VLSI Technology* paper “The impact of uniaxial strain engineering on channel backscattering in nanoscale MOSFETs”
- STMicroelectronics/CNRS/LETI/NXP Semiconductor in 2005 December Issue of IEEE TED “A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET”
- TSMC in 2006 *IEEE EDL*
- TSMC in 2006 *VLSI-TSA*
- CEA/LETI/L2MP (France) in 2007 *Symposium on VLSI Technology*: “Will strain be useful for 10nm quasi-ballistic FDSOI devices? An experimental study”
- (Univ. Udine, Italy) M. Zilli, P. Palestri, D. Esseni, and L. Selmi, “On the experimental determination of channel backscattering in nanoMOSFETs,” *IEEE IEDM*, p. 105, 2007.
- (Beijing Uni., China and Sumsung, Korea) Y. Tian, et al., “New self-aligned silicon nanowire transistors on bulk substrate fabricated by Epi-free compatible CMOS technology: process integration, experimental characterization of carrier transport and low frequency noise,” *IEEE IEDM*, p. 895, 2007.
- (Grenoble, France) M. Ferrier, et al., “Conventional technological boosters for injection velocity in ultrathin-body MOSFETs,” *IEEE Nanotechnology*, vol. 6, pp. 613-621, Nov. 2007.

- (Bologna Univ. Italy) C. Fiegna, Y. Yang, E. Sangiorgi, et al., "Analysis of self-heating effects in ultrathin-body SOI MOSFETs by device simulation," *IEEE TED*, vol. 55, pp. 233-244, Jan. 2008.
- (MIT) A. Khakifirooz and D. A. Antoniadis, "MOSFET performance scaling-Part I: Historical Trends," *IEEE TED*, vol. 55, pp. 1391-1400, June 2008.

簡言之，目下傳統的半導體元件物理已不能應付下世代奈米元件物理所需，以波動導向觀點的物理圖像則趁勢而起。本人在此關鍵領域的成功可由 Prof. Gerhard Klimeck, Technical Director, Network for Computational Nanotechnology, Purdue University, 01/10 2007 e-mail 中的一段得知: "..Interestingly enough we have difficulty trying to get success stories like this and the NSF keeps asking us if the site is useful for research….". 本人最近更審查國外十幾篇有關 Channel Backscattering 的 submitted papers.

五、結論與討論 (ii)

應變矽技術最近已被廣泛應用在奈米 CMOS 製程技術中。 主要有二種不同的方法在製程中加入應力: (1) 在矽鍺基板上長出磊晶矽原子層; 以及(2) 利用製程步驟本身及材料性質差異製造應力，如：淺塹渠絕緣、覆蓋層、矽化物或者矽鍺源汲極等。至目前為止，針對機械應力的重要性有兩個主要的探討方向。其一是晶圓在生產過程所感受的機械應力會增強或減緩雜質的擴散，也因此影響最終摻雜在元件之中分佈的情形。在做了上述這些製程的改變後，檢驗應變矽元件表面特性及閘級介電層的健全度是否受到影響是很重要的。另一方面，機械應力也可改變元件的能帶結構，因之改變了電晶體特性，諸如載子遷移率、熱載子造成的可靠度問題、臨界電壓和閘極直接穿隧電流等。憑仗這幾年的努力，我們已在應變矽技術領域產出重要成果:

- 利用閘極直接穿隧電流估算應變矽金氧半場效電晶體通道應力大小

能夠定量的推斷出元件結構內部的應力大小及應力的種類(如：壓縮應力、伸張應力)是必要的。目前已經有三種評估元件結構內部應力的方法被提出：(1) 彎曲晶圓夾具，(2)精密的應力模擬，及(3)拉曼光譜。但是利用電晶體電性改變來推斷內部應力大小及種類的方法仍未被提出過。然而，值得一提的是經由外部施加應力造成的閘極直接穿隧電流改變已經被深入的探討過了。另一方面，根據最近的研究，形變位能係數已經可由實驗萃取而得，並且和理論計算所預測的值一致。因此，在形變位能係數已知的情況下，利用閘級穿隧電流來反推元件內部應力大小已經變成一個可行的方案。研究細節可參考我們發表的相關文獻:

C. Y. Hsieh and M. J. Chen, "Measurement of channel stress using gate direct tunneling current in uniaxially stressed n-MOSFETs," *IEEE Electron Device Letters*, vol. 28, pp. 818-820, Sept. 2007.

- 應力製程微觀物理

我們在產製下世代受應力電子元件 Strain Engineering 領域針對 Uniaxial Strain 下 Impurities (為目前國際上高度挑戰卻也爭議性極大的題目) 在 Silicon 的高溫特殊擴散行為提出前所未有、創新微觀物理模式並獲得實驗強力支持。且藉由成熟的元件製程模擬，所謂的 TCAD(製程電腦輔助設計)，可以延伸到實際元件的應用。研究細節可參考我們發表的相關文獻:

1. M. J. Chen and Y. M. Sheu, "Effect of uniaxial strain on anisotropic diffusion in silicon," *Applied Physics Letters*, Vol. 89, pp. 161908-1-181908-3, Oct., 2006.

2. Y. M. Sheu, S. J. Yang, C. C. Wang, C. S. Chang, L. P. Huang, T. Y. Huang, M. J. Chen, and C. H. Diaz, "Modeling mechanical stress effect on dopant diffusion in scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. **52**, pp. 30-38, January 2005.

此兩篇論文最近被跨國際團隊(IMEC, Univ. Leuven, ASM USA, ASM Belgium, and TI)引用:

E. Simoen, et al., "Leakage current study of $Si_{1-x}C_x$ embedded source/drain junctions," Applied Surface Science, vo. 254, pp. 6140-6143, March 2008.

- 藉由邊緣直接穿隧電流量測在機械應力下雜質的擴散情況

能夠擁有從電性量測反推元件因生產過程而增強或是減低雜質擴散的能力是不可或缺的。傳統上，這是由 TCAD 來達成。我們提出了一個電性的方法,稱之為邊緣直接穿隧電流的方式，可直接地決定在源極及汲極的局部機械應力對摻雜在通道中橫向的擴散。研究細節可參考我們發表的一篇長文:

C. Y. Hsieh and M. J. Chen, "Electrical measurement of local stress and lateral diffusion near source/drain extension corner of uniaxially stressed n-MOSFETs," *IEEE Trans. Electron Devices*, vol.55, pp. 844-849, March 2008.

- 量測應變矽 MOSFETs 閘級介電層與矽介面的缺陷密度

在做了應變製程的改變後，檢驗應變矽元件表面特性及閘級氧化層介面的健全度是否受到影響是很重要的。而我們最近進行的應變矽 MOSFETs 元件的 1/f 低頻雜訊量測正好可以作為此一議題深入分析的有效工具。研究細節可參考我們發表的相關文獻:

1. M. P. Lu, W. C. Lee, M. J. Chen, "Channel-width dependence of low-frequency noise in process tensile-strained n-channel metal-oxide-semiconductor transistors," *Applied Physics Letters*, vol. **88**, pp. 063511-1—063511-3, Feb. 2006.

2. C. Y. Hsieh, Y. T. Lin, T. H. Liang, W. C. Lee, J. B. Bouche, and M. J. Chen, "Effect of STI mechanical stress on p-channel gate oxide integrity," *IEEE Semiconductor Interface Specialist Conference*, p.5, 2007.

- 我們另有其他貢獻於應變矽技術領域者:

國際上, 從事應變矽技術的研究者在 *IEEE Symposium on VLSI Technology* 頂尖國際會議上引用了我們的成果:

1. H. Tsuno, K. Anzai, M. Matsumura, S. Minami, A. Honjo, H. Koike, Y. Hiura, A. Takeo, W. Fu, Y. Fukuzaki, M. Kanno, H. Ansai, and N. Nagashima, "Advanced analysis and modeling of MOSFET characteristics fluctuation caused by layout variation," *IEEE Symposium on VLSI Technology*, p. 204, 2007.

2. V. Barral, et al., "Will strain be useful for 10nm quasi-ballistic FDSOI devices? An experimental study," *IEEE Symposium on VLSI Technology*, p. 128, 2007.

3. H. N. Lin, et al., "The impact of uniaxial strain engineering on channel backscattering in nanoscale MOSFETs" *IEEE Symposium on VLSI Technology*, p. 174, 2005.

- 我們培育出應變矽技術的頂尖人才:

1. 許義明博士: 2007 年畢業(with Ph.D. Dissertation entitled "Layout Dependent Effect on Advanced MOSFETs") 即成為 TSMC RD Manager. TCAD and Device Engineering 領域權威, 曾發表多篇 IEDM 及 Symposium on VLSI Technology 會議論文.

2. 黃煥宗博士：TSMC 32/22 奈米 RD 技術經理; 2003-2005 年選派為 Scientist to Freescale Company, USA. 曾發表多篇 IEDM 及 Symposium on VLSI Technology 會議論文; 去年就以第一作者領銜一篇 IEDM 論文: H. T. Huang, et al., "45nm high-k/metal-gate CMOS technology for GPU/NPU applications with highest PFET performance," *IEEE IEDM Tech. Dig.*, p. 285, 2007.

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2. Y. M. Sheu, S. J. Yang, C. C. Wang, C. S. Chang, L. P. Huang, T. Y. Huang, M. J. Chen, and C. H. Diaz, "Modeling mechanical stress effect on dopant diffusion in scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. **52**, pp. 30-38, January 2005.
3. M. P. Lu, C. Y. Hsian, P. Y. Lo, J. H. Wei, Y. S. Yang, and M. J. Chen, "Semiconducting single-walled carbon nanotubes exposed to distilled water and aqueous solution: electrical measurement and theoretical calculation," *Applied Physics Letters*, vol. 88, pp. 053114-1—053114-3, Feb. 2006.
4. M. P. Lu, C. Y. Hsian, P. Y. Lo, J. H. Wei, Y. S. Yang, and M. J. Chen, "Semiconducting single-walled carbon nanotubes exposed to distilled water and aqueous solution: electrical measurement and theoretical calculation," Selected Articles in *Virtual Journal of Nanoscale Science & Technology*, Vol. **13**, Issue 6, 2006.
5. M. P. Lu, C. Y. Hsian, P. Y. Lo, J. H. Wei, Y. S. Yang, and M. J. Chen, "Semiconducting single-walled carbon nanotubes exposed to distilled water and aqueous solution: electrical measurement and theoretical calculation," Selected Articles in *Virtual Journal of Biological Physics Research*, Vol. **11**, Issue 4, 2006.
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9. M. J. Chen and Y. M. Sheu, "Effect of uniaxial strain on anisotropic diffusion in silicon," *Applied Physics Letters*, Vol. 89, pp. 161908-1-181908-3, Oct., 2006.
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11. C. Y. Hsieh and M. J. Chen, "Measurement of channel stress using gate direct tunneling current in uniaxially stressed n-MOSFETs," *IEEE Electron Device Letters*, vol. 28, pp. 818-820, Sept. 2007.
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Important Figures(see attached papers)

A Parabolic Potential Barrier-Oriented Compact Model for the k_BT Layer's Width in Nano-MOSFETs

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***Abstract*—On the basis of a parabolic potential profile around the source-channel junction barrier of nanoscale MOSFETs, a new compact model is physically derived, which links the width of thermal energy k_BT layer (a critical zone in the context of the backscattering theory) to the geometrical and bias parameters of the devices. The proposed model is supported by experimental data and by a critical analysis of various simulation works presented in the literature. The only fitting parameter remains constant in a wide range of channel length (10–65 nm), gate voltage (0.4–1.2 V), drain voltage (0.2–1.2 V), and temperature (100 K–500 K). The confusing temperature-dependent issues in the open literature are straightforwardly clarified.**

***Index Terms*—Backscattering, MOSFET, nanometer.**

I. Introduction

While applied to electrically saturated nanoscale MOSFETs, the channel backscattering theory [1], [2] establishes a link between the thermal energy k_BT layer, which occupies a small fraction of the conductive channel near the source, and the drive capability of the device. Thus, the ability to quantitatively determine the width of this critical zone is essential. To address the issue transparently, an analytically compact treatment is desirable. One such model can be quoted in the literature [3]

$$l \approx L\left(\frac{k_BT}{qV_D}\right)^{\alpha} \tag{1}$$

where l is the width of the k_BT layer, and L is the metallurgical channel length. However, so far, there has been some confusion as to the magnitude of the temperature power exponent α. First of all, fitting of the room-temperature I–V characteristics of a simulation double-gate MOSFET has produced the apparent $\alpha \approx 0.57$ [3]. Comparable $\alpha \approx 0.5$ has also been obtained on experimental bulk n-MOSFETs in a temperature range of 233 K–298 K [4], [5]. In contrast, for the bulk case covering the same temperature range, a higher $\alpha \approx 0.75$ has been experimentally determined [6]. Even $\alpha \approx 1$ has already been adopted in a temperature-dependent backscattering-coefficient extraction method [7]. This is also the case for the recent double-gate device simulation [8], which has shown that l is approximately proportional to the temperature from 100 K to 500 K. Obviously, these widespread values of the apparent α must be clarified. On the other hand, a study on experimental bulk n-MOSFETs has revealed that l significantly decreases with increasing gate voltage [4], [6]; however, it is difficult for (1) to elucidate due to the lack of the gate voltage. This hurdle may be overcome by accurate modeling of the potential profile in the channel [9]; however, a simple approach without loss of accuracy is favored.

In this brief, the experimentally determined parabolic potential profile in the previous work [4], [5] will be utilized to approximate the source-channel junction barrier of nanoscale MOSFETs in saturation. Then, a new compact model will be physically derived for l with the channel length, gate overdrive, drain voltage, and temperature as input parameters. The validity and applicability of the resulting model will also be examined, followed by a significant clarification on the aforementioned α differences.

II. Parabolic Barrier Picture

A parabolic potential profile near the source is schematically shown in Fig. 1. Its extension to the remaining channel can be described by

$$V(x) = V_D(x/\widetilde{L})^2. \tag{2}$$

The origin $x = 0$ indicates the peak of the barrier. $\widetilde{L}$ is the apparent channel length corresponding to a certain position where the parabolic potential drop from the top of the barrier is equal to V_D. Here, the barrier height with respect to the source side is neglected due to the large drain voltages used. By substituting $x = l$ into (2) for a local potential drop of k_BT/q to constitute the thermal energy layer [1], [2], the following expression can be obtained:

$$l = \widetilde{L}\left(\frac{k_BT}{qV_D}\right)^{0.5}. \tag{3}$$

$\widetilde{L}$ is expected to be a function of the channel length, gate and drain voltage, and temperature. In other words, there exists a set

Manuscript received November 15, 2007; revised January 28, 2008. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC 96-2221-E-009-187. The review of this brief was arranged by Editor C. Jungemann.

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Digital Object Identifier 10.1109/TED.2008.919317

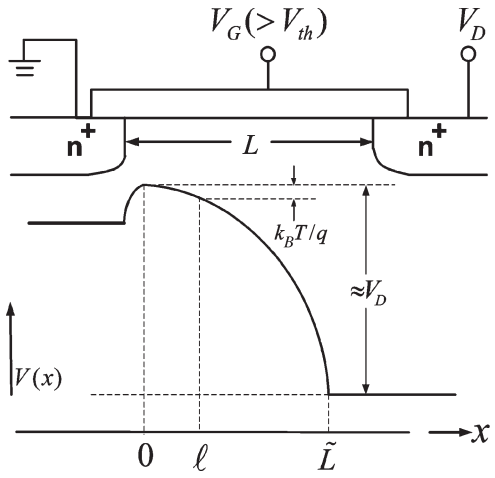

Fig. 1. Schematic demonstration of the parabolic source-channel potential barrier picture corresponding to nano-MOSFET in saturation. The parabolic potential profile is extended to the drain side to highlight the apparent channel length designated by $\widetilde{L}$. Also shown is the width l of the k_BT layer.

of the specific gate and drain voltage denoted by $V_{\rm Go}$ and $V_{\rm Do}$, respectively, at a given temperature T_o, which can ensure that $\widetilde{L} = L$. The corresponding thermal energy layer has a width denoted by l_o, which can be calculated from (3) with $\widetilde{L} \to L$, $T \to T_o$, and $V_D \to V_{\rm Do}$. Then, if the temperature individually changes from T_o to T, a power-law relation can hold: $\widetilde{L} = L(T/T_o)^{0.5}$. This formalism can be obtained by assuming that the potential profile does not change with temperature; that is, the local electric field across the thermal energy layer ($\approx k_BT_o/ql_o$, according to the backscattering theory [1], [2]) at T_o is approximately equal to that ($\approx k_BT/ql$) at T. As for gate-voltage factor, a similar relation can be physically derived but expressed in terms of the gate overdrive (the gate voltage V_G minus the threshold voltage $V_{\rm th}$). This is achieved by twice differentiating (2) with respect to x, leading to $d^2V(x)/dx^2 = 2V_D/\widetilde{L}^2$, which, according to Poisson's equation (see [3] for details), can be linearly related to the underlying inversion-layer carrier density or, equivalently, the gate overdrive. As a result, one achieves $\widetilde{L} = L((V_{\rm Go} - V_{\rm th})/(V_G - V_{\rm th}))^{0.5}$. Here, the term $V_{\rm Go} - V_{\rm th}$ represents the specific gate overdrive for $\widetilde{L}$ approaching L. Finally, if the drain voltage increases to $V_D(> V_{\rm Do})$, the local electric field [$= 2V_Dx/\widetilde{L}^2$ as from (2)] must be larger than that ($= 2V_{\rm Do}x/L^2$) at $V_{\rm Do}$. As a result, one obtains $\widetilde{L} = L(V_D/V_{\rm Do})^{\nu}$ with the power exponent ν of no more than 0.5. This formula remains valid for $V_D < V_{\rm Do}$. Indeed, ν of around 0.25 has been experimentally determined elsewhere [4] and will be cited here.

Through the combination of the aforementioned power-law relationships, a unique expression can be created for $\widetilde{L}$

$$\widetilde{L} = \eta L \frac{V_D^{0.25}}{(V_G - V_{\rm th})^{0.5}} \left(\frac{k_BT}{q}\right)^{0.5}. \tag{4}$$

Here, $\eta = (k_BT_o/q)^{-0.5}(V_{\rm Go} - V_{\rm th})^{0.5}V_{\rm Do}^{-0.25}$. In this brief, η is fixed and is also the only fitting parameter. It is expected that η is a constant, regardless of the channel length, gate and drain voltage, and temperature; otherwise, the applicability of the resulting model may be limited.

III. Confirmative Evidence and Clarification

The experimental l was created from 55-nm bulk n-MOSFETs by means of a parameter extraction process detailed elsewhere [4]–[6]. The results are shown in Fig. 2 versus gate voltage for two drain voltages of 0.5 and 1.0 V and three temperatures of 233 K, 263 K, and 298 K. With known l, T, and V_D, the corresponding $\widetilde{L}$ can be obtained directly from (3), as shown in Fig. 2(c) and (d) versus the gate voltage. The near-equilibrium threshold voltages denoted by $V_{\rm tho}$ are 0.360, 0.345, and 0.328 V for 233 K, 263 K, and 298 K, respectively, and the drain-induced barrier lowering (DIBL) magnitudes are 120, 123, and 130 mV/V, respectively. Throughout this brief, the threshold voltage $V_{\rm th}$ at higher drain voltages is equal to $V_{\rm tho} - {\rm DIBL} \times V_D$ [4]–[7]. Also shown in Fig. 2 are the calculated results from (3) and (4) using a specific η whose value will be explained slightly later. On the other hand, the rich literature [8], [10] dedicated to double-gate device simulations is quoted. First, in [8], the extracted l at $V_D = V_G = 1$ V is available in a wide range of the channel length from 14 to 37 nm and the temperature from 100 K to 500 K. The underlying threshold voltage $V_{\rm tho}$ and DIBL are reasonably 0.3 V and 110 mV/V, respectively [10]. Second, the citation [10] can further provide the relevant data at 300 K: l from 2.0 to 7.0 nm, L from 14 to 65 nm, $V_D(= V_G)$ from 1.0 to 1.2 V, and DIBL from 11 to 230 mV/V. In addition, we have also extracted l directly from the published channel potential profiles on the simulation double-gate devices [2], [3], [9], [11], [12]. The corresponding key parameters are the following: 1) $L = 10$ nm, $V_{\rm tho} \approx 0.33$ V, DIBL ≈ 140 mV/V, $V_D = 0.6$ V, $V_G = 0.6$ V, and $T = 300$ K [2]; 2) $L = 20$ nm, $V_{\rm tho} \approx 0.33$ V, DIBL ≈ 25 mV/V, $V_D = 0.2$ V, $V_G = 0.55$ V, and $T = 300$ K [3]; 3) $L = 25$ nm, $V_{\rm tho} \approx 0.3$ V, DIBL $\approx$ 100 mV/V, $V_D = 0.8$ V, $V_G = 0.5$, 0.8, and 1.0 V, and $T =$ 300 K [9]; 4) $L = 15$ nm, $V_{\rm tho} \approx 0.2$ V, DIBL ≈ 120 mV/V, $V_D = 0.7$ V, $V_G = 0.7$ V, and $T = 300$ K [11]; and 5) $L =$ 15 nm, $V_{\rm tho} \approx 0.3$ V, DIBL ≈ 77 mV/V, $V_D = 0.7$ V, $V_G =$ 0.7 V, and $T = 300$ K [12]. At this point, a scatter plot can be created, as shown in Fig. 3, in terms of the experimental and simulated l versus the quantity of the functional expression $LV_D^{0.25}(V_G - V_{\rm th})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Strikingly, all data are seen to fall on or around a straight line. The slope of the line furnishes η with a value of 4.1 $\rm V^{-0.25}$. As expected, η remains constant, regardless of the channel length, gate and drain voltage, and temperature.

Some remarks can now be made to clarify the confusing α values in the open literature [3]–[8]. First, it is noticed that in the case of bulk n-MOSFET, two different values of α were produced: one of 0.5 [4], [5] and one of 0.75 [6]. This difference can be attributed to the different subband treatments during the parameter extraction process. A Schrödinger–Poisson equation solving was utilized in [4] and [5], whereas in [6], this was done by a triangular potential approximation [13]. Therefore, the different subband levels can lead to different average thermal injection velocities, which in turn give rise to different l values. Second, based on (4), the temperature range of 233 K–298 K in case of a 55-nm bulk device [4], [5] is not large enough to affect the calculated $\widetilde{L}$. In other words, $\widetilde{L}$ is considerably

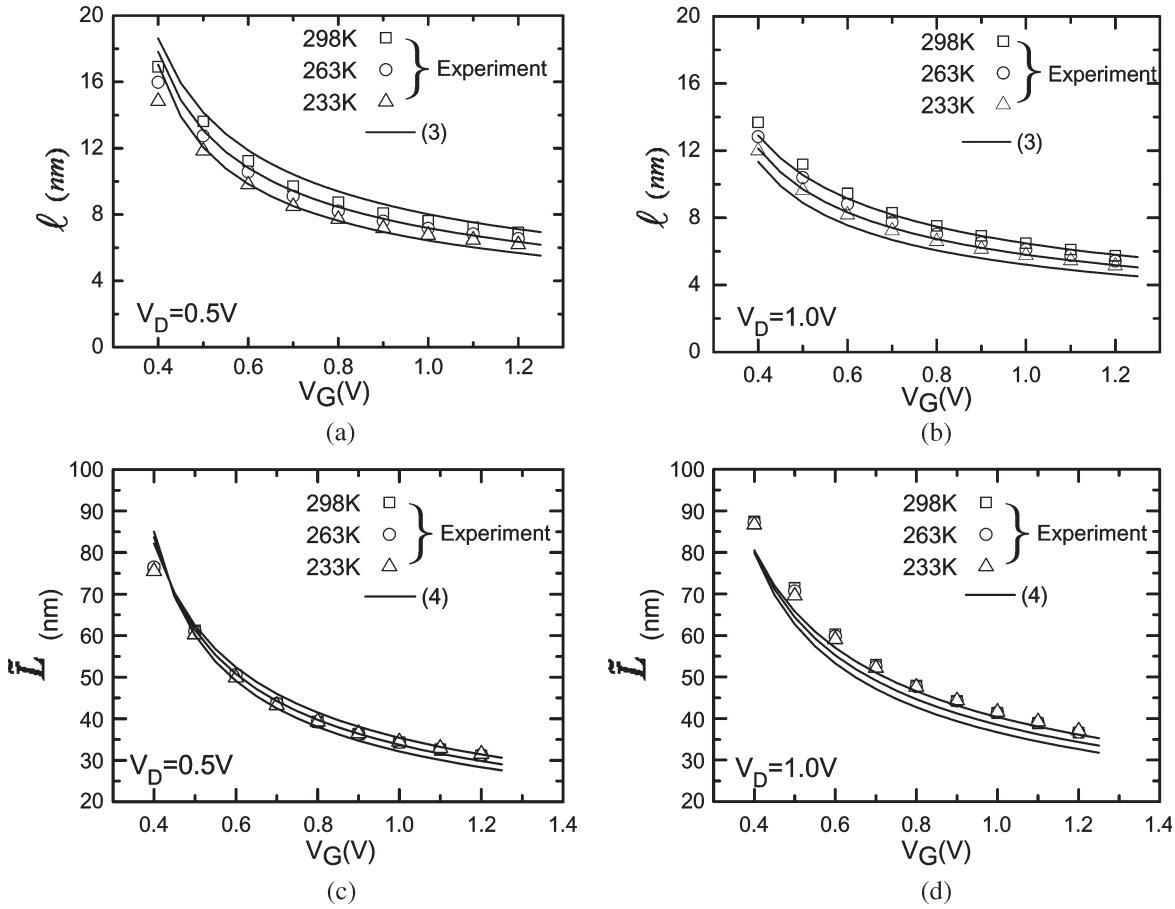

Fig. 2. Measured and calculated l versus gate voltage at two drain voltages of (a) 0.5 V and (b) 1.0 V for three temperatures and the corresponding $\widetilde{L}$ versus gate voltage for the drain voltages of (c) 0.5 V and (d) 1.0 V. The test device is a 55-nm bulk n-MOSFET. The calculation lines are from (3) and (4) with $\eta = 4.1\ \mathrm{V}^{-0.25}$.

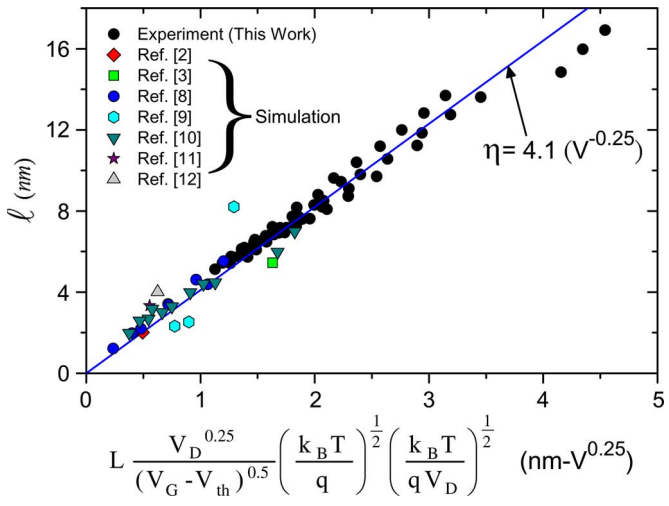

Fig. 3. Scatter plot of the experimental and simulated l versus the quantity of the functional expression $L(V_D^{0.25})(V_G - V_{\mathrm{th}})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Also shown is a straight line which fits the data points. The slope of the line yields η of 4.1 $\mathrm{V}^{-0.25}$.

insensitive to such a narrow temperature range. Consequently, the resulting apparent temperature power exponent was limited to 0.5, as reported in the previous work [4], [5]. Indeed, with the known η as input, fairly good reproduction can be achieved, as shown in Fig. 2, without adjusting any parameters. The same interpretations also apply to the $\alpha \approx 0.57$ case [3]. Only the room temperature of operation was involved, and therefore, the temperature effect of $\widetilde{L}$ can no longer be examined. In other words, only in a wide temperature range (as done in the comprehensive study of [8] and [10]) can the linear relationship of $l \propto T$, as shown in Fig. 3, be observed. Finally, from the aspect of temperature dependences or the excellent coincidence with a significant number of data, as shown in Fig. 3, the existing backscattering-coefficient extraction method [7] is valid.

IV. Conclusion

Based on a parabolic potential profile that is used to approximate the source-channel junction barrier of nanoscale MOSFETs, a new compact model of the k_BT layer's width has been physically derived along with the channel length, gate overdrive, drain voltage, and temperature as input. The validity of the parabolic potential barrier picture and the applicability of the resulting compact model have been justified by experimental data and by a critical analysis of various simulation works presented in the literature. In particular, the confusing temperature-dependent issues in the open literature have been satisfactorily clarified.

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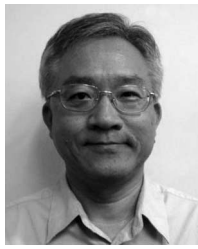

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Effect of uniaxial strain on anisotropic diffusion in silicon

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(Received 9 June 2006; accepted 30 August 2006; published online 17 October 2006)

A physical model is directly extended from the thermodynamic framework to deal with anisotropic diffusion in uniaxially stressed silicon. With the anisotropy of the uniaxial strain induced activation energy as input, two fundamental material parameters, the activation volume and the migration strain anisotropy, can be quantitatively determined. When applied to boron, a process-device coupled simulation is performed on a *p*-type metal-oxide-semiconductor field-effect transistor undergoing uniaxial stress in a manufacturing process. The resulting material parameters have been found to be in satisfactory agreement with values presented in the literature. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2362980]

Strain engineering has been widely recognized as an indispensable performance booster in producing next-generation metal-oxide-semiconductor field-effect transistors (MOSFETs).[1,2] There have been two fundamentally different methods used to achieve this goal:[1,2] (i) biaxially strained silicon on a relaxed SiGe buffer layer and (ii) uniaxially strained silicon through the use of trench isolation, silicide, and cap layers during the manufacturing process. However, diffusion in strained silicon is essentially different from that of unstrained silicon. Thus, an understanding of strain dependent diffusion, as well as its control, is a challenging issue. So far, there have been significant studies in this direction covering a wide range of experimental findings and confirmations,[3–9] atomistic calculations,[10–13] physical models,[10–16] and technology computer-aided design.[17] Specifically, Cowern *et al.*[5] experimentally revealed a linear dependence of the activation energy on strain. Within the thermodynamic framework constructed by Aziz *et al.* (see Ref. 18, which is more recent and more thorough than the earlier works cited above), the activation volume ($\tilde{V}$) and the anisotropy of the migration volume ($\tilde{V}^m_{\parallel}-\tilde{V}^m_{\perp}$) exist in nature. The combination of the activation energy, the activation volume, and the anisotropy of the migration volume is remarkable, as demonstrated in a physical model[14–16,18] dedicated to both the hydrostatic pressure experiment and the in-plane biaxial stress experiment,

$$\tilde{V}+\frac{3}{2}\frac{Q'_{33-\mathrm{biax}}}{Y_{\mathrm{biax}}}=\pm\Omega+(\tilde{V}^m_{\parallel}-\tilde{V}^m_{\perp}), \tag{1}$$

$$\tilde{V}+\frac{3}{2}\frac{Q'_{11-\mathrm{biax}}}{Y_{\mathrm{biax}}}=\pm\Omega-\frac{1}{2}(\tilde{V}^m_{\parallel}-\tilde{V}^m_{\perp}), \tag{2}$$

where $Q'_{33-\mathrm{biax}}$ is the biaxial strain induced activation energy in the direction normal to the silicon surface, Y_{biax} is the biaxial modulus, Ω is the lattice site volume, and $Q'_{11-\mathrm{biax}}$ is the biaxial strain induced activation energy in the direction parallel to the surface.

On the other hand, in the case of uniaxial stress as encountered while fabricating the MOSFET, without the use of a relaxed SiGe buffer layer, the stress is created through the trench isolation, silicide, or cap layers in a manufacturing process. Therefore, a straightforward extension to the uniaxial strain counterpart is essential. In this letter, one such model is derived and its linkage to the case of biaxial strain, Eqs. (1) and (2), is established. When applied to boron, a process-device coupled simulation is performed on a *p*-type MOSFET undergoing uniaxial stressing during the manufacturing process, followed by a systematic assessment of the fundamental material parameters.

According to Aziz[14] and Aziz *et al.*,[18] in the case of equilibrium or a quickly equilibrated point defect, the effect of stress on the dopant diffusivity in the direction normal to a (001) surface can be written as

$$\frac{D_{33}(\sigma)}{D_{33}(0)}=\exp\left(\frac{\sigma[V^f+\tilde{V}^m_{33}]}{k_BT}\right). \tag{3}$$

Here the product of the stress tensor σ and the formation strain tensor V^f is the work done against the stress field in defect formation, the product of the stress tensor σ and the migration strain tensor $\tilde{V}^m_{33}$ is the work required for the transition in the migration path, k_B is Boltzmann's constant, and T is the diffusion temperature. The tensor V^f involves the creation or annihilation of a lattice site, followed by a relaxation process,[14,18]

$$V^f=\pm\Omega\begin{bmatrix}0&&\\&0&\\&&1\end{bmatrix}+\frac{V^r}{3}\begin{bmatrix}1&&\\&1&\\&&1\end{bmatrix}. \tag{4}$$

The + sign denotes vacancy formation and the − sign represents interstitial formation. The relaxation volume propagates elastically to all surfaces, resulting in a change in the volume of the crystal by an amount V^r. $\tilde{V}^m_{33}$ is expected to have the form[14,18]

$$\tilde{V}^m_{33}=\begin{bmatrix}\tilde{V}^m_{\perp}&&\\&\tilde{V}^m_{\perp}&\\&&\tilde{V}^m_{\parallel}\end{bmatrix}. \tag{5}$$

In Eq. (5), $\tilde{V}^m_{\perp}$ and $\tilde{V}^m_{\parallel}$, respectively, reflect the dimension changes perpendicular and parallel to the direction of the net transport when the point defect reaches its saddle point.[14,18] Aziz further defined the activation volume as the sum of the

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three diagonal elements of the formation strain tensor and the migration strain tensor, as expressed by

$$\tilde{V} = \pm\Omega + V^r + 2\tilde{V}^m_{\perp} + \tilde{V}^m_{\parallel}. \tag{6}$$

It is well recognized[12] that when applying a uniaxial stress in a certain direction parallel to the silicon surface, the solid will modify its shape in order to minimize the energy of the system. In other words, the solid will deform in such a way that each surface perpendicular to the applied stress direction becomes stress-free. The underlying stress tensor therefore is

$$\sigma = \sigma_{\text{uniax}} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}. \tag{7}$$

On the basis of Hooke's law, σ_{uniax} in the linear elastic regime can be related to the uniaxial strain $\varepsilon_{\text{uniax}}$ induced in the same direction: $\sigma_{\text{uniax}} = Y_{\text{uniax}}\varepsilon_{\text{uniax}}$, where the uniaxial modulus $Y_{\text{uniax}} = (C_{11} - 2\nu C_{12})$ with Poisson's ratio $\nu = C_{12}/(C_{11} + C_{12})$. C_{11} and C_{12} are the elasticity constants. Analogous to previous work,[5] the uniaxial strain induced activation energy in the direction normal to the (001) surface, $Q'_{33-\text{uniax}}$, can be linked to the underlying diffusivity,

$$\frac{D_{33}(\varepsilon_{\text{uniax}})}{D_{33}(0)} = \exp\left(-\frac{Q'_{33-\text{uniax}}\varepsilon_{\text{uniax}}}{k_B T}\right). \tag{8}$$

By combining Eqs. (4), (5), and (7) and equalizing Eqs. (3)–(8), one obtains $Q'_{33-\text{uniax}}/Y_{\text{uniax}} = -V^r/3 - \tilde{V}^m_{\perp}$. Again, by incorporating Eq. (6), the following expression is produced:

$$\tilde{V} + 3\frac{Q'_{33-\text{uniax}}}{Y_{\text{uniax}}} = \pm\Omega + (\tilde{V}^m_{\parallel} - \tilde{V}^m_{\perp}). \tag{9}$$

It is then a straightforward task to derive the uniaxial strain induced activation energy $Q'_{11-\text{uniax}}$ in the applied stress direction: $Q'_{11-\text{uniax}}/Y_{\text{uniax}} = -V^r/3 - \tilde{V}^m_{\parallel}$. Consequently, a similar model is achieved,

$$\tilde{V} + 3\frac{Q'_{11-\text{uniax}}}{Y_{\text{uniax}}} = \pm\Omega - 2(\tilde{V}^m_{\parallel} - \tilde{V}^m_{\perp}). \tag{10}$$

Obviously, the uniaxial strain version is closely related to its biaxial counterpart: by comparing Eqs. (1) and (9), $Q'_{33-\text{uniax}} = (Y_{\text{uniax}}/2Y_{\text{biax}})Q'_{33-\text{biax}}$ is obtained. Another relation can then be readily derived: $Q'_{11-\text{uniax}} = -(Y_{\text{uniax}}/2Y_{\text{biax}})Q'_{33-\text{biax}} + (Y_{\text{uniax}}/Y_{\text{biax}})Q'_{11-\text{biax}}$.

To produce the experimental parameters in terms of the anisotropy of the uniaxial strain induced activation energy, a uniaxial stress experiment was carried out in terms of a *p*-channel MOSFET in a state-of-the-art manufacturing process.[17] The channel length was maintained at 65 nm while changing the spacing in the channel length direction between the two trench isolation sidewalls. The topside layout is detailed elsewhere.[17] Under such a situation, the channel zone encounters a compressive stress from the nearby trench isolation regions in the channel length direction. The devices used are quite wide (10 μm), meaning that the strain in the channel width direction is relatively negligible. The (001) silicon surface is supposed to be stress free. This hypothesis has been validated using the sophisticated simulations detailed in Ref. 17, which revealed that in the proximity of the silicon surface, the stress in the channel length direction is much larger in magnitude than that in the direction normal to the surface. Therefore, the proposed physical model can be adequately applied. The effect of changing the spacing between the two trench isolation regions in the channel length direction is reflected in the measured saturation threshold voltage, as displayed in Fig. 1. The negative shift in the saturation threshold voltage with increasing stress (via decreasing spacing between the trench isolation regions) shown in Fig. 1 can be attributed to the retarded boron diffusion.

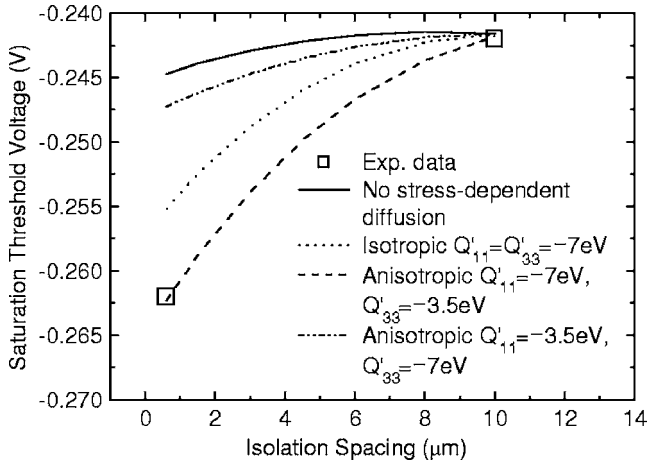

FIG. 1. Measured *p*-MOSFET saturation threshold voltage vs the spacing between the nearby trench isolation sidewalls in the channel length direction. Also shown are those (lines) from the process-device coupled simulation with and without the strain induced activation energies. The reason that the "no stress-dependent diffusion curve" is not entirely horizontal is due to dopant segregation near the edges of the source/drain regions. Specifically, the nonuniformity is caused by boron segregation occurring close to trench isolation oxide during the thermal process. Although the affected profile is not in vicinity of the MOSFET core region, a minor threshold voltage difference (~3 mV) between large and small active areas can still be observed, even without the stress-dependent diffusion model.

A two-dimensional process-device coupled simulation, as detailed in Ref. 17, was slightly modified by taking the anisotropy of the boron diffusivity into account,

$$\frac{D_{33}(\varepsilon_t)}{D_{33}(0)} = \exp\left(-\frac{Q'_{33-\text{TCAD}}\varepsilon_t}{k_B T}\right), \tag{11}$$

$$\frac{D_{11}(\varepsilon_t)}{D_{11}(0)} = \exp\left(-\frac{Q'_{11-\text{TCAD}}\varepsilon_t}{k_B T}\right). \tag{12}$$

According to the work in Ref. 17 the total strain ε_t is the sum of the three strain components: ε_{xx} in the channel length direction, ε_{yy} in the channel width direction, and ε_{zz} in the direction normal to the silicon surface. From the simulated strain distributions, $\varepsilon_t \sim \varepsilon_{xx}$, leading to $Q'_{33-\text{TCAD}} \approx Q'_{33-\text{uniax}}$ and $Q'_{11-\text{TCAD}} \approx Q'_{11-\text{uniax}}$. The simulated saturation threshold voltages for different values of $Q'_{33-\text{uniax}}$ and $Q'_{11-\text{uniax}}$ are plotted in Fig. 1 for comparison. The figure clearly exhibits that (i) the largest deviation occurs at $Q'_{33-\text{uniax}} = 0$ and $Q'_{11-\text{uniax}} = 0$, the case of no stress dependencies; (ii) the most accurate reproduction is achieved with the anisotropic activation energies, rather than the isotropic variety; and (iii) the anisotropy of the activation energy must be adequate, that is, $Q'_{11-\text{uniax}} = -7$ eV per unit strain and $Q'_{33-\text{uniax}} = -3.5$ eV per unit strain are more favorable than $Q'_{11-\text{uniax}} = -3.5$ eV per unit strain and $Q'_{33-\text{uniax}} = -7$ eV per unit strain.

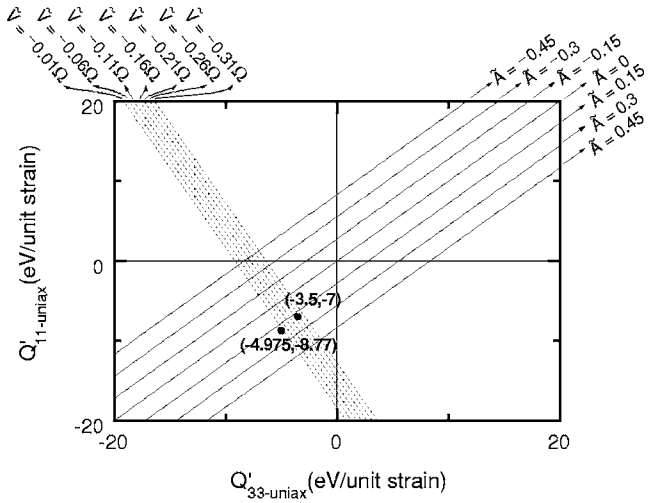

FIG. 2. Uniaxial strain induced activation energy in the applied stress direction (parallel to the silicon surface) vs that normal to the silicon surface. The lines are from Eqs. (9) and (10) for a literature range (Refs. 15, 16, and 18) of the activation volume and the migration strain anisotropy. Also plotted are the data points from the underlying experiment and the existing *ab initio* calculations (Refs. 12 and 13).

Prior to determining the fundamental material parameters, a systematic treatment, such as that indicated in Fig. 2, is demanded. In Fig. 2 a series of straight lines of $Q'_{11-\text{uniax}}$ vs $Q'_{33-\text{uniax}}$ are from Eqs. (9) and (10) for a literature range[15,16,18] of $\tilde{V}$ and the migration strain anisotropy $\tilde{A}$ $(\equiv(\tilde{V}^m_{\parallel}-\tilde{V}^m_{\perp})/\Omega)$.[18] In the calculation procedure, the following literature values were employed:[19] (i) $C_{11}=168$ GPa and $C_{12}=65$ GPa, giving rise to $Y_{\text{uniax}}=131$ GPa and $\nu=0.28$; (ii) $\Omega=2.26\times10^{-23}$ cm^3. The above experimental parameters are also added to the figure. From the figure a set of $\tilde{V}$ and $\tilde{A}$ can be clearly located around the data point. On the other hand, uncertainties exist based on a series of literature data: $\tilde{V}=-0.16\pm0.05$ Ω.[18] Taking such uncertainties into account, Fig. 2 reveals that the data point does match the upper limit, that is, $\tilde{V}=-0.21$ Ω. The corresponding $\tilde{V}^m_{\parallel}-\tilde{V}^m_{\perp}$ in the vicinity of 0.15 Ω is determined accordingly, falling within the reasonable range.[15,16,18] Such corroborating experimental evidence further indicates that the transient enhanced diffusion effect is relatively insignificant when compared to the long-term diffusion times in the underlying manufacturing process. Under such circumstances, the point defect is rapidly equilibrated relative to the entire diffusion time.

Finally, we quoted the existing *ab initio* calculations:[12,13] $Q'_{11-\text{biax}}=-19.2$ eV per unit strain and $Q'_{33-\text{biax}}=-13.9$ eV per unit strain, which were transformed via the aforementioned relationship into the equivalent $Q'_{11-\text{uniax}}$ of −8.77 eV per unit strain and $Q'_{33-\text{uniax}}$ of −4.975 eV per unit strain. In this process, the Y_{biax} used was equal to 183 GPa according to $Y_{\text{biax}}=(C_{11}+C_{12}-\nu C_{12})$ with its Poisson's ratio $\nu=2C_{12}/C_{11}$. Evidently, the two data points are quite comparable to each other, as displayed in Fig. 2.

A physical model dealing with anisotropic diffusion in uniaxially stressed silicon is derived and is quantitatively connected to the biaxial case. A process-device coupled simulation is performed on a *p*-type MOSFET undergoing uniaxial stress during the manufacturing process. A systematic treatment is conducted and the resulting fundamental material parameters are in satisfactory agreement with literature values.

This research is supported by the National Science Council of Taiwan under Contract No. NSC94-2215-E-009-005.

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On the Mean Free Path for Backscattering in k_BT Layer of Bulk Nano-MOSFETs

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***Abstract*—We perform Monte Carlo particle simulations on a silicon conductor for the purposes of reexamining the channel backscattering in *bulk* nano-MOSFETs. The resulting mean free path λ_o for backscattering in a *long* and near-equilibrium conductor is constant, regardless of the potential profile. However, the *apparent* mean free path λ_1 in a local quasi-ballistic k_BT layer depends on the curvature of the potential profile. In a linear potential profile, the λ_1 extracted in a wide range of the conductor length (15 to 100 nm) and lattice temperature (150 to 300 K) is found to fall below λ_o. The carrier heating as the origin of reduced mean free path is inferred from the simulated carrier velocity distribution near the injection point. Strikingly, the mean free paths in a parabolic potential profile remain consistent: $\lambda_1 = \lambda_o$. This indicates the absence or weakening of the carrier heating in the layer of interest, valid only for the parabolic potential barrier.**

***Index Terms*—Backscattering, MOSFET, nanoscale.**

I. Introduction

THE understanding of the electrical properties of a near-equilibrium bulk conductor can be made clear from the backscattering point of view [1]. The backscattering events in the conductor have been systematically treated, leading to a functional expression for r_c, the well-known backscattering coefficient at the injection point

$$r_c = \frac{L}{L + \lambda_o}. \tag{1}$$

Here, L is the length of the conductor, and λ_o is the equilibrium mean free path for backscattering. Once r_c is known, the total resistance of the conductor can be determined accordingly. Note that, in the case of quasi-ballistic transport (i.e., $\lambda_o > L$), (1) remains valid [1]. Essentially, (1) can apply to the channel backscattering in MOSFETs under near-equilibrium conditions [2]. Extension to the saturation regime of operation can be done by simply replacing the conductor's length L in (1) with the width designated l of a localized *quasi-equilibrium* zone near the source, namely, k_BT layer [2], [3]. The resulting expression reads as [2], [3]

$$r_c = \frac{l}{l + \lambda_o}. \tag{2}$$

Manuscript received July 18, 2008. This work was supported by the National Science Council of Taiwan under Contract NSC 95-2221-E-009-285. The review of this brief was arranged by Editor C. McAndrew.

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Digital Object Identifier 10.1109/TED.2008.2006532

Within the context of the channel backscattering [2], [3], λ_o is the only mean free path for all operating conditions. More recently, however, sophisticated Monte Carlo simulation studies [4]–[7] have pointed to the significance of the carrier heating in k_BT layer or, in general, the nonequilibrium transport over the channel. In a sense, the carrier heating factor has been incorporated [7] by replacing λ_o in (2) with the *apparent* mean free path λ_1, thus constituting a new expression

$$r_c = \frac{l}{l + \lambda_1}. \tag{3}$$

In particular, in case of nondegenerate statistics, the Monte Carlo simulations at room temperature on a *linear* channel potential profile have exhibited a certain relationship (see [7, Fig. 4]): $\lambda_1 = \lambda_o/\gamma$ with $\gamma = 1.5$ to 2.0, different at all from that ($\lambda_1 = \lambda_o$) in the literature [2], [3]. Thus, some clarifications are demanded.

To achieve the goal, in this brief, the Monte Carlo particle simulations are performed on a silicon bulk conductor for different conductor lengths, lattice temperatures, and potential profiles. Then, the *apparent* mean free path for backscattering in the k_BT layer is extracted and compared with the equilibrium ones of a long conductor. The results can adequately apply to the channel backscattering in *bulk* nano-MOSFETs. The reasons are that the underlying carrier degeneracy is quite weak, as reflected by an existing low value (=1.13 for a 1-V gate voltage, as cited in [8, Fig. 4]) of the Fermi–Dirac to Maxwellian injection velocity ratio. In addition, this argument holds as compared with the ultrathin film counterparts, where the carrier degeneracy is pronounced due to the *space* confinement effect. The potential profile under study is not self-consistent but *frozen*, as frequently adopted elsewhere [7], [9], [10], which allows a *direct* examination of the mean-free-path issue.

II. Monte Carlo Simulation

A Monte Carlo particle simulation program dedicated to the solving of the complicated scattering events (i.e., acoustic phonon scattering, optical phonon scattering, and ionized impurity scattering) in a silicon bulk conductor has been developed elsewhere [11]. This program named SDemon (currently merged into a new one called DEMONs [11]) can provide the rich information concerning the carrier positively and negatively directed velocity distributions in the transport direction. The boundary conditions used are as follows: 1) At the origin $x = 0$, the hemi-Maxwellian carriers are injected while, in

the steady state, absorbing the backscattered carriers without further reflections; and 2) at the end of the conductor ($x = L$), the positively directed carriers are absorbed without any ones injected. At the injection point $x = 0$, the ratio of the negatively directed flux to the positively directed flux yields the backscattering coefficient r_c. In the previous work [12] on 80-nm silicon conductor of 10^{12} cm^{-3} doping with a linear potential profile, the simulation program SDemon has been validated in terms of the extracted mobility versus temperature that has been found to be comparable with the published silicon mobility data [13]. The same simulation works are executed here but with the following significant augmentations: a parabolic potential profile added; four different conductor lengths of 15, 25, 50, and 100 nm; and three different lattice temperatures of 150, 200, and 300 K. According to the backscattering framework [2], [3], l can be explicitly expressed as a function of the conductor length L, the thermal energy k_BT, and the applied voltage V_a : $l = Lk_BT/qV_a$ for the linear potential profile and $L\sqrt{k_BT/qV_a}$ for the parabolic one.

III. Results and Comparisons

On the longest conductor ($L = 100$ nm), the outcome of the simulation over 10^{-5} V $\leq V_a \leq 10^{-3}$ V furnishes the quantities of the near-equilibrium r_c. Indeed, the r_c of a linear potential profile is found to be close to that of the parabolic one, as expected. The corresponding λ_o is 56, 105, and 155 nm for 300, 200, and 150 K, respectively. Moreover, the extracted value of λ_o at room temperature is identical to that of the previous work [12].

Unlike its near-equilibrium counterparts, the curvature of the potential profile for $V_a \gg k_BT/q$ can play a relevant role in determining r_c. First of all, in a linear potential profile, the simulated r_c is shown in Fig. 1 for different temperatures versus applied voltage with the conductor length as a parameter. Also shown in the figure are the calculated results from (4) with known λ_o as input [9]

$$r_c = \frac{1 - \exp\left(-\frac{L}{l}\right)}{1 + \eta\frac{\lambda_0}{l} - \exp\left(-\frac{L}{l}\right)} \tag{4}$$

where η is the potential profile dependent coefficient and equals unity in the linear potential profile. The primary reasons of using (4) rather than directly (2) are that it can adequately produce r_c in the proximity of zero applied voltage while exactly reducing to (2) for $V_a \gg k_BT/q$ or equivalently $L \gg l$ (see [9] for details). It can be seen that significant deviations are created with respect to the calculation results. In particular, this error increases with increasing applied voltage or decreasing conductor length. It is noteworthy that the lattice temperature does not significantly affect such trends. Indeed, the discrepancies in Fig. 1 can provide the opportunity to examine the mean-free-path issue. By substituting the simulated r_c into the following [9]:

$$r_c = \frac{1 - \exp\left(-\frac{L}{l}\right)}{1 + \eta\frac{\lambda_1}{l} - \exp\left(-\frac{L}{l}\right)} \tag{5}$$

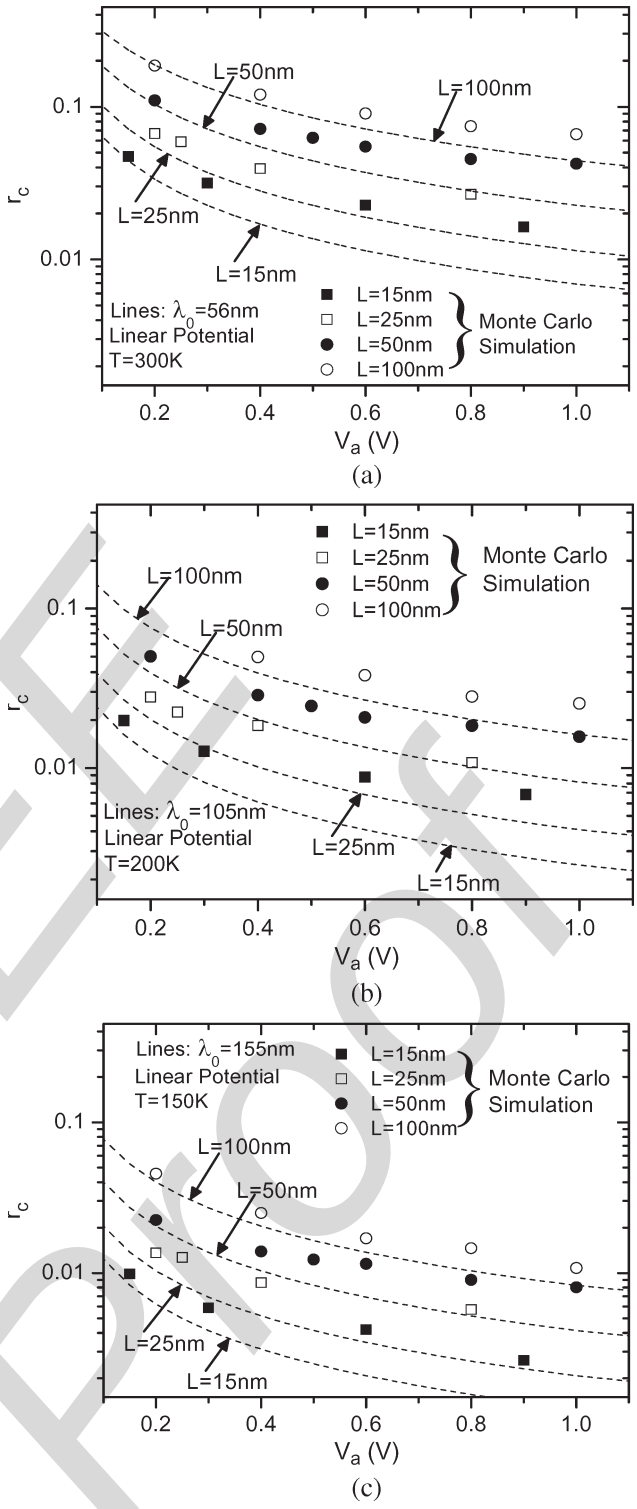

Fig. 1. (Symbols) Simulated r_c in a linear potential profile for four conductor lengths versus applied voltage for (a) 300 K, (b) 200 K, and (c) 150 K. Also shown for comparison are (lines) the calculated results from (4) with $\eta = 1$.

the underlying λ_1 can be extracted, as shown in Fig. 2 versus the applied voltage. It can be seen that 1) λ_1 falls below λ_o; particularly at 1-V applied voltage, one can draw a specific relation of $\lambda_1 = \lambda_o/\gamma$ with $\gamma = 1.5$ to 2.5; 2) on average, λ_1 decreases with decreasing conductor length; and 3) again on average, λ_1 decreases with the applied voltage. It is therefore

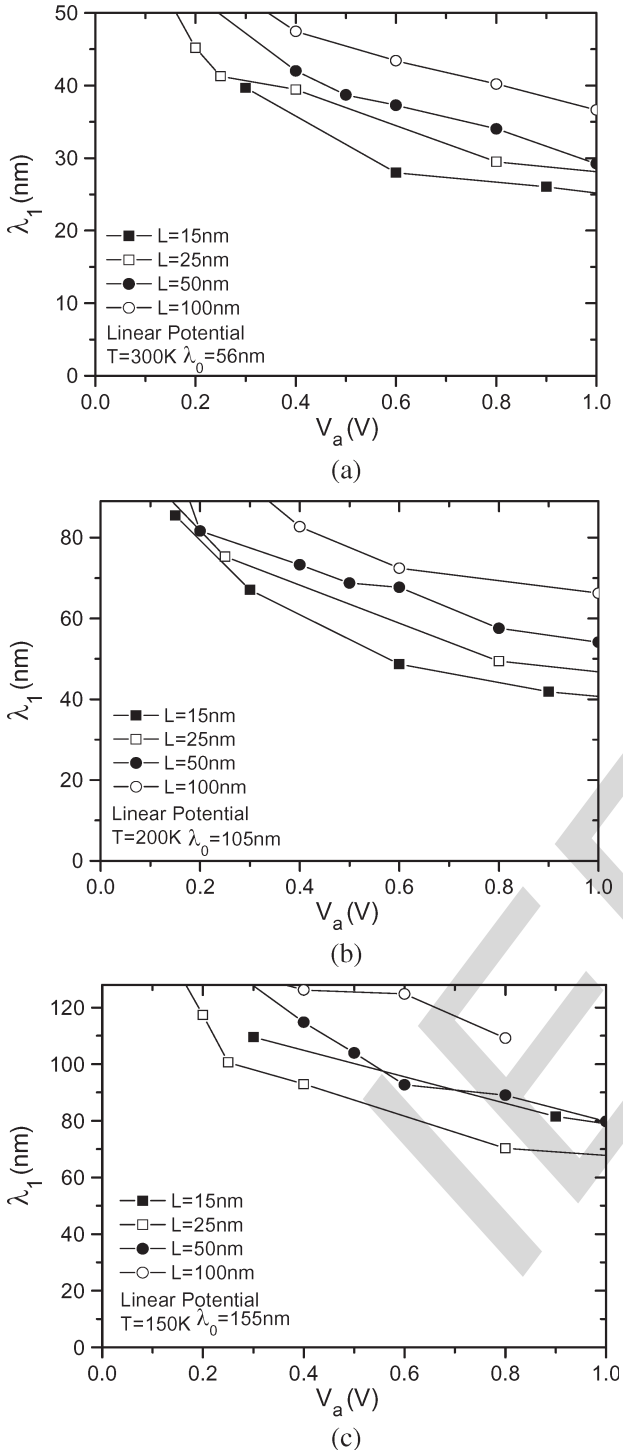

Fig. 2. Extracted *apparent* mean free path λ_1 via (5) with $\eta = 1$ corresponding to the data points in Fig. 1 for (a) 300 K, (b) 200 K, and (c) 150 K.

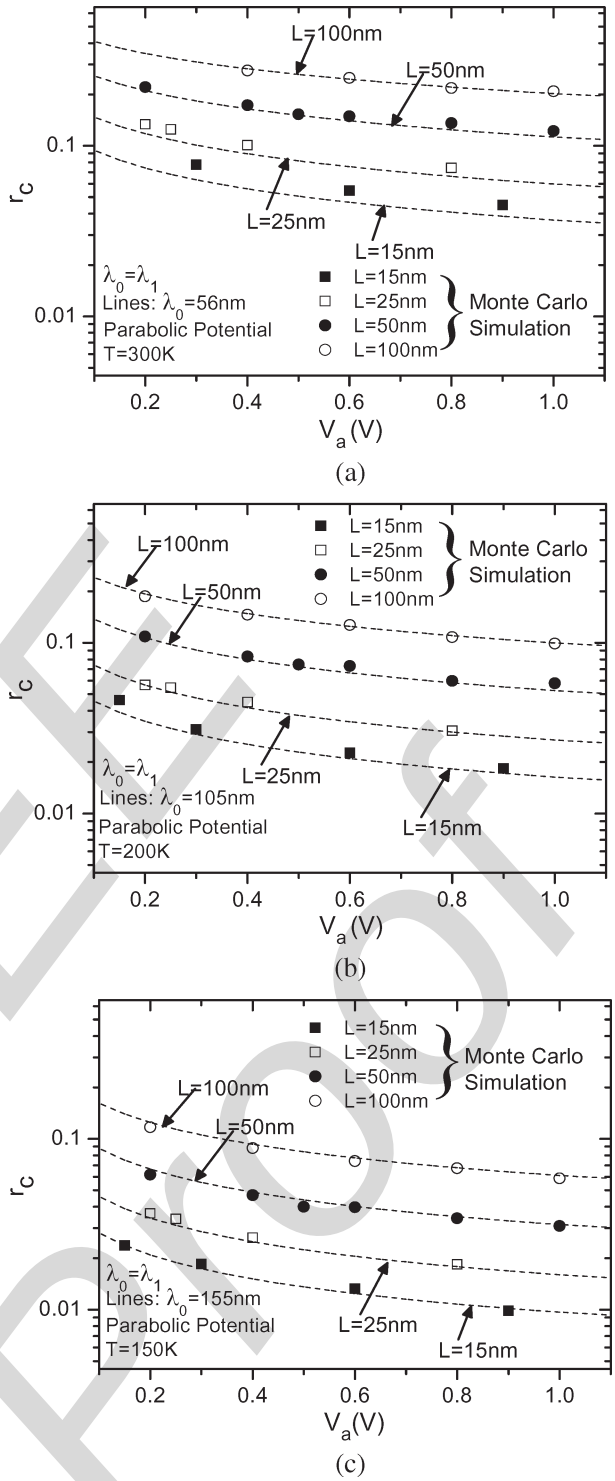

Fig. 3. Comparison of the (symbols) simulated and (lines) calculated r_c's for four conductor lengths in a parabolic potential profile versus applied voltage for (a) 300 K, (b) 200 K, and (c) 150 K. The calculations are from (5) with $\eta = 2/\sqrt{\pi}$ [9] and $\lambda_1 = \lambda_o$.

inferred that only with increasing conductor length or decreasing applied voltage can the upper limit of λ_o be recovered. Once again, the ratio of λ_1 to λ_o appears to be a weak function of the lattice temperature. Note that the recent Monte Carlo simulations [7], devoted to a linear potential profile at 300 K, have produced similar results, as mentioned earlier.

For the parabolic potential profile, the corresponding simulation results are shown in Fig. 3. Also shown are the calculated lines from (5) with $\eta = 2/\sqrt{\pi}$ (see [9, Eq. (37)]) and $\lambda_1 = \lambda_o$ = 56, 105, and 155 nm for 300, 200, and 150 K, respectively. We found that good reproduction of data points for different conductor lengths, temperatures, and applied voltages can all be achieved with simply $\lambda_1 = \lambda_o$, without adjusting any parameters. This means that, despite the quasi-ballistic transport

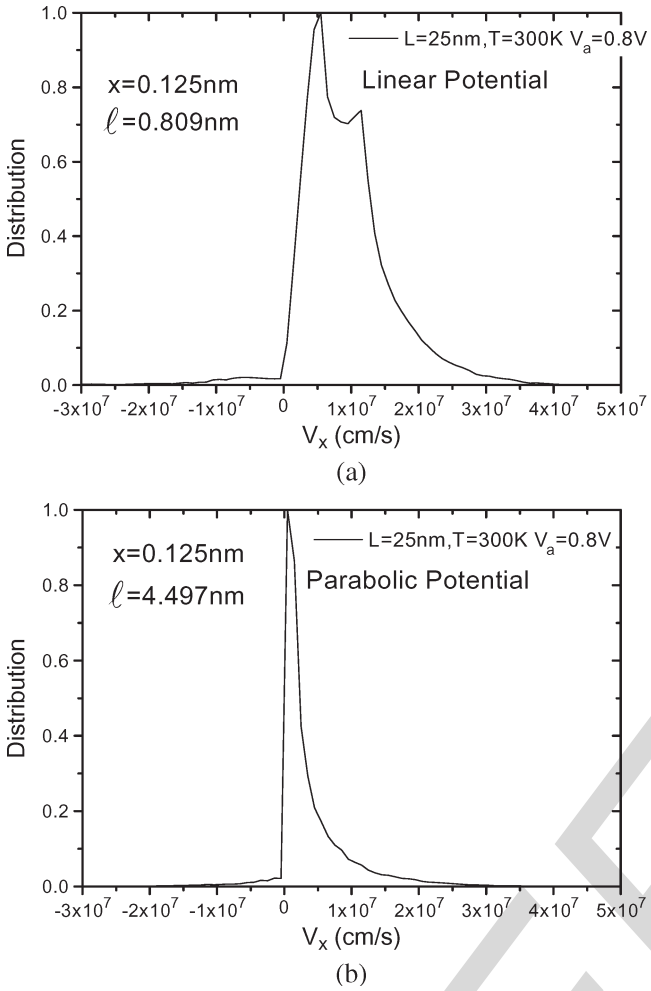

Fig. 4. Simulated carrier velocity component distribution in the transport direction at $x = 0.125$ nm for (a) a linear potential profile and (b) a parabolic potential profile. $L = 25$ nm, $T = 300$ K, and $V_a = 0.8$ V.

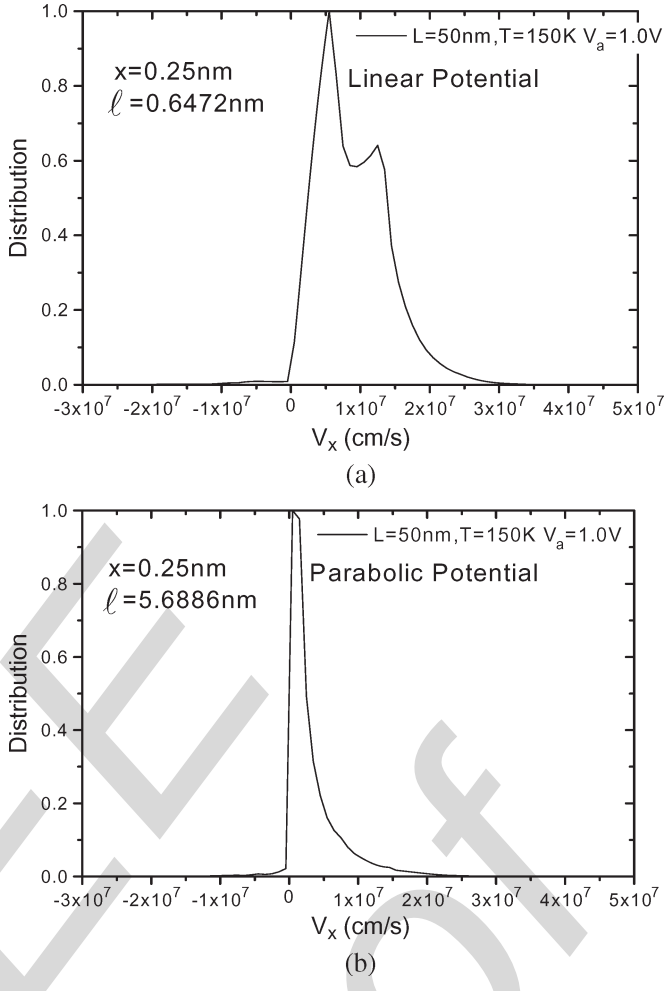

Fig. 5. Simulated carrier velocity component distribution in the transport direction at $x = 0.25$ nm for (a) a linear potential profile and (b) a parabolic potential profile. $L = 50$ nm, $T = 150$ K, and $V_a = 1.0$ V.

prevailing in the k_BT layer ($\lambda_1 > l$), the quasi-equilibrium conditions still govern the backscattered carriers.

IV. Evidence for Carrier Heating

Here, we demonstrate that the different mean free paths between the parabolic and linear potential profiles can be traced to the curvature of the potential profile, particularly the presence or absence of a zero or weak field regime near the injection point. For a parabolic potential profile, there is a significant fraction of the k_BT layer, which can be identified as the zero-field regime. With this in mind, although the deviations from the lattice temperature would be possible as entering into the remainder (i.e., out of the zero-field regime), the overall carrier heating in the k_BT layer should be weakened. For a linear potential profile, however, such a zero-field regime is lacking. Therefore, once injected at the beginning of the k_BT layer, the carriers immediately undergo acceleration from the nonzero field. Owing to the quasi-ballistic transport (less collision), the carrier temperature is expected to be higher than the lattice temperature, and the mean free path is therefore no longer independent of the carrier energy. The confirmative evidence is presented in terms of the carrier velocity component v_x distribution in the transport direction near the injection point, as shown in Figs. 4 and 5 for $L = 25$ nm at $V_a = 0.8$ V and 300 K and $L = 50$ nm at $V_a = 1.0$ V and 150 K, respectively. They are all created by the program DEMONs. These figures clearly reveal two significant differences between the potential profiles. First, in a parabolic potential profile, a single hemi-Maxwellian distribution is retained in the positively directed carriers but is split into two distinct components in the linear potential case: One of the longitudinal effective masses and one of the transverse effective masses. This strongly points to the effect of the nonzero field in the linear potential profile. Second, the distribution of the negatively directed or backscattered carriers appears to be wider in a linear potential profile than the parabolic one.

V. Conclusion

The Monte Carlo simulations have been extensively carried out on a silicon bulk conductor aimed at reexamining the channel backscattering in bulk nano-MOSFETs. The main results achieved in this brief can be summarized as follows.

1) The near-equilibrium mean free path for backscattering λ_o is independent of the potential profile.

2) The apparent mean free path λ_1 in a localized quasi-ballistic k_BT layer can be linked with the curvature of the potential profile.
3) The λ_1 in a linear potential profile is lower than λ_o due to the presence of the carrier heating, as highlighted by the carrier velocity distribution near the injection point.
4) In a parabolic potential profile, the mean free paths remain consistent: $\lambda_1 = \lambda_o$. This means that, despite the quasi-ballistic transport prevailing in the k_BT layer ($\lambda_1 > l$), the quasi-equilibrium conditions still govern the backscattered carriers.

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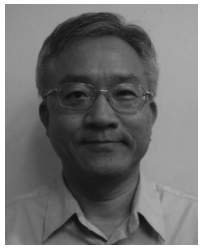

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NanoFETs Channel Backscattering: Recent Research Trends and Challenging Issues

(Invited Paper)

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Abstract --- *The flux aspect in terms of the channel backscattering has emerged as a promising tool to examine the transport phenomena and performance limits in nanoFETs, both theoretically and experimentally. In this paper, the historical overview of the channel backscattering framework is given. Then, the recent studies in this direction are highlighted, followed by several challenging issues. It is further suggested that the device researchers worldwide collaborate together in an effort to improve the device physics in the context of the channel backscattering. The ultimate aim is to render the channel backscattering framework practically suitable for the nanoFET structures, both 1-D and 2-D, with the feature size down to 10 nm and beyond.*

Keywords*:* Nano, MOSFETs, Transport, Scattering

I. Introduction

The conventional device physics knowledge as drawn from a well-known drift/diffusion picture has recently encountered the difficulty in elucidating nanoFETs transport, especially in the saturation regime of operation. To overcome this obstacle, the flux aspect of channel backscattering has been alternatively introduced [1],[2]. The main merits of this new picture are that (i) it can provide a clear understanding of the underlying device physics, on the basis of a small fraction of the channel near the quasi-equilibrium source, rather than the traditional high-field one near the drain; (ii) it can meet the computationally efficient requirements; and (iii) it can furnish information about how close to the thermal limit the device performance can achieve.

In this paper, the historical overview of the channel backscattering framework is presented. Then, the recent research trends are highlighted. The challenging issues are subsequently addressed. Finally, several key directions are suggested for the years ahead. The ultimate aim is to make the channel backscattering practically suitable for the next generation of device physics, valid for 1-D and 2-D nanoFETs down to 10-nm feature size and beyond.

II. Channel Backscattering: Historical Overview (Maxwellian-Boltzmann Statistics)

Understanding of the electrical properties of a near-equilibrium bulk conductor can be made clear from the backscattering point of view [3]. The backscattering events in the conductor have been systematically treated by Datta [3], leading to a functional expression for r_c, the well-known backscattering coefficient at the injection point:

$$r_c = \frac{L}{L + \lambda_o}. \tag{1}$$

Here L is the length of the conductor and λ_o is the equilibrium mean-free-path for backscattering. Once r_c is known, the total conductance can be determined accordingly. Even in the case of quasi-ballistic transport (i.e., $\lambda_o > L$), (1) remains valid [3]. Essentially, Eq. (1) can apply to the channel backscattering in MOSFETs under near-equilibrium conditions [1],[2]. In Lundstrom's view [1] (see Fig. 1), extension to the saturation regime of operation can be done by simply replacing the conductor's length L in (1) with the width designated l of a localized *quasi-equilibrium* zone near the source, over which the potential drops by k_BT/q. The resulting expression reads as

$$r_c = \frac{l}{l + \lambda_o} \quad . \tag{2}$$

Within the context of the channel backscattering [1],[2], λ_o is the only mean-free-path for all operating conditions. One of the merits of the channel backscattering picture is that it is concentrated solely on a local zone near the quasi-equilibrium source, rather than conventionally the high-field region near the drain where the carrier heating and scattering are extremely difficult to analyze. Once r_c is known, then the saturation and linear drain current *per unit width* can be calculated [1],[2]:

$$I_{Dsat} = Q_{inv} v_{inj} \frac{1 - r_c}{1 + r_c} \tag{3a}$$

$$I_{Dlin} = Q_{inv} v_{inj} \frac{1 - r_c}{2k_BT/q} V_D \tag{3b}$$

where Q_{inv} is the inversion layer charge per unit area and v_{inj} is the positively-directed average thermal injection velocity, both defined at the peak of the source-channel barrier or the virtual source. Q_{inv} appropriately follows the MOS electrostatics: $Q_{inv} = C_{eff}(V_G - V_{th})$, where C_{eff} is the inversion gate

capacitance per unit area and V_{th} is the threshold voltage. The effect of the external series resistance R_{SD} is implicitly included in (3).

Years later, Clerc, et al. [4] have physically derived an analytic model along with the hypothesis that the backscattered flux is Maxwellian and that the mean-free-path for backscattering does not depend on the carrier energy. The resulting model reads as [4]:

$$r_c = \frac{1-\exp(-\frac{L}{l})}{1+\xi\frac{\lambda_0}{l}-\exp(-\frac{L}{l})} \qquad (4)$$

where ξ is the potential profile dependent coefficient and equals unity in the linear potential profile. Eq.(4) can adequately produce r_c in the proximity of zero drain voltage while exactly reducing to (2) for $V_D >> k_BT/q$ or equivalently $L >> l$. This also is the case for $V_D << k_BT/q$ or equivalently $L << l$, under which (4) reduces to (1).

III. Recent Studies and Trends -I

A. *Temperature Dependent r_C Extraction* [5]

Differentiating above equation (3a) with respect to the reference temperature T_o produces an analytic expression for the ratio of the mean-free-path λ_o to the critical length l at T_o:

$$\frac{\lambda_o(T_o)}{l(T_o)} = \frac{-2(1+\beta_\mu-\beta_{vinj}-\beta_l)}{\beta_{vinj}-(\alpha_{ID}+\rho_Q)T_o} - 2 \qquad (5)$$

The relationship of $\lambda_o = 2\mu k_BT/qv_{inj}$ [1],[2] was applied in deriving (5). Here α_{ID} represents the normalized drain current change percentage ($=\partial I_D/(I_D\partial T)$ with respect to I_D at T_o; and ρ_Q is the normalized inversion layer charge change ($= -\partial Q_{inv}/(Q_{inv}\partial T)$ *or* $-\partial(V_G\text{-}V_{th})/((V_G\text{-}V_{th})\partial T)$). Here the threshold voltage V_{th} is the near-equilibrium threshold voltage V_{tho} minus the product of the *DIBL* and drain voltage: $V_{th} = V_{tho} - DIBL\times V_D$. To take into account the external series resistance R_{SD}, above V_G and V_D terms ought to be replaced with $V_G - I_DR_{SD}/2$ and $V_D - I_DR_{SD}$, respectively. Meanwhile, the following power law relations are adopted: the injection thermal velocity $v_{inj} \propto T^{\beta vinj}$; the near-equilibrium mobility $\mu \propto T^{\beta\mu}$; and the critical length $l \propto T^{\beta l}$. Some values were suggested when this temperature method was introduced [5]: β_{vinj} (= 0.5) as drawn from the non-degeneracy statistics; β_l = 1 from the k_BT layer concept; and β_μ = -1.5, one of the typical values cited in the device physics textbook.

Once λ_o/l is obtained via (5), then its values for other temperatures can be determined according to above power law relationships:

$$\frac{\lambda_o(T)}{l(T)} = \frac{\lambda_o(T_o)}{l(T_o)}\left(\frac{T}{T_o}\right)^{1+\beta_\mu-\beta_{vinj}-\beta_l} \qquad (6)$$

Furthermore, the corresponding backscattering coefficient r_c and hence the drain current can be readily calculated (see Fig. 2 to 4).

B. *Strain Engineering*

With the aid of the temperature dependent method, Lin, et al. [6] have examined the influence of uniaxial strain on the channel backscattering coefficient in nanoscale MOSFETs. The resulting channel backscattering coefficients are shown to be reduced in tensile stress nMOSFET but increased in compressive stress pMOSFET. Meanwhile, the carrier injection velocity is increased in both cases. Drive current is hence determined not only by backscattering coefficient but also by the injection velocity. Strain techniques and/or device structures with simultaneous enhancement of channel backscattering coefficient and injection velocity are therefore favorable for ultimate performance improvement [6].

Interestingly, Liow, et al. [7] have reported, on sub-30-nm FinFETs with $Si_{0.99}C_{0.01}$ source/drain regions, a carrier backscattering study of the devices. The resulting carrier transport characteristics in terms of the ballistic fraction and carrier source injection velocity have shown consistency with observed I_{Dsat} enhancement.

C. *Self-Heating*

Electro-thermal coupling and device design are expected to become more important with continued scaling [8]. Self-heating is sensitive to several device parameters. Specifically, the thermal conductivity of bulk germanium is only 40 percentage as large as that of silicon, which combined with the poor thermal conductivity of the buried oxide may lead to worse thermal problems for GOI (germanium-on-insulator) than those already well documented for SOI (silicon-on-insulator). Thus, it is crucial to examine and compare the electro-thermal behaviors of GOI and SOI devices near the limits of scaling. To achieve this goal, Pop, et al. [8] have developed a self-consistent electro-thermal compact model, on the basis of the aforementioned temperature dependent power law relationships, for calculating device temperature, saturation current and intrinsic gate delay. In turn, the device source/drain has been designed to help simultaneously minimize device temperature and parasitic capacitance. This comprehensive analysis has led to the conclusion that optimized GOI devices could provide at least 30 percent performance advantages over similar SOI devices in the presence of the self-heating [8].

IV. Recent Studies and Trends -II

A. *On the Temperature Dependent Method*

Chen, et al. [9] have performed a systematical study on a 68-nm gate length nMOSFET (see Fig. 5 to 12), without accounting for the temperature

dependent r_c extraction method, to experimentally assess the power exponents of concern. The results are that for V_G increasing from 0.3 V to 1.2 V, β_l decreases from 1.0 to 0.75, β_{vinj} from 0.45 to 0.25, and β_μ from 0.45 to around -1.5. The corresponding inversion charge coefficient ρ_Q is about $0.4\times10^{-3}/^oK$. Evidently, the initially introduced power exponents are fairly reasonable [5].

However, serious questions on the precision of the temperature dependent r_c extraction method have recently arisen. By means of sophisticated Monte Carlo simulations on the double-gate MOSFETs, Zilli, et al. [10] have exhibited the influence of the inversion charge coefficient ρ_Q on the precision of the temperature method. The plausible origins are the uncertainties encountered in estimating the inversion charge coefficient ρ_Q. However, the experimental values of ρ_Q of about $0.4\times10^{-3}/^oK$ in [5],[9] is less than those ($\sim10^{-3}/^oK$) of the Monte Carlo simulations [10]. Nevertheless, further study is needed to resolve this contradicting issue.

B. On the Functional Expression of $\lambda_o = 2\mu k_BT/qv_{inj}$

A Monte Carlo particle simulation program dedicated to the solving of the complicated scattering events (i.e., acoustic phonon scattering, optical phonon scattering, and ionized impurity scattering) in a silicon bulk conductor has been developed elsewhere [11]. This program named SDemon (currently merged into a new one called DEMONs [11]) can provide the rich information concerning the carrier positively-directed and negatively-directed velocity distributions in the transport direction. The boundary conditions used are that (i) at the origin x = 0, the hemi-Maxwellian carriers are injected while, in the steady state, absorbing the backscattered carriers without further reflections; and (ii) at the end of the conductor ($x = L$) the positively-directed carriers are absorbed without any ones injected. At the injection point x = 0, the ratio of the negatively-directed flux to the positively-directed flux yields the backscattering coefficient r_c. In the work of Chen, et al. [12] on 80-nm silicon conductor with a linear potential profile, the extracted mobility versus temperature has been found to be comparable with the literature silicon mobility data. This therefore confirms the validity of the relationship of $\lambda_o = 2\mu k_BT/qv_{inj}$, the non-degenerate case. The degenerate situation is addressed in the next section.

C. On the Mean-Free-Path for Backscattering

(1) Non-degenerate Statistics

Within the context of the channel backscattering [1],[2], the Boltzmann λ_o is the only mean-free-path for all operating conditions. More recently, however, sophisticated Monte Carlo simulation studies have pointed to the significance of the carrier heating in k_BT layer or in general the non-equilibrium transport over the channel. In the work of Palestri, et al. [13],[14], the carrier heating factor has been incorporated [14] by replacing λ_o in (2) with the *apparent* mean-free-path λ_1, thus constituting a new expression:

$$r_c = \frac{l}{l+\lambda_1} \quad . \tag{7}$$

Particularly, in case of non-degenerate statistics, the Monte Carlo simulations [14] at room temperature on a *linear* channel potential profile have exhibited a certain relationship: $\lambda_1 = \lambda_o/\gamma$ with γ = 1.5 to 2.0, different at all from that ($\lambda_1 = \lambda_o$) in the literature [1],[2]. This means that the backscattered flux is not Maxwellian but with much higher energy than the lattice temperature. Equivalently, the actual characteristic length over which backscattering affects r_c is longer than l and hence in the context of the channel backscattering this change is reflected in the change of the mean-free-path for backscattering [13],[14].

To clarify above arguments, Chen, et al. [15] have performed Monte Carlo simulations [11] on a silicon bulk conductor aimed at re-examining the channel backscattering in bulk nano-MOSFETs (see Fig. 13 to 17). Here, the potential profile used is not self-consistent but *frozen*, which allows a *direct* examination of the mean-free-path issue. The main results achieved in this study can be summarized below:

(i) The near-equilibrium mean-free-path for backscattering, λ_o, is independent of the potential profile.

(ii) The *apparent* mean-free-path, λ_1, in a localized quasi-ballistic k_BT layer can be linked with the curvature of the potential profile.

(iii) λ_1 in a linear potential profile is lower than λ_o due to the presence of the carrier heating, as highlighted by the carrier velocity distribution near the injection point.

(iv) In a parabolic potential profile, the mean-free-paths remain consistent: $\lambda_1 = \lambda_o$. This means that despite the quasi-ballistic transport prevailing in the k_BT layer ($\lambda_1 > l$), the quasi-equilibrium conditions still govern the backscattered carriers.

(2) Degenerate Statistics

Palestri, et al. [14] have further examined the effects of the carrier degeneracy in an inversion layer. Their conclusive remarks can be summarized as follows:

(i) Degeneracy can increase the Fermi-Dirac v_{inj} relative to the Maxwellian-Boltzmann v_{inj}.

(ii) Degeneracy can also increase the Fermi-Dirac λ_o relative to the Maxwellian-Boltzmann λ_o.

(iii) Degeneracy slightly increases r_c, relative to a significant improvement in the injection velocity.

(iv) In the presence of degeneracy, the mean-free-path for backscattering, λ_o or λ_1, is roughly proportional to the mobility.

(v) The relationship of $\lambda_1 = \lambda_o/\gamma$ holds while the corresponding γ needs further investigation.

(vi) In degenerate inversion layers, the dependence of r_c on l is essentially that of the non-degenerate case, valid as long as the above mentioned γ is correctly used.

D. Compact Models for the Critical Length l-I

On the basis of a parabolic potential profile around the source-channel junction barrier of nanoscale MOSFETs, a new compact model has been physically derived by Chen, et al. [16], which links the width of thermal energy k_BT layer (a critical zone in the context of the backscattering theory) to the geometrical and bias parameters of the devices:

$$l = \eta L \frac{1}{(V_G - V_{th})^{0.5}} \frac{1}{V_D^{0.25}} \frac{k_B T}{q} \qquad (8)$$

In this work, η is fixed and also is the only fitting parameter. It is expected that η is a constant, regardless of the channel length, gate and drain voltage, and temperature; otherwise, the applicability of the resulting model may be limited. A scatter plot has been created (see Fig.18 to 19) in terms of the experimental [12] and simulated [2],[13],[17]-[21] l versus the quantity of the functional expression $LV_D^{0.25}(V_G - V_{th})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Strikingly, all data are seen to fall on or around a straight line. The slope of the line furnishes η with a value of 4.1 $V^{-0.25}$. As expected, η remains constant, regardless of the channel length, gate and drain voltage, and temperature. The only fitting parameter remains constant in a wide range of channel length (10 to 65 nm), gate voltage (0.4 to 1.2 V), drain voltage (0.2 to 1.2 V), and temperature (100 to 500 K).

Some remarks can now be made to clarify the confusing α values in the power law of $l \propto T^{\alpha}$ in the open literature. Firstly, it is noticed that in case of bulk n-MOSFET two different values of α were produced: one of 0.5 [12] and one of 0.75 [9]. This difference can be attributed to the different subband treatments during the parameter extraction process: a Schrödinger-Poisson equation solving was utilized in [12] whereas in [9] this was done by a triangular potential approximation. Therefore, the different subband levels can lead to different average thermal injection velocities, which in turn give rise to different l values. Secondly, the temperature range of 233 to 298 K in case of 55-nm bulk device [12] is not wide enough. In other words, the result is considerably insensitive to such a narrow temperature range. Consequently, the resulting *apparent* temperature power exponent was limited to 0.5 as reported in the previous work [12]. Indeed, with the known η as input, fairly good reproduction can be achieved, without adjusting any parameters. The same interpretations also apply to the $\alpha \approx 0.57$ case [17]: only the room temperature of operation was involved and therefore the temperature effect cannot be examined fully. In other words, only in a wide temperature range (as done in the comprehensive study of [13],[19]) can the linear relationship of $l \propto T$ be observed. Finally, from the aspect of temperature dependencies or the excellent coincidence with a significant number of data, the existing backscattering coefficient extraction method [5] remains valid.

E. Compact Models for the Critical Length l-II

Recently, Khakifirooz and Antoniadis [22] have established a new power law relationship between l and the mobility:

$$l \propto \mu^{-\beta} \qquad (9)$$

Here, the power exponent β has been empirically determined to be around 0.45 [22]. The velocity overshoot near drain is responsible. Additionally, the ballistic velocity has also a power exponent of its own: $v_{inj} \propto \mu^{\alpha}$ with $\alpha \sim 0.5$ [22]. Consequently, the relative change of the virtual source carrier velocity v_{xo} can be linearly connected to that of the mobility [22]:

$$\frac{\partial v_{xo}}{v_{xo}} = (\alpha + (1-B)(1-\alpha+\beta)) \frac{\partial \mu}{\mu} \qquad (10)$$

where B is the ballistic fraction and is equal to $\lambda/(2l+\lambda)$. Here λ represents the underlying mean-free-path for backscattering. This expression can provide the design guideline for the strain engineering.

F. Compact Models for r_c Extraction

Barral, et al. [23] have derived a new analytic model to help extract r_c accurately. In this model, the injection velocity has been expressed as a function of both Q_{inv} and r_c:

$$v_{inj} = a\sqrt{\frac{Q_{inv}}{1+r_c}} \qquad (11)$$

where a is a physical constant. This experimentally oriented r_c extraction method has been successfully applied to 10-nm FDSOI devices [23].

V. Challenging Issues

A. Equilibrium versus Non-equilibrium

First of all, Chen, et al. [15] have demonstrated that the different mean-free-paths between the parabolic and linear potential profiles can be traced to the curvature of the potential profile, especially the presence or absence of a zero or weak field regime near the injection point. For a parabolic potential profile, there is a significant fraction of the k_BT layer, which can be identified as the zero-field regime. With this in mind, although the deviations from the lattice

temperature would be possible as entering into the remainder (that is, out of the zero-field regime), the overall carrier heating in the k_BT layer should be weakened. For a linear potential profile, however, such a zero-field regime is lacking. Therefore, once injected at the beginning of the k_BT layer, the carriers immediately undergo acceleration from the non-zero field. Owing to the quasi-ballistic transport (less collision), the carrier temperature is expected to be higher than the lattice temperature and the mean-free-path is therefore no longer independent of the carrier energy. The confirmative evidence is presented in terms of the carrier velocity component υ_x distribution in the transport direction near the injection point (see Fig. 16 and 17). They were all created by the program DEMONs. For a parabolic potential profile a single hemi-Maxwellian distribution is retained in the positively-directed carriers but is split into two distinct components in the linear potential case: One of the longitudinal effective mass and one of the transverse effective mass. This strongly points to the effect of the non-zero field in the linear potential profile.

Through the Monte Carlo simulation with the degeneracy effects neglected, Jungemann, et al. [24] have observed that (i) the positively-directed injection velocity at the peak of the source-channel barrier increases due to non-equilibrium effects; and (ii) the backscattered velocity is reduced thus increasing the drift velocity even further. This effect is stronger in strained silicon, where the backward velocity is almost the same as for unstrained Si, while the injection velocity is much higher.

Fischetti, et al. [25] have emphasized the significance of the so-called "source starvation": the inability of the source region to sustain a large flow of carriers in longitudinal velocity states in the channel, unless the momentum relaxation rate and/or the doping density in the source are sufficiently large. Their simulation results have pointed to the fact that it can be erroneous to assume an equilibrium carrier distribution, not only near the source-channel junction or in the channel, but also a few diffusion-lengths inside the heavily-doped source region. Within or near the ballistic regime, electrons are carried away so efficiently along the channel that the source region becomes "starved" of carriers populating longitudinal k states. Unless the momentum relaxation time in the source becomes sufficiently short, there will not be enough carriers which can be injected into the channel and contribute to the drain current. A higher doping in the source supplies more carriers which can be scattered and redirected into longitudinal k states. It also reduces the momentum relaxation time, as there are more impurities to which electrons can transfer momentum [25].

B. Carrier Degeneracy

In *bulk* nano-MOSFETs, the underlying carrier degeneracy is quite weak, as reflected by an existing low value (≈1.3 for a 1-V gate voltage as cited from Ref. [9]) of the Fermi-Dirac injection velocity to Maxwellian injection velocity ratio. However, for the case of the ultra-thin film counterparts, the carrier degeneracy is pronounced due to the *space* confinement effect [14].

C. Drain Scattering and Coulomb Scattering

Well recognized backscattering theory of MOSFETs [1],[2] argues that a key zone located near the thermal equilibrium reservoir source can critically determine the device's performance. This statement remains valid as long as the backscattered carriers from the remainder of the channel are energetically insignificant with respect to the peak of the source-channel barrier. For ultra-short devices with ballistic transport across the channel, however, the backscattering events in the drain, through the feedback to the source, may ultimately dominate, as revealed by the Monte Carlo particle simulations [26],[27].

Khakifirooz and Antoniadis [22] have experimentally shown that the virtual source electron velocity or equivalently the ballistic fraction B increases with channel length shrinking but tends to saturate as the channel length is reduced below a certain critical length of 40 to 60 nm. They have attributed such a saturation trend to the halo implant pocket induced Coulomb scattering. Alternative interpretations have been suggested by Fischetti, et al. [28]: Long-range electron-electron interactions. Such Coulomb scattering encountered by electrons in the channel may stem from those in the source, the drain, and even the gate [28].

D. Nanowires

Tian, et al. [29] have successfully fabricated silicon nanowire transistors with 10-nm diameter. They have also measured corresponding channel backscattering characteristics for the first time.

VI. Conclusion

The historical overview of the channel backscattering framework has been presented. Both the recent studies and the challenging issues have been addressed. To improve the existing channel backscattering framework, several key directions are suggested in the following:

- The effects of non-equilibrium conditions, such as the source starvation, the velocity overshoot near the drain, and the carrier heating in the source;
- The effects of carrier degeneracy;
- The temperature dependent method clarified;
- The effects of long-range Coulomb scattering;
- Significant extension to 1-D nanoFETs case.

It is therefore expected that the device researchers worldwide would collaborate together in an effort to improve the device physics in the context of the channel backscattering. Ultimately, the resulting updated channel backscattering framework can apply to thermal injection nanoFET structures, both 1-D and 2-D, with the feature size down to 10 nm and beyond.

Acknowledgements

This work was supported by the National Science Council under contract no. NSC 96-2221-E-009-187.

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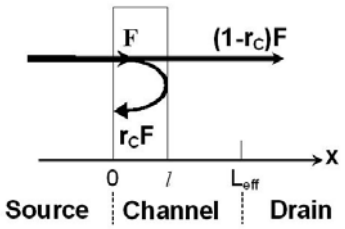

Fig. 1 Schematic diagram of channel backscattering theory. F is the incident flux from the source, *l* is the critical distance in a KT/q drop, and r_C is the channel backscattering coefficient. The channel length L_{eff} is the mask gate length L_{GM} minus the source/drain extensions.

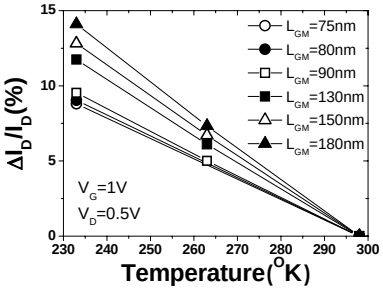

Fig. 2 Measured drain current change at V_G = 1 V versus temperature with mask gate length as a parameter. V_D = 0. 5 V.

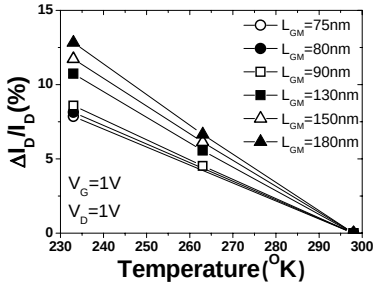

Fig. 3 Measured drain current change at V_G = 1 V versus temperature with mask gate length as a parameter for V_D = 1 V.

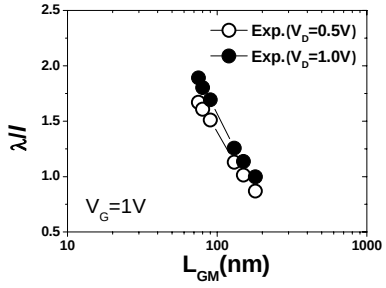

Fig. 4 Extracted λ_o/l at V_G = 1 V versus gate length for two drain voltages.

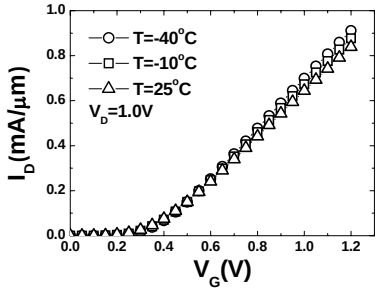

Fig. 5 Measured drain current versus gate voltage at V_D = 1 V for three temperatures.

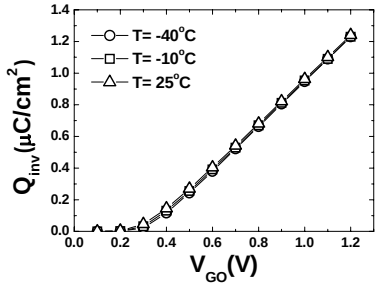

Fig. 6 Calculated inversion-layer charge density versus intrinsic gate voltage for three temperatures.

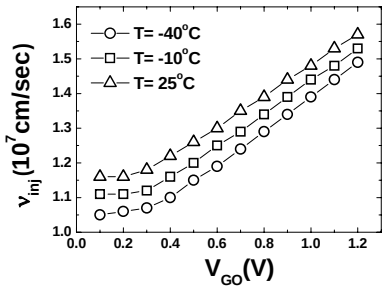

Fig. 7 Calculated thermal injection velocity versus intrinsic gate voltage for three temperatures.

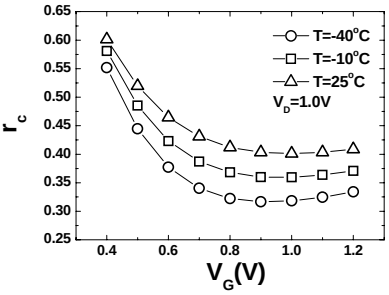

Fig. 8 Extracted backscattering coefficients corresponding to Fig. 5.

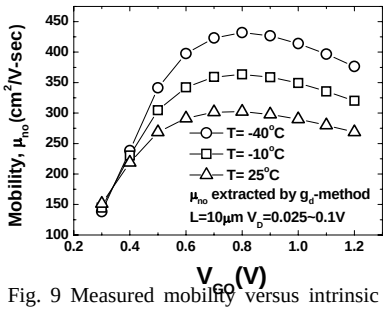

Fig. 9 Measured mobility versus intrinsic gate voltage for three temperatures.

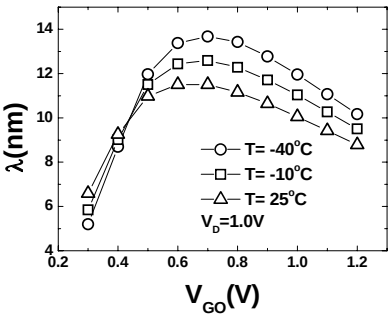

Fig. 10 Extracted mean-free-path λ_o versus intrinsic gate voltage for three temperatures.

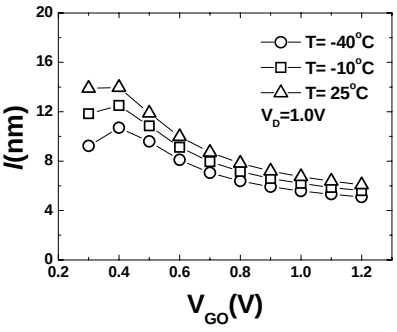

Fig. 11 Extracted k_BT layer width corresponding to Fig. 5.

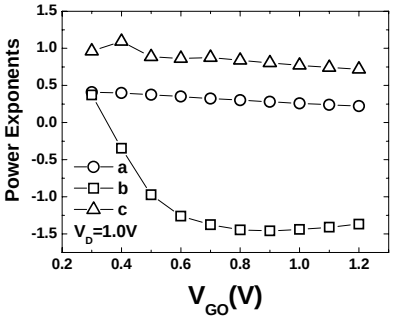

Fig. 12 Fitted power exponents versus gate voltage. The label a stands for β_{vinj}, b for β_μ and c for β_l.

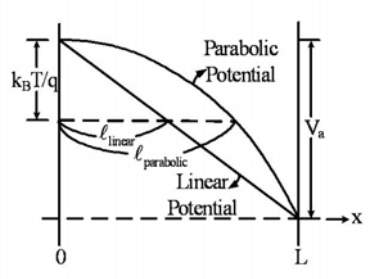

Fig. 13 The two potential profiles used in the simulation study. Also shown is the width of the k_BT layer.

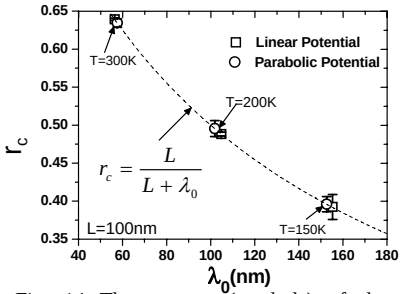

Fig. 14 The average (symbols) of the simulated r_c over 10^{-5} V ≤ V_a ≤ 10^{-3} V for two potential profiles and three temperatures versus corresponding near-equilibrium mean-free-path λ_o via Eq.(1). The bar stands for the range of the simulated r_c values.

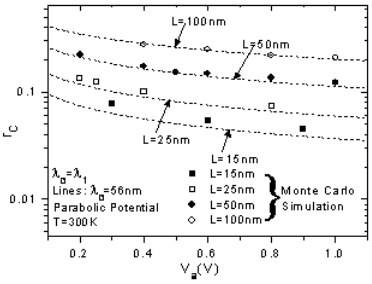

Fig. 15a Comparison of the simulated (symbols) and calculated (lines) r_c for four conductor lengths in a parabolic potential profile versus applied voltage for (a) 300 K, (b) 200 K, and (c) 150 K. The calculations are from Eq.(4) with $\xi = 2/\sqrt{\pi}$ [4] and $\lambda_1 = \lambda_o$.

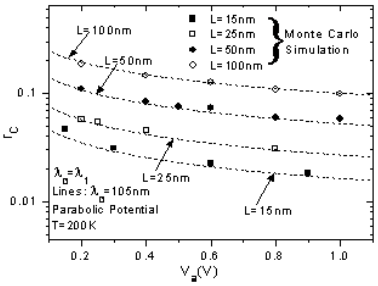

Fig. 15b Comparison of the simulated (symbols) and calculated (lines) r_c for four conductor lengths in a parabolic potential profile versus applied voltage for (a) 300 K, (b) 200 K, and (c) 150 K. The calculations are from Eq.(4) with $\xi = 2/\sqrt{\pi}$ [4] and $\lambda_1 = \lambda_o$.

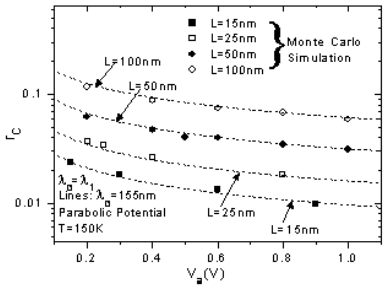

Fig. 15c Comparison of the simulated (symbols) and calculated (lines) r_c for four conductor lengths in a parabolic potential profile versus applied voltage for (a) 300 K, (b) 200 K, and (c) 150 K. The calculations are from Eq.(4) with $\xi = 2/\sqrt{\pi}$ [4] and $\lambda_1 = \lambda_o$.

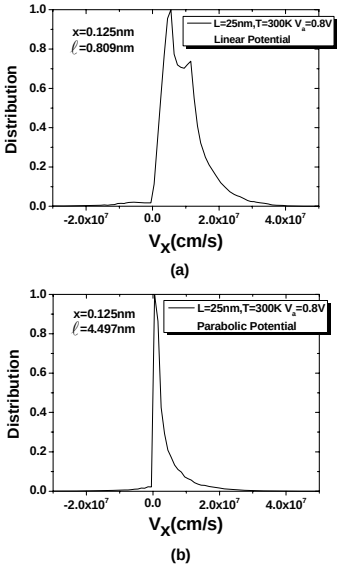

Fig. 16 The simulated carrier velocity component distribution in the transport direction at x = 0.125 nm for (a) a linear potential profile and (b) a parabolic potential profile. L = 25 nm, T = 300 K, and V_a = 0.8 V.

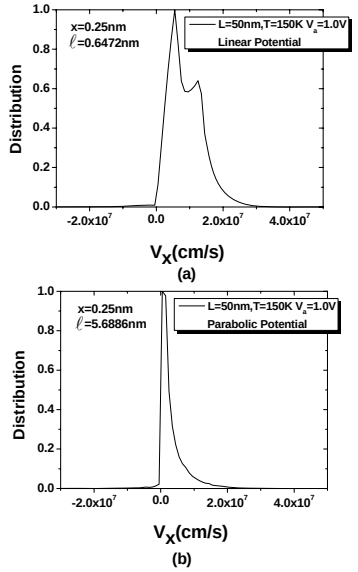

Fig. 17 The simulated carrier velocity component distribution in the transport direction at x = 0.25 nm for (a) a linear potential profile and (b) a parabolic potential profile. L = 50 nm, T = 150 K, and V_a = 1.0 V.

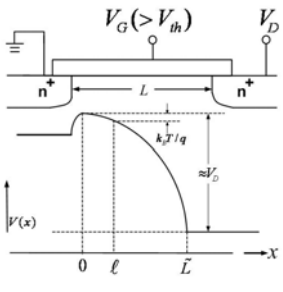

Fig. 18 Schematic demonstration of the parabolic source-channel potential barrier picture corresponding to a nano-MOSFET in saturation. The parabolic potential profile is extended to the drain side to highlight the *apparent* channel length designated $\tilde{L}$. Also shown is the width l of the k_BT layer.

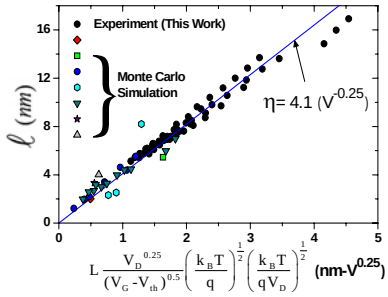

Fig. 19 Scatter plot of the experimental and simulated l versus the quantity of the functional expression $L(V_D^{0.25})(V_G-V_{th})^{-0.5}(k_BT/q)^{0.5}(k_BT/qV_D)^{0.5}$. Also shown is a straight line which fits the data points. The slope of the line yields η of 4.1 $V^{-0.25}$.