行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：■個別型計畫　　□整合型計畫

計畫編號：NSC 89-2215-E-009-037

執行期間：88 年 8 月 1 日至 89 年 7 月 31 日

計畫主持人：黃調元 交通大學電子工程系教授

協同研究人員：林鴻志 國科會毫微米實驗室研究員

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

□赴大陸地區出差或研習心得報告一份

■出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

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中 華 民 國 89 年 10 月 30 日

行政院國家科學委員會專題研究計畫成果報告

深次微米 T 型閘極金氧半電晶體之改良研製及其效應之研究

Fabrication and Characterization of deep-submicron MOSFET with T-gate structure using a refined process with nitride/TEOS stack spacer

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一、中文摘要

本計畫延續並改善上年度研製新式自我校準之T型閘極金氧半電晶體，我們簡稱為STAIR製程，進而提升元件操作之性能與應用。原先的製程中，我們使用B.O.E溶液去除T型側翼下方之氧化層，然而此步驟控制不易，將造成閘極氧化層邊緣之閘極漏電流，低電荷崩潰之缺陷。故本計畫成功的提出沈積一Si_3N_4/TEOS堆疊薄膜於閘極區域邊襯上，用以保護閘極氧化層，改善原先T型閘極電晶體製程上的缺失。此外，閘極和源/汲極間之鈷矽化物橋接現象也有極大的改善。

關鍵詞：自我校準，T 型閘極，堆疊邊襯，橋接

Abstract

The project is the continuation and improvement of the previous year project: “Development and Characterization of a Novel Method for Fabricating deep-micron Si MOSFET with T-Shaped Gate”, which we have dubbed STAIR [1-2](Self-Aligned T-shaped Gate and Air Spacer) for achieving high performance. In the original process flow to fabricate the STAIR transistors, the critical thin gate oxide edge was exposed during the required long B.O.E. treatment, thus severely undermined the thin gate oxide integrity and yield. In this project, we propose and demonstrate a refined and manufacturable process flow to fabricate robust STAIR transistor that eliminates the above-mentioned short-comings altogether. This improved process adopts a nitride/TEOS stack-spacer at the sidewall of the poly-Si gate, which serves as a protection layer during the following process steps. Its effectiveness in reducing the gate leakage as well as bridging probability is clearly demonstrated in this work.

Keywords: Self-Aligned, T-shaped gate, stack-spacer, bridging

二、緣由與目的

Self-aligned silicide (salicide) process is extremely important for deep sub-micron manufacturing in order to reduce device's parasitic resistance. As devices' dimensions are scaled down, however, the sheet resistance of narrow silicide lines is known to rise with decreasing line width due to increasing difficulty in phase transition of silicide [3][4], and/or poor thermal stability [5]. In the past year , we proposed a novel T-shaped gate formation process to solve the aforementioned problems [1]. This is ascribed to the structural improvement since the effective width of silicide on salicided poly-Si gates increases. We have also developed a novel transistor structure dubbed STAIR, since the fabricated devices feature self-aligned T-shaped gate and air spacer [2]. However, in the original process now to fabricate the STAIR transistors, the critical thin gate oxide was exposed during the required long BOE treatment, thus severely undermined the thin gate oxide integrity and yield. In this project, we propose and demonstrate an improved process now to fabricate robust STAIR transistor that eliminates the above-mentioned short-

comings altogether.

三、研究方法與成果

The improved process now is as illustrated in Fig.1. Briefly, after growing a gate oxide (4.8 nm) and n^+-poly-Si layers (200 nm), gate resist patterns were formed, followed by conventional steps to form the gate and S/D regions. A novel nitride (5 nm)/TEOS (100 nm) stack-spacer was formed (Fig.1a). The spacer was used for self-aligned separation of the extension and deep S/D regions. Then, an additional 550nm-thick TEOS was deposited and planarized by CMP to a remaining thickness of around 350 nm (Fig.1b). BOE selective etching was then used to further thin down the TEOS layer to around 100 nm. The thin nitride on the sidewall of the exposed gate was then stripped with H3PO4 solution (Fig.1c). Next, a 2nd poly-Si layer was deposited and R.I.E.-etched to form the T-shaped gate (Fig.1d). The remaining TEOS was then stripped off by BOE etching (Fig.1e). SEM Picture the T-shaped gate structure after this step is shown in Fig.2. Co Salicide treatment was performed on some of the fabricated samples. A Co (10nm)/TiN (30 nm) stacked layer was deposited by sputtering. Due to the shadowing nature of the T-shaped gate, the metal film is deposited with a form as shown in Fig.3(a) and demonstrated by SEM picture in Fig.3(b). Such film structure can potentially reduce the possibility of bridging between gate and source/drain since the deposited films are disconnected. After the T-gate processing, a550-nm-thick TEOS was deposited and an air spacer is formed, as shown in Fig.4. In this work, both low-pressure chemical vapor deposition (LPCVD) and plasma-enhanced (PE) CVD were employed for forming the TEOS layer. Both methods successfully show the formation of air spacer, as shown in Figs.4(a) and(b), respectively. These results are ascribed to the fast deposition rate of TEOS as well as the weight of the TEOS film imposing on the T-shaped gate. The weight serves to bow the “wing” of the gate down and help prevent the deposited species from entering the portion underneath the “wing”.

In the step shown in Fig.1(e), the presence of the thin nitride layer at the sidewall of the gate is critical to protect the gate oxide. While in the original scheme which is without nitride protection [5], gate oxide near the sidewall is vulnerable to attack by BOE(Fig.5), thus leads to dramatic increase in gate leakage. Such degradation is clearly illustrated in Fig.6. In this figure, test devices received an intended longer overetch time during BOE etching in order to highlight the damage. It can be seen that a significant portion of samples without nitride layer shows high gate leakage. On the other hand, the 5-nm-thick nitride spacer is demonstrated to be effective in protecting the gate oxide from being damaged. Fig. 7 (a) (b) are the typical subthreshold I-V ,and gate leakage current curve of T-shaped gate devices without or with nitride protection, respectively.

The effectiveness of T-shaped gate in reducing the sheet resistance is illustrated in Fig.8, in which the sheet resistance of conventional poly-Si gate, poly-Si T-shaped gate, and salicided T-shaped gate were measured and compared. It can be seen that the conventional poly-Si gate structure indeed suffers from the so called “narrow-line-width effect", depicting a dramatic increase in sheet resistance for gate length smaller than 0.4 μm. This undesirable effect is effectively suppressed with the use of poly-Si T-shaped gate structure. Further improvement in sheet resistance is achieved with the implementation of Co Salicide.

An edge-intensive test structure (total length =10 cm) was used to characterize the bridging performance. The results are shown in Fig.9. Again, thin nitride protection at sidewall is shown to be effective in reducing the bridging probability. Since the deposited metal layers on the gate and source/drain regions are disconnected, bridging due to formation of silicide over dielectric spacer encountered in conventional salicide scheme should not occur in the STAIR devices.

Bridging may probably be induced due to a small amount of metal deposited near the S/D regions close to the gate sidewall. These metal species could form silicide and short the gate and source/drain. With the nitride protection, however, such phenomenon can be effectively suppressed.

Typical I-V Characteristics of 0.25μm devices with conventional poly-Si gate and salicided T-shaped gate are shown in Fig10 and Fig11. Significant improvement in the driving current is observed for the salicided T-gate devices, indicating that the source and drain contact resistance is effectively reduced.

四、結果與討論

In this work, we report a modified STAIR process by adding a thin nitride layer at the sidewall of poly-Si gate. Our results clearly demonstrated that the refined approach can effectively reduce the gate leakage and bridging probability. The improved version is therefore robust and production-worthy.

五、計畫成果自評

STAIR transistors using a refined process with nitride/TEOS spacer is robust and manufacturable in deep-submicron regime. In addition, it is compatible with salicide process. It is therefore very promising for future high-speed device applications.

Some works have been published on the proceeding of conference [2] [6]. .

六、致謝

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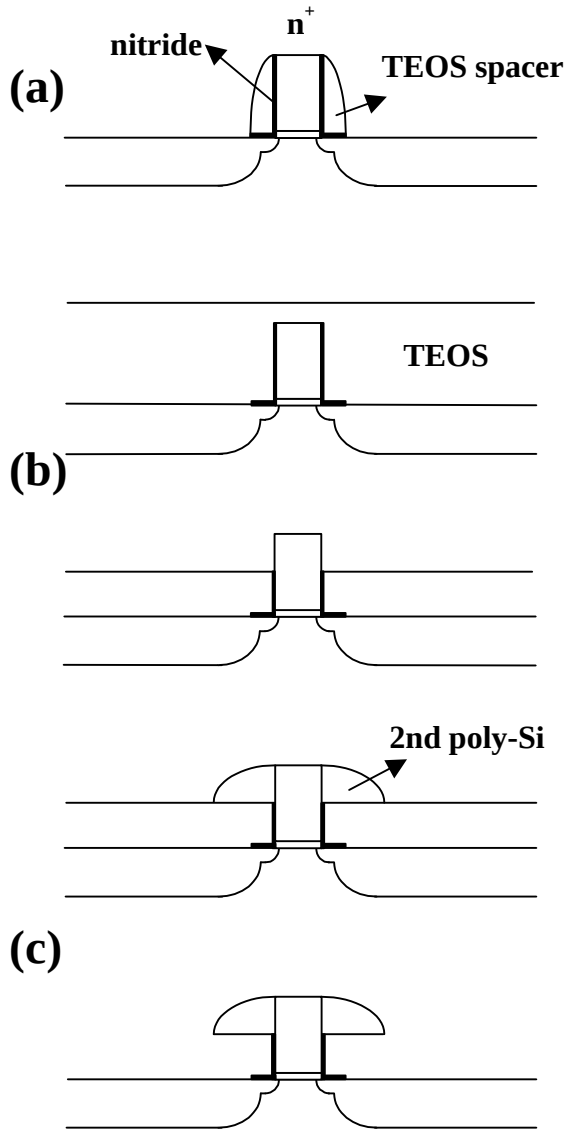

Fig. 1 Process Flow of the Improved T-gate Formation Method.

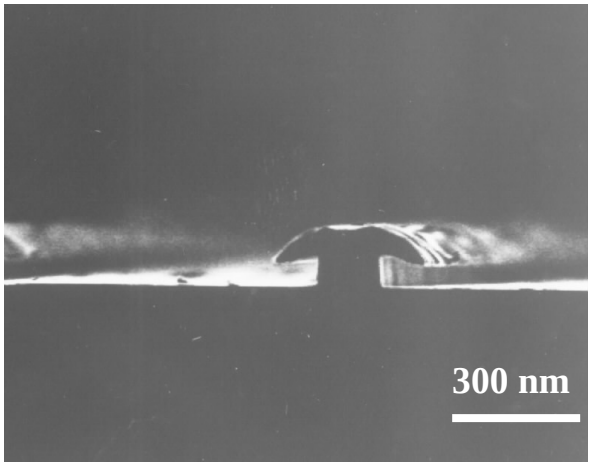

Fig. 2 SEM of the T-shaped Gate.

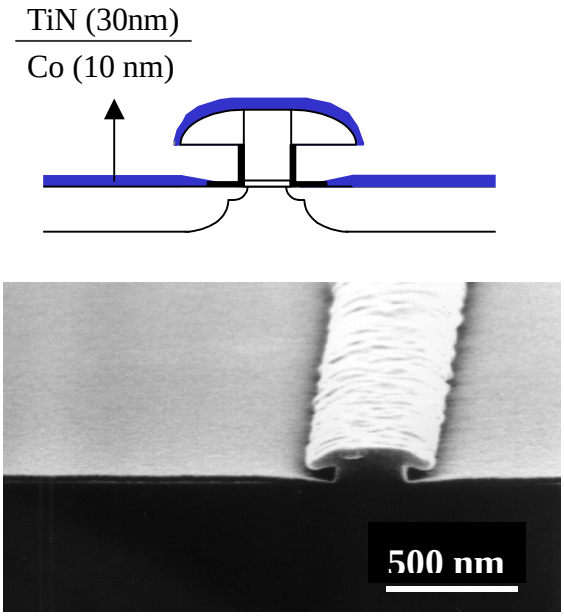

Fig. 3 (a) Illustration and (b) SEM picture of the film deposited on the T-gate structure.

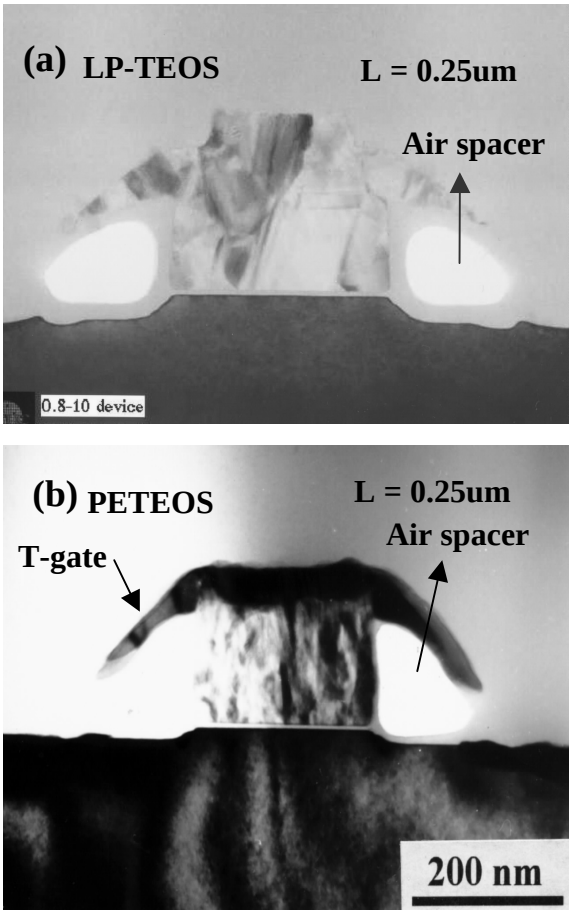

Fig. 4 Cross-sectional TEMs of gate Structure Showing the T-gate and Air Spacer with (a) LPCVD and (b) PECVD TEOS passivation.

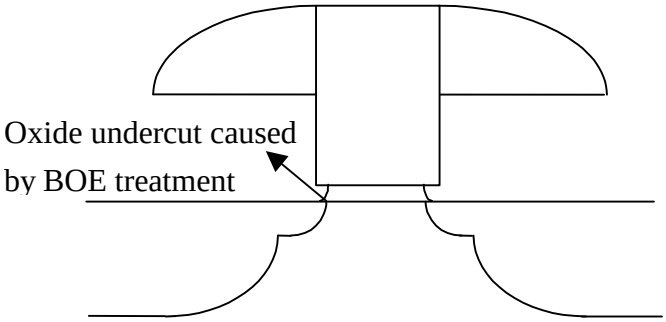

Fig. 5 Undercut formation in gate oxide without sidewall nitride protection during BOE etching in the original scheme.

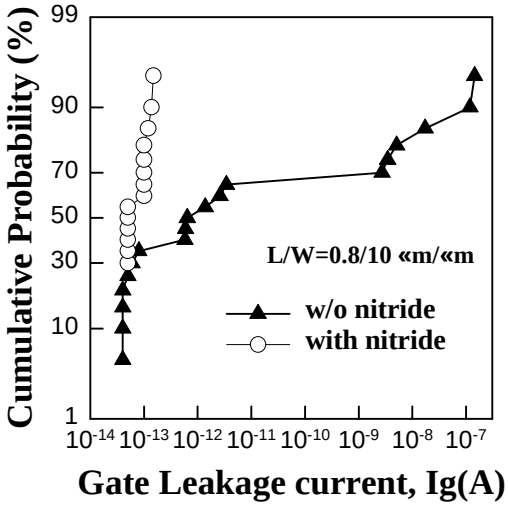

Fig. 6 Gate leakage characteristics of NMOS with intentional long BOE etching

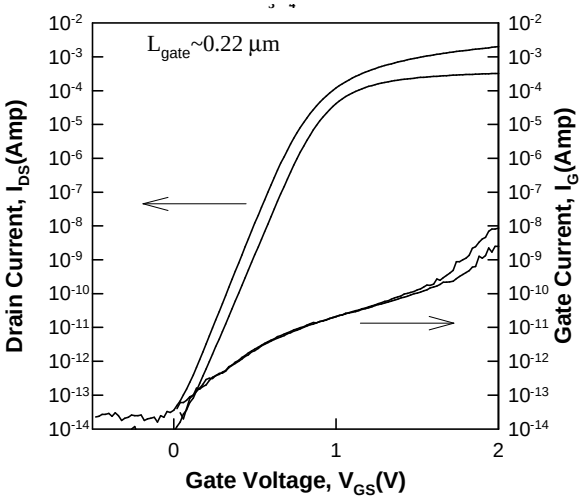

Fig. 7(a) Effect of gate leakage without sidewall nitride protection.

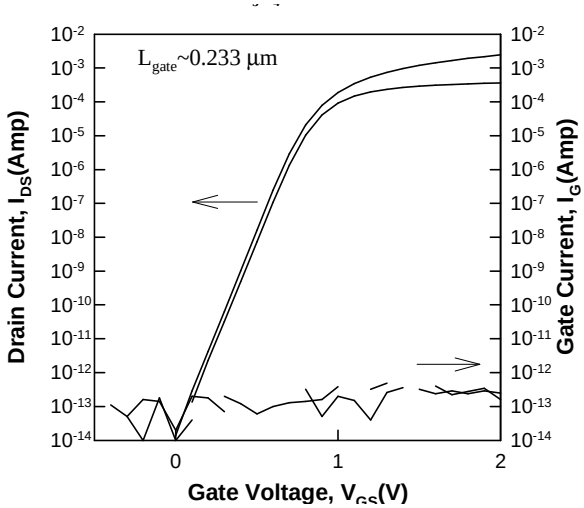

Fig. 7(b) Effect of gate leakage with sidewall nitride protection.

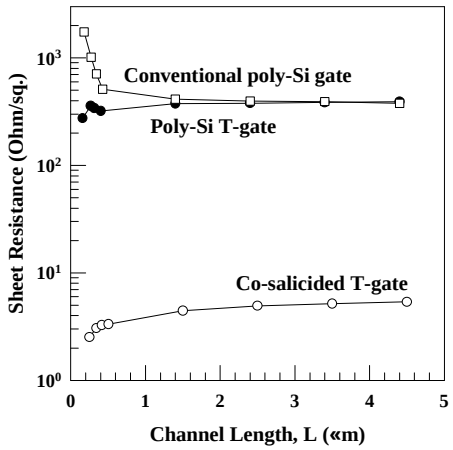

Fig. 8 Sheet resistance of conventional poly-Si gate, poly-Si T-gate, and Co-salicided T-gate structures as a function of channel length.

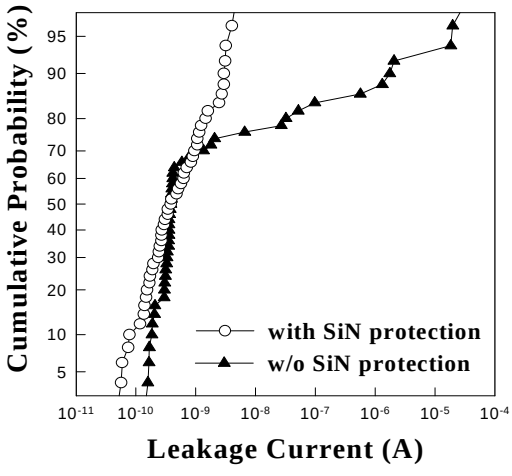

Fig. 9 Leakage current between gate and source/drain.

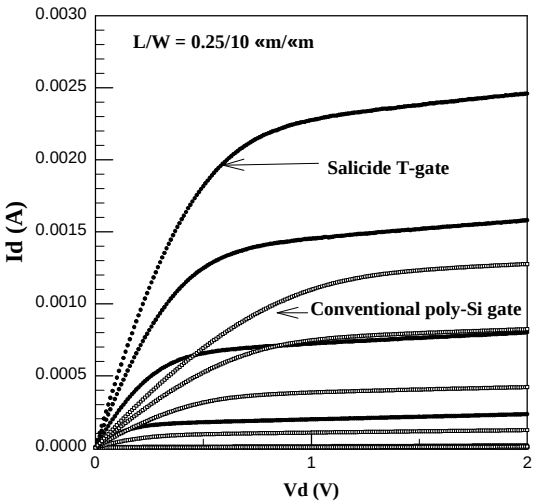

Fig.10 Output Characteristics of 0.25 um NMOS Transistors.

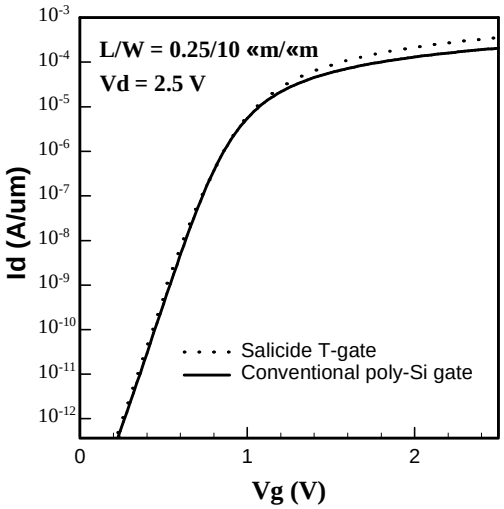

Fig.11 Subthreshold Characteristics of 0.25 um NMOS Transistors.