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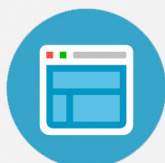

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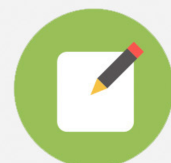

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# Self-aligned contact metallization technology for III-V metal-oxide-semiconductor field effect transistors

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The demonstration of a salicidelike self-aligned contact technology for III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) is reported. A thin and continuous crystalline germanium-silicon (GeSi) layer was selectively formed on $n^+$ doped gallium arsenide (GaAs) regions by epitaxy. A new self-aligned nickel germanosilicide (NiGeSi) Ohmic contact with good morphology was achieved using a two-step annealing process with precise conversion of the GeSi layer into NiGeSi. NiGeSi contact with the contact resistivity ($\rho_c$) of 1.57 $\Omega$ mm and sheet resistance ($R_{\text{sh}}$) of 2.8 $\Omega/\square$ was achieved. The NiGeSi-based self-aligned contact technology is promising for future integration in high performance III-V MOSFETs. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3592211]

## I. INTRODUCTION

III-V materials such as gallium arsenide (GaAs) and indium gallium arsenide (InGaAs) have significantly higher electron mobility than silicon (Si) and are attractive channel material candidates for metal-oxide-semiconductor field-effect transistors (MOSFETs) in future high-speed and low-power logic applications.[1–12] To realize high-performance III-V MOSFETs, low channel resistance as well as low parasitic series resistance in the source/drain (S/D) regions are required. Series resistance in the S/D regions includes the resistance in the doped S/D and the contact resistance between the doped S/D and the contact material. Selective growth of *in situ* doped S/D materials has recently been used for reducing the series resistance in the doped S/D.[13–15] In addition, contacts with low contact resistance to the S/D regions are required. Contacts for III-V MOSFETs can be formed by direct deposition and patterning (e.g., lift-off) of metals on the doped S/D, with or without a subsequent alloying anneal.[16–22] Contact metallization in III-V MOSFETs is usually non-self-aligned with respect to the gate stack, unlike the self-aligned salicidation process in Si MOSFETs. A spacing between the contact metal and the gate leads to increased series resistance that compromises drive current $I_{\text{Dsat}}$ performance. III-V MOSFETs with self-aligned contacts are thus needed for reduction of series resistance and for better device density scaling.[23,24] While a height selective etching process has been developed to achieve self-aligned contact for III-V MOSFETs,[15,24] a self-aligned metallization process analogous to the salicidation process in Si complementary metal-oxide-semiconductor technology is still needed for III-V MOSFETs.[25,26]

In this article, we report the demonstration of a salicide-like self-aligned nickel germanide (NiGe) based contact technology for GaAs MOSFETs. NiGe-based contact is attractive due to the low resistivity of NiGe (22 $\mu\Omega$ cm) as compared with PdGe (30 $\mu\Omega$ cm), the low cost of Ni, and the low germanide formation temperature[27–29] that is compatible with III-V materials. Transmission line method (TLM) test structures were fabricated using a process flow shown in Fig. 1 in the development of the self-aligned metallization technology. A thin continuous high-quality germa-

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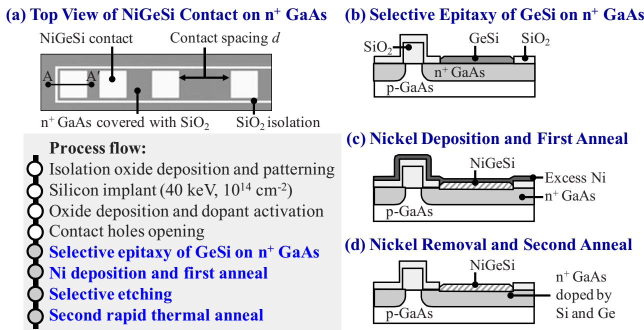


FIG. 1. (Color online) (a) Plan-view optical microscopy image of the TLM structure. The self-aligned ohmic contact formation process comprises (b) selective epitaxy of GeSi on n$^+$ GaAs in a contact hole, (c) Ni deposition and a first thermal anneal for NiGeSi formation, (d) removal of excess Ni, and a second thermal anneal to form the Ohmic contact.

nium silicon (GeSi) layer was first selectively grown on n$^+$ doped GaAs regions [Fig. 1(b)]. Second, a two-step germanosilicide process was developed to form nickel germanosilicide (NiGeSi) Ohmic contacts on GaAs, where hydrochloric acid (HCl) was employed for selective removal of unreacted Ni [Figs. 1(c) and 1(d)].

## II. DEVELOPMENT OF SELF-ALIGNED CONTACT TECHNOLOGY

p-type ($N_A \sim 5 \times 10^{16}$ cm$^{-3}$) GaAs (001) substrates were used to fabricate test structures which enable the extraction of contact resistance using the TLM.[30,31] A $SiO_2$ isolation pattern was formed and Si was implanted at an energy of 40 keV and a dose of $1 \times 10^{14}$ cm$^{-2}$. The projected Si implant depth and straggle are 43 and 22 nm, respectively. A thin capping layer of $SiO_2$ ($\sim$30 nm) was then deposited before dopant activation at 800 °C for 10 s. The $SiO_2$ cap was patterned and etched to define contact holes that exposed the n$^+$ GaAs surface for contact formation.

### A. Selective epitaxy of germanium silicon (GeSi) on GaAs

An epitaxy process was employed to selectively form a continuous GeSi film ($\sim$40 nm) on the n$^+$ GaAs surface in the contact holes. The wafers were annealed in vacuum at 650 °C for native oxide desorption before being loaded into a GeSi growth chamber. Epitaxial growth was performed at 565 °C using $SiH_4$ and $GeH_4$ as precursors with the flow rates of 3 and 5 SCCM (SCCM denotes cubic centimeter per minute at STP), respectively. The process pressure was maintained at 30 mTorr. $SiH_4$ flow was introduced during growth in an attempt to overcome the islanding issue which occurs when only $GeH_4$ precursor was used. Growth of GeSi seemed to have a flatter surface morphology as compared to the growth of Ge.[32] Ge islanding on n$^+$ GaAs gives a discontinuous Ge film and would cause Ni penetration into GaAs during a subsequent contact metallization step. This is expected to result in a nonuniform contact. It has been reported that NiGe formed on single crystalline Ge exhibits better uniformity and thermal stability than that formed on poly-

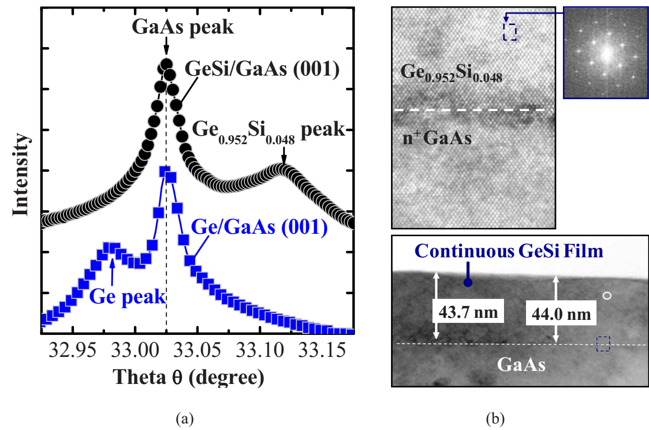


FIG. 2. (Color online) (a) High resolution x-ray diffraction (HRXRD) shows that 4.8 at. % of Si was incorporated in GeSi. The spectra intensity is plotted using a logarithmic scale. GeSi formed on GaAs is under tensile strain. (b) Transmission electron microscopy (TEM) shows the GeSi/GaAs heterostructure formed and a diffractogram of a selected region enclosed by a dashed box indicates the good crystalline quality of GeSi.

crystalline Ge.[33] A continuous GeSi film with good single crystalline quality is crucial for NiGeSi contact formation.

The grown Ge and GeSi (004) diffraction peaks were clearly observed from the high resolution x-ray diffraction (XRD) [Fig. 2(a)]. The values of full width at half maximum were 0.02° and 0.037° for the Ge and $Ge_{0.952}Si_{0.048}$ films, respectively, suggesting that the crystal quality is better for a lower lattice mismatch between the epilayer and GaAs. XRD spectra indicates that Ge (lattice constant=5.6577 Å) film on GaAs (lattice constant=5.6537 Å) is under a slight compressive strain with $2\theta$=32.981° while fully relaxed Ge has a $2\theta$ of 33.0°. However, GeSi film on GaAs is fully tensile strained with $2\theta$=33.118° and the composition was extracted to be $Ge_{0.952}Si_{0.048}$ by fitting XRD spectra using X'Pert epitaxy. Peak shift of Raman spectroscopy (not shown here) is 301 cm$^{-1}$ for Ge/GaAs and 298.9 cm$^{-1}$ for GeSi/GaAs, consistent with the strain and composition of the epilayers.

Transmission electron microscopy (TEM) images [Fig. 2(b)] indicate that the single-crystalline GeSi was uniformly formed and is free from dislocations. The TEM images in Fig. 2(b) also show the abrupt interface between GeSi and GaAs. Fast Fourier transform diffractogram [Fig. 2(b)] reveals the good crystalline quality of the GeSi epitaxial layer.

### B. Two-step metallization process for contact formation

Single crystalline GeSi film (40$\sim$50 nm) was grown on blanket GaAs substrate followed by Ni ($\sim$30 nm) deposition. The structure of the sample is illustrated in Fig. 3. The Ni/GeSi/GaAs wafer was then cut into pieces and each piece went through rapid thermal anneal (RTA) at a different temperature for 60 s for the formation of NiGeSi. The RTA temperature ranges from 150 to 600 °C. The sheet resistance ($R_{sh}$) of NiGeSi formed at various anneal temperatures was



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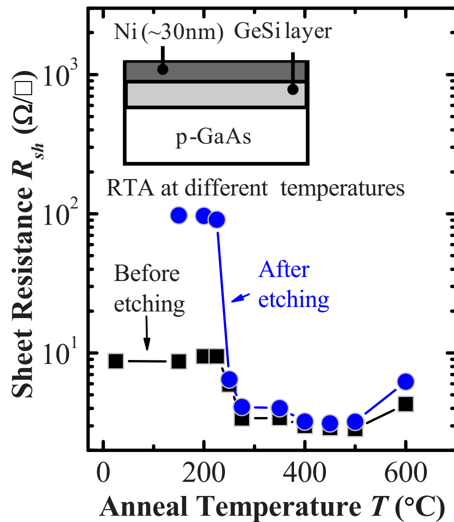


FIG. 3. (Color online) Sheet resistance vs anneal temperature for ~30 nm Ni on blanket GeSi/GaAs sample annealed at different temperatures for 60 s. The sheet resistance values of annealed sample with and without selective etching in hot HCl are indicated by square and circle symbols, respectively. Nickel germanosilicide formed at above 250 °C has a low sheet resistance even after the selective etching process.

investigated. A four-point probe was used to measure $R_{sh}$. XRD was performed to analyze the nickel germanide phase transformation.

Figure 3 shows the $R_{sh}$ of NiGeSi/GaAs samples right after RTA (square symbols) at different temperatures. The $R_{sh}$ of the as-deposited sample was 8.7 Ω/□. After annealing at 200–225 °C, $R_{sh}$ was slightly increased to 9.5 Ω/□ due to Ni consumption and $Ni_5Ge_3$ formation (Fig. 4). $Ni_5Ge_3$ has a higher resistivity than the deposited Ni film. Nickel monogermanide (NiGe), a low resistivity phase, started to form at 250 °C and $R_{sh}$ decreased to 5.9 Ω/□. Both $Ni_5Ge_3$ and NiGe phases exist when the samples were annealed at 250 °C. When the annealing temperature was increased

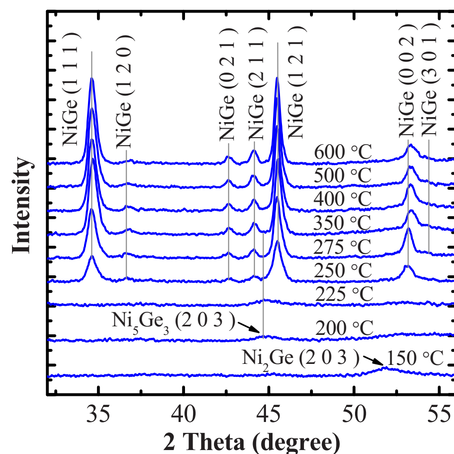


FIG. 4. (Color online) XRD spectra shows nickel germanide phases formed from 150 and 600 °C. The spectra intensity is plotted using a linear scale. The spectra indicates that NiGe started to form when annealing at 250 °C and confirms that only NiGe phase was formed with annealing temperature over 275 °C.

above 275 °C, only the NiGe phase existed, and the lowest $R_{sh}$ of 2.8 Ω/□ was achieved at annealing temperatures of 450 and 500 °C. NiGe (111), (121), (120), (021), (211), (002), and (301) peaks can be observed (Fig. 4). When the anneal temperature was increased further to 600 °C, $R_{sh}$ increased to 4.3 Ω/□ due to the effects of agglomeration.[33]

A selective etching process for removing excess Ni was developed to enable integration of self-aligned NiGeSi/GaAs contacts for GaAs MOSFETs. Dilute HCl (1:10) could achieve good etching selectivity of Ni over nickel germanide and thus was employed to remove the unreacted Ni. The $R_{sh}$ values of NiGeSi/GaAs samples after the HCl etching are also shown in Fig. 3 (circle symbols). The $R_{sh}$ increased significantly to ~95 Ω/□ after the selective etching when the anneal temperature was below 225 °C. This is because some of the Ni was still unreacted and was removed by the subsequent HCl dip. However, Ni was completely consumed and nickel germanide ($Ni_5Ge_3$ and NiGe) was formed when the annealing temperature was over 250 °C, giving low $R_{sh}$ even after the selective etching step.

A two-step contact metallization process for Ohmic contact formation on $n^+$ GaAs was conceived. A brief dilute hydroflouric acid dip was performed to remove the native oxide of GeSi prior to e-beam deposition of Ni (~30 nm). A first anneal at the temperature of 250 °C was then performed to consume all of the Ni on GeSi by forming nickel germanide. Unreacted Ni on $SiO_2$ was subsequently selectively removed by hot HCl. After the first anneal, we found that the nickel germanide does not form an Ohmic contact to the underlying GaAs yet. A second high temperature RTA at 500 °C was then performed to convert the nickel germanide phases into the nickel monogermanide phase, which achieves an Ohmic contact with GaAs and a low $R_{sh}$.

Figure 1(a) shows the top-view of a TLM structure with NiGeSi contacts on $n^+$ GaAs. TEM analysis of a portion (A-A′) of the TLM structure (Fig. 5) clearly shows the polycrystalline structure of NiGeSi, which has a thickness of ~30 nm. No nickel germanide was observed on the $SiO_2$ region, indicating good selectivity of GeSi epitaxy. High resolution TEM image shows good uniformity of the NiGeSi and several grains of NiGeSi could be observed clearly, showing a distinct interface between NiGeSi and GaAs. Energy dispersive x-ray spectrometry (EDX) indicates the approximate NiGeSi composition ratio of Ni:Ge:Si =39.8:58.8:1.4. Secondary ion mass spectrometry (SIMS) analysis performed on the NiGeSi/$n^+$GaAs contact shows the elemental distribution of Ga, As, Ni, Ge, and Si, as plotted in Fig. 6. The gray dashed line represents the estimated NiGeSi/GaAs interface. The thickness of NiGeSi obtained using SIMS is quite consistent with that obtained from TEM (Fig. 5).

## III. ELECTRICAL CHARACTERISTICS AND DISCUSSION

After the first anneal at 250 °C and selective removal of unreacted Ni, the current-voltage (*I-V*) curve measured between two adjacent germanosilicide ($Ni_5Ge_3$, NiGe) contacts



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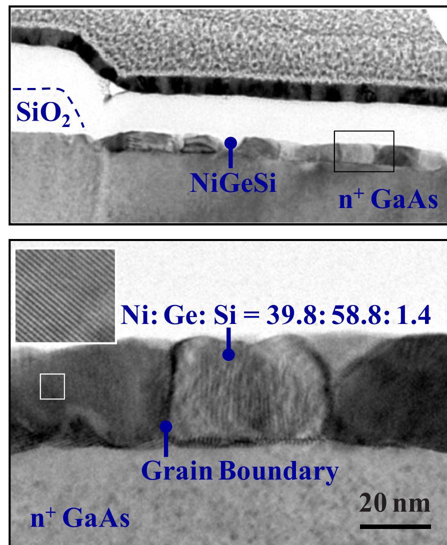


FIG. 5. (Color online) Cross-sectional TEM image (top) of TLM structure shows the formation of polycrystalline NiGeSi on n+ GaAs that is not covered by $SiO_2$. No Ge or NiGeSi was also observed on the $SiO_2$ region, which confirmed the selectivity of GeSi epitaxy. A zoomed-in view (bottom) showing several grains of NiGeSi. A high-resolution TEM image of a portion of a NiGeSi grain is shown on the inset.

in a TLM structure did not show Ohmic behavior. A second high temperature anneal at 500 °C converted the nickel germanide phases into a low resistivity nickel monogermanide phase, and probably helped to drive Ge and/or Si diffusion into GaAs. Ge has been also reported to dope GaAs heavily through interdiffusion between Ge and GaAs.[21] A Ge-rich GaAs interfacial layer right beneath the NiGeSi was also detected by EDX. Increasing the n-type doping concentration in GaAs can help to achieve good Ohmic contact with low $R_C$.

After the second anneal at 500 °C, an Ohmic contact was obtained, as shown in Fig. 7(a). *I-V* characteristics was measured between two adjacent NiGeSi/n+GaAs contact pads

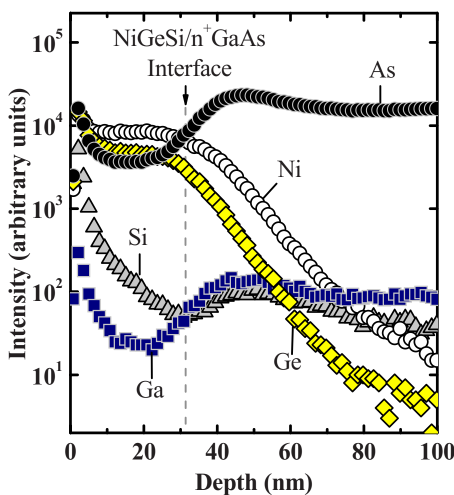


FIG. 6. (Color online) SIMS analysis of NiGeSi contact on n+ GaAs gives the elemental distribution. The interface between NiGeSi and GaAs is indicated by the dashed vertical line.

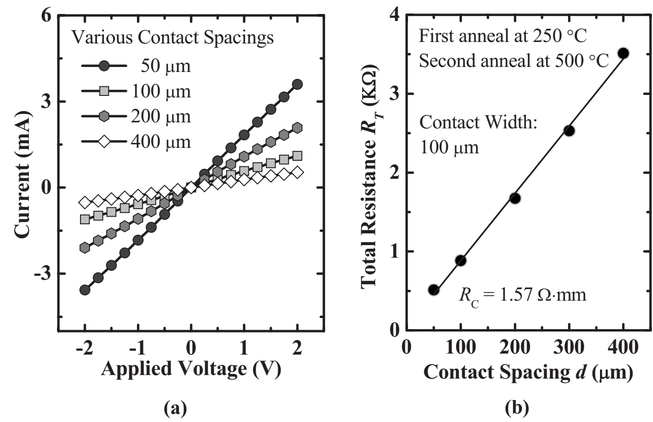


FIG. 7. (a) NiGeSi Ohmic contacts were formed on n+ GaAs using a two-step anneal process. *I-V* curves measured between NiGeSi contacts with different contact spacings *d* formed on n+ GaAs show excellent Ohmic behavior. (b) Plot of total resistance $R_T$ between two NiGeSi contacts as a function of the contact spacing *d*.

separated by various contact spacings *d*. The total resistance $R_T$ between two contacts decreases linearly with decreasing *d*. By plotting $R_T$ versus *d*, as shown in Fig. 7(b), one can extract the contact resistance $R_C$ from the intercept of the linear fitting line with the vertical axis and the sheet resistance $R_{sh,GaAs}$ of the doped substrate from the line slope. $R_C$ and $R_{sh,GaAs}$ were ~1.57 Ω mm and 852 Ω/□, respectively.

It should be noted that the $R_C$ is not optimized in this work, and further improvement is possible. Work function tuning of the contact metal, increasing the doping concentration of n+ GaAs, or forming an intermediate layer with smaller band gap could also be explored to reduce $R_C$.[34–36]

## IV. CONCLUSION

A self-aligned Ohmic contact metallization technology for GaAs was demonstrated. A continuous and single crystalline GeSi film was selectively grown on n+ GaAs for forming a NiGeSi-based contact using a two-step anneal. Ohmic contact behavior of NiGeSi on n+ GaAs regions was obtained. Contact resistivity $\rho_c$ as low as 1.57 Ω mm was achieved. The NiGeSi Ohmic contact technology is compatible and can be integrated in III-V MOSFETs for future high speed low power logic applications.

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