# A High-Performance Thin-Film Transistor with a Vertical Offset Structure

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***Abstract*—In this study, we propose a novel device structure combined with conventional hydrogenated amorphous silicon (a-Si:H) for the source and drain regions and microcrystalline silicon ($\mu$c-Si:H) for the channel region to obtain a high-performance thin-film transistor (TFT). This is a vertical a-Si:H offset structure used to suppress OFF-state current to a small value which is comparable to the conventional a-Si:H TFT's with a much higher drivability. The fabrication process is simple, low temperature ($\leq$ 300 °C), and low cost, with a potential for high reliability.**

## I. Introduction

RECENTLY, hydrogenated amorphous-silicon thin-film transistors (a-Si:H TFT's) have been investigated extensively for applications in large area switching devices such as active-matrix liquid crystal display (AM-LCD) [1], [2]. The most serious problems of present a-Si:H TFT's are the low field-effect mobility of carriers in the a-Si:H channel and the reliability. Thus the current driving capability is low. On the other hand, polysilicon (poly-Si) TFT's improve the current drivability while sacrificing the turn-off capability. Hence, there are many investigations for improving the turn-on characteristics of TFT's including double gate electrode [3], short channel device [4], and vertical structure [5]. For the improvement of drivability of poly-Si TFT's, an offset structure is proposed to reduce the OFF-current [6]. All of these technologies are complicated and costly. Meanwhile, a new crystalline material of higher band mobility (namely microcrystalline silicon, or $\mu$c-Si:H) is used to achieve high-speed TFT's [7]–[9]. Tsai *et al.* [10] proposed an $H_2$-dilution method to deposit a high-quality $\mu$c-Si film which is used in the $\mu$c-Si TFT's. Although a higher mobility than a-Si:H TFT's can be obtained, the OFF-currents of $\mu$c-Si:H TFT's are still very high; therefore, the ON/OFF current ratio is only five orders of magnitude or less. An offset structure is usually used to suppress the carrier conduction effectively due to the carrier trapping. In this letter, we propose a novel structure the channel of which is composed of $\mu$c-Si:H film while intrinsic a-Si:H film is an offset layer to improve the performance. The high conductance of the thin $\mu$c-Si:H layer can increase the ON-current and field-effect mobility and the vertical a-Si:H layer suppresses the OFF-current comparable to the conventional a-Si:H device.

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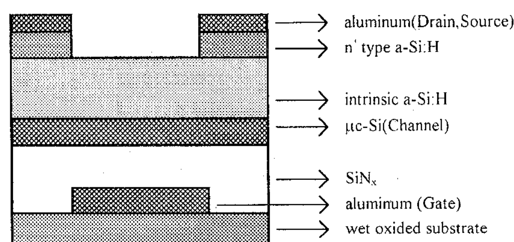


Fig. 1. A schematic diagram of the proposed novel thin-film transistor device.

## II. Experimental

Our novel device is shown schematically in Fig. 1. The fabrication process is similar to the conventional inverted stagger a-Si:H TFT's except for the insertion of a thin $H_2$-dilution deposited $\mu$c-Si:H film embedded between the gate insulator and undoped a-Si:H films. First, an aluminum film 250-nm thick is evaporated on a thermal oxide coated wafer and patterned to form the gate electrode by photolithography and wet etching. Secondly, silicon nitride, $H_2$-diluted $\mu$c-Si:H, undoped a-Si:H and $n^+$ a-Si:H films of 300-nm, 20-nm, 140-nm, and 70-nm thicknesses are deposited consecutively in a plasma enhanced chemical vapor deposition (PECVD) system without breaking the vacuum. The silicon nitride film is deposited at 300 °C, 27.78 mw/cm$^2$, 1 torr, while undoped and $n^+$ a-Si:H films are deposited at 250 °C, 25 mw/cm$^2$, 0.3 torr. Besides, $\mu$c-Si:H films are deposited at 250 °C, 0.55 torr, and 25 mw/cm$^2$ using the $[H_2]/\{[SiH_4]+[H_2]\}$ flow rate ratio values of 980 sccm/(20 sccm + 980 sccm) for 98% diluted film and 990 sccm/(10 sccm + 990 sccm) for 99% diluted film, respectively. The grain size of $\mu$c-Si:H after final processing was approximately 20 nm for 98% diluted film while was 18 nm for the 99% diluted film, respectively. Another aluminum film of 250-nm thickness is also evaporated and patterned to form source–drain electrodes by photolithography and wet etching processes. Finally, we use $CF_4$ plasma etching to define the device active region and remove the unwanted $n^+$ a-Si layer region. All the devices were annealed in 200 °C $N_2$ ambient for 25 min and the electrical properties of our TFT's are measured by a HP4145B semiconductor parameter measurement system with a PC system.

## III. Results and Discussions

Fig. 2 shows the transfer curves for different devices we made. All the devices have good performances such as small

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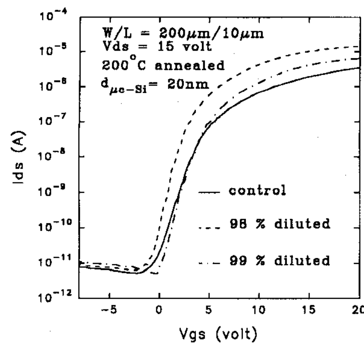
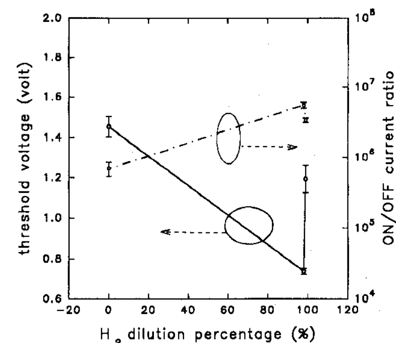
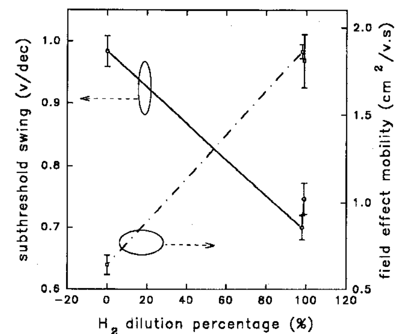



Fig. 2. Transfer characteristic of the proposed novel thin-film transistor device. Here $W$ is the channel width and $L$ is the channel length for our device.

threshold voltage and sharp transition region. The novel structure devices reveal higher current driving capabilities than the control device (conventional a-Si:H TFT's). Indeed, we can make sure that our novel device improves turn-on characteristics with little degradation due to the a-Si:H. On the other hand, turn-off characteristics will not degrade due to the presence of the a-Si:H layer. The a-Si:H layer behaves like two vertical offset regions to block the carrier conduction in the turn-off state, hence the OFF-current can be suppressed as the control device possesses. As shown in Fig. 2, it is found that 98% diluted device has a better performance over 99% diluted device. We believe that some ion-bombardment damages due to the $H_2$-plasma etching effect occur. These damages will produce new trap defects which enhance the trap assisted tunneling [11]. The large amount of $H_2$ dilution will increase the probability of trap defect formation. Hence, the 99% diluted device shows a smaller ON-current than 98% diluted one. In Fig. 2 and Fig. 3(a), the ON/OFF increases from $7 \times 10^5$ (0% diluted device) to $5.49 \times 10^6$ (98% diluted device) then drops to $3.36 \times 10^6$ (99% diluted device). The highest ON-current density is due to less bulk trap density. We have measured and deduced the density of deep gap states ($N_{\text{deep}}$) according to the equation: $N_{\text{deep}} = C_{\text{ins}} S (qkt)^{-1}$ decreases from $4.11 \times 10^{12}$ $cm^{-2}$ $ev^{-1}$ (0% dilution) to $2.54 \times 10^{12}$ $cm^{-2}$ $ev^{-1}$ (98% dilution) then increases to $2.87 \times 10^{12}$ $cm^{-2}$ $ev^{-1}$ (99% dilution), where $S$ is the subthreshold swing. From 0% to 98% $H_2$-plasma, the annealing effect prevails which fills the dangling bonds in the amorphous film. Then plasma damage occurs beyond 98% to 99% which produces more bulk trap density. This trend of trapped charge occurs simultaneously in the dielectric film. However, the interface trap is monotonically improved by $H_2$-plasma. The large amount of $H_2$ gas fills the growth ambient such that the growth rate for $\mu$c-Si:H is very slow. This produces a smooth interface between gate insulator and $\mu$c-Si:H. The 98% diluted device has a smaller threshold voltage of 0.74 V, due to less trapped charges, than 1.19 V for the 99% diluted one. In Fig. 3(b), the conductance of 98% diluted $\mu$c-Si:H film is superior to 99% diluted $\mu$c-Si:H film such that 98% $H_2$ diluted device has a higher field-effect mobility of 1.87 $cm^2/v \cdot s$, presumably due to less interface state scattering, than 99% diluted device of




(a)




(b)

Fig. 3. The dependence of $H_2$-dilution percentage on (a) threshold voltage, ON/OFF current ratio and (b) subthreshold swing, field-effect mobility of the proposed thin-film transistor device.

1.80 $cm^2/v \cdot s$ which are measured in the saturated region and deduced from the equation: $I_{ds} = \mu_{fe} C_{\text{ins}} W (V_{gs}\text{-}V_{th})^2 / 2L$. The subthreshold swing is also relative to the interface state. The smallest subthreshold swing value of 0.70 V/dec occurs on 98% diluted device which is less than that for the 99% diluted device of 0.75 V/dec. In conclusion, we have made the novel structure devices which demonstrate high performance over the conventional a-Si:H TFT's. The 20-nm thick $\mu$c-Si:H in our device operates well so far. It maybe further improved by optimizing the $\mu$c-Si:H thickness in the future.

## IV. Conclusion

We have proposed a novel vertical offset structure device for the first time to improve the thin-film transistor performance. A thin $H_2$-diluted $\mu$c-Si:H film is used to increase the turn-on driving current which can enhance operation speed while the vertical a-Si:H offset structure can suppress the OFF-current.

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