行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：☑個別型計畫　　□整合型計畫

計畫編號：NSC－89－2215－E－009－047

執行期間： 88 年 8 月 1 日至 89 年 7 月 31 日

計畫主持人：葉清發

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執行單位：國立交通大學電子工程系

中　華　民　國　89　年　10　月　29　日

行政院國家科學委員會專題研究計畫成果報告

低溫製作高移動率偏置型鋁閘極複晶矽薄膜電晶體

Fabrication of High Mobility Low Temperature Poly-Si Thin Film Transistor with Shifted Al-Gate

計畫編號：NSC 89-2215-E-009-047

執行期限：88 年 8 月 1 日至 89 年 7 月 31 日

主持人：葉清發 國立交通大學電子工程系教授

一、中文摘要

在第一個部份中，我們研究金屬致再結晶的關鍵技術並將它運用在複晶矽薄膜電晶體製程。從 X 光繞射儀（XRD）的譜線裡及拉曼位移譜線中我們驗證了再結晶膜的形成。此外，我們萃取了各種非晶矽薄膜的再結晶速率，希望能建立一個可讓往後製作薄膜電晶體時的參考資料庫。和傳統的 600℃ 固態結晶(SPC)技術比較起來，MILC TFTs 展現了極佳的元件特性。同時，我們也提出了一個新穎的技術，也就是利用雙閘極結構來防止側向結晶的結合邊界（Merging boundary）形成在元件通道中。這個技術大大改善了元件臨界電壓值（Threshold voltage）。另外，這個技術同時也能大幅降低汲極附近橫向電場而有效抑制了元件的漏電流而具有雙重優點。

在第二部分中，我們利用氘氣(deuterium)電漿以及氫氣電漿處理，作為金屬致再結晶複晶矽薄膜電晶體的缺陷填補技術。我們可以發現氫化處理以及氘氣處理均可有效改善元件特性，且改善幅度接近相同。這個結果可以歸因於矽與氘氣以及氫氣鍵結間的同位素效應(isotope effect)。

關鍵詞：薄膜電晶體、再結晶、矽化物

Abstract

In the first part, low-temperature (<550 ^{o}C) metal induced crystallization is investigated and applied to TFT's process. X-ray diffraction shows the prefer orientation of <1 1 1> for our MILC films and Raman microscopy reflects the poly-band after crystallization. Furthermore, crystallization rate for different films are also investigated and developed as a database for TFT's process. The MILC TFT's performs excellent characteristics as compare to conventional SPC method. A novel method is utilized to prevent merging boundary from locating in channel by dual gate structure thus improve the device performance. Besides, the leakage current is also sufficiently reduced by the same structure for the lowering of longitudinal electrical field near drain region.

In the second part, we utilized deuterium (D_2) plasma and hydrogen (H_2) plasma treatment to passivate defect densities. Both treatments improved device performance, but no clear difference can be distinguished for H_2-and D_2- plasma treated samples. This result can be attributed to the isotope effect between Si-H and Si-D bonds.

Keywords: TFT, Recrystallization, MILC, silicide

二、緣由與目的

Improving the device performance of low temperature processed (LTP) poly-Si TFT's is always an important issue in developing related technologies of active matrix liquid crystal display (AMLCD). In addition to growing a high quality gate oxide, improving the poly-Si channel layer is essential. Laser crystallization [1] or rapid thermal annealing [2] technology was developed to largely improve the quality of poly-Si channel layer, where the initial α-Si layer can be re-crystallized by way of exposure to high energy illumination. But both technologies usually suffer problems of expensive equipments, low throughput, and poor process tolerance.

Recently, a new technology of

metal-induced laterally crystallization (MILC) [3] had been paid much attention for the advantages of superior re-crystallization of α-Si layer, low temperature process (~500°C), one-way grain orientation and typical process equipments. In the technology, the metal atoms dissolved in α-Si film may weaken Si bonds and enhance nucleation of crystalline Si. Additionally, the metal silicide serves as a nucleus for Si crystallization. Nickel-disilicide ($NiSi_2$) was reported that there is less lattice mismatch with Si lattice [3], and thus it is superior to be the re-crystallization source.

In this paper, low-temperature (<550°C) Ni-metal induced lateral crystallization is investigated and applied to TFT's process. Raman microscopy is used to analyze the re-crystallized properties of α-Si film, and the electrical characteristics will be compared with conventional SPC poly-Si TFT's. Furthermore, the material properties of channel layer prior to re-crystallization are also investigated. The MILC-TFT's with different α-Si films deposited by SiH_4 or Si_2H_6 gas were processed and evaluated.

三、金屬致再結晶於不同複晶矽薄膜上的電性與物性探討；Material Effects of Silane and Disilane Gas for Low Temperature Metal-Induced Laterally Crystallized (MILC) Poly-Si TFT's

I. Device Fabrication

Low temperature co-planar MILC-TFT's are fabricated with a maximum processing temperature of 550°C. A 100nm-thick amorphous silicon layer was deposited as the active layer by LPCVD system using SiH_4 gas at 550°C or Si_2H_6 gas at 470 °C. After the active layer was patterned, samples were cleaned by RCA process and then soaked in liquid phase deposition (LPD) system. A 400 Å-thick LPD-oxide was deposited at 23°C as the gate insulator [4]. Samples were then treated with 5 minutes nitrous plasma in multi-chamber PECVD system for densification. Another 300nm-thick LPCVD amorphous silicon layer was deposited as gate electrode. After defining the gate geometry, a self-aligned phosphorous implantation with 2×10^{15} cm^{-2} doses was performed at 60keV to form the source, drain and gate doping regions. A 500nm-thick tetraethyl orthosilicate (TEOS) SiO_2 was deposited as the interlayer. After the contact holes were patterned, samples were deposited a 50 Å-thick Ni layer by dual E-gun system. The Ni layer was then patterned in contact hole by using lift-off method. Two-step furnace annealing was performed for the MILC process, where the dopants were instantaneously activated. Finally, a 500nm-thick aluminum layer was evaporated and patterned. Aluminum sintering was performed at 400°C for 30 minutes.

II. Result and Discussion

Figure 1 shows the process scheme of the two-step furnace annealing, where the nikel-disilicide ($NiSi_2$) is formed in step 1 at 400°C for 30 min, and performs crystallization toward to the channel in step 2 at 550°C for 24hr. The advantages of the above process scheme include that there is no need for extra mask and it is compatible with typical TFT's process. Figure 2 shows the Raman spectra of Ni-induced crystallized Si film annealed at 550°C for 15hrs with different α-Si films, which are deposited by SiH_4 or Si_2H_6 gas. The optical phonon peak of the transverse optical mode for the poly-Si is clearly observed at 519.7 cm^{-1}, which is near the crystalline band (520.5 cm^{-1}). It implies that both the SiH_4 and Si_2H_6 samples are re-crystallized by metal mediated nucleation. The signal peak of the Si_2H_6 sample is larger than that of the SiH_4 sample, which implies that the crystallized properties of the Si_2H_6 sample are much better than that of the SiH_4 sample. Figure 3 shows the transfer characteristics for both SiH_4 and Si_2H_6 deposited MILC-TFT's, where the conventional SPC poly-Si TFT is shown for comparison. The device performance is largely improved in the MILC-TFT's rather than the SPC poly-Si TFT. The inset indicates the transconductance for all samples. The Si_2H_6 processed MILC-TFT shows the largest mobility as compared to the other two samples. It is well known that SPC poly-Si has a columnar grain structure with grain boundaries randomly oriented with

respect to the direction of I_{DS} [5]. These grain boundaries trap carriers and build up potential barriers to the flow of carriers. When the device is turned on, conducting carriers will be scattered by this potential barrier, thus degrading the carrier mobility. These problems are eliminated in the MILC-TFTs because silicide-improved lateral crystallization can effectively control the location of grains in the longitudinal direction. While longitudinal grains and their boundaries (LGGB's) are largely parallel to I_{DS}, hence less impeding to carrier flow and resulting in lower Vth, smaller subthreshold swing, and higher mobility [6]. The reason why the Si_2H_6 sample shows a better performance than the SiH_4 sample can be suggested that the Si_2H_6 deposited α-Si film will be re-crystallized easier than the SiH_4 deposited α-Si film under the same annealing temperature because the former has a rougher α-Si structure. A rougher α-Si film can be easily rearranged or re-crystallized. The earlier literatures [7] reported that the higher disorder contained in film, the more difficult it will be to form the nucleation sites, but the larger grain size will it result. It implies that the Si_2H_6 deposited α-Si film has the higher re-growth rate than the SiH_4 deposited α-Si film. Table I summarizes the characteristic parameters for both the SiH_4 and the Si_2H_6 deposited MILC-TFT's, where the SPC TFT is also compared. The Si_2H_6 sample has smaller trap state densities (N_t) than the SiH_4 sample, which can be due to the better-crystallized properties in the Si_2H_6 sample rather than the SiH_4 sample. The carrier mobility of the MILC-TFT's is dramatically improved from 7.7 to 45 (cm2/v.sec) as compared to the SPC poly-Si TFT. The characteristic parameters are continuely improved from the SiH_4 sample to the Si_2H_6 sample.

四、使用雙閘極結構來製作金屬致再結晶薄膜電晶體；A Smart "U-Shape" Double-Gate Structure for Metal-Induced Laterally Crystallized (MILC) Poly-Si TFT's

I. Device Fabrication

Low temperature co-planar MILC-TFT's are fabricated with a maximum processing temperature of 550°C. A 100nm-thick amorphous silicon layer was deposited as the active layer by LPCVD system using SiH_4 gas at 550°C. After the active layer was patterned, samples were cleaned by RCA process and then soaked in liquid phase deposition (LPD) system. A 400 Å-thick LPD-oxide was deposited at 23°C as the gate insulator [8]. Samples were then treated with 5 minutes nitrous plasma in multi-chamber PECVD system for densification. Another 300nm-thick LPCVD amorphous silicon layer was deposited as gate electrode. After defining the gate geometry, a self-aligned phosphorous implantation with 2×10^{15} cm^{-2} doses was performed at 60keV to form the source, drain and gate doping regions. A 500nm-thick tetraethyl orthosilicate (TEOS) SiO_2 was deposited as the interlayer. After the contact holes were patterned, samples were deposited a 50 Å-thick Ni layer by dual E-gun system. Then nickel was patterned only in the source and drain surfaces. Two steps furnace annealing were utilized to form $NiSi_2$ in step 1 at 400°C, and start re-crystallization in step 2 at 550°C, where the dopants were activated instantaneously. Finally, a 500nm-thick aluminum layer was evaporated and patterned. Aluminum sintering was performed at 400°C for 30 minutes.

II. Result and Discussion

Comparing those typical characteristic parameters for conventional SPC poly-Si TFT's and MILC-TFT's [5], the device performance such as field effect mobility (from 7.7 to 45.8 cm^2/v·sec), threshold voltage (from 11.89 to 1.28 V) and ON/OFF current ratio (from $8x10^5$ to $4.7x10^6$) has been largely improved due to the metal-induced lateral re-crystallization. Rather than the random oriented grain growth in conventional SPC poly-Si TFT's, the MILC-TFT's exist a regular one-way grain orientation [9] and perform superior electrical characteristics. Figure 4 shows the optical microscopy (OM) image of the metal-induced laterally re-crystallized process, where the □-Si layer is gradually re-crystallized with the annealing time. The

bright field is the re-crystallized region, while the dark part is still the amorphous state. In the figure, both crystallization fronts tend to merge at the center of the channel. At the top of the OM image, the cross-sectional view of a MILC-TFT is shown for comparison. Ni source is deposited at the source/drain contact hole region, and $NiSi_2$ pattern is then formed and re-crystallized toward the channel direction via the two-step annealing processes (400°C and 550°C) [5]. One of the advantages in our MILC process needs no extra mask, and it is therefore compatible with typical TFT processes.

Since both crystallization fronts merge at the center of the channel and form the merging boundary. The device characteristics of the MILC-TFT's could be more or less affected and unpredictable. The merging boundary consists of metal-silicide residues, and represents the combination of two oriented grains. It certainly contains large amounts of dangling bonds, and could be considered as a large and transverse grain boundary [10]. From the viewpoint of energy, the merging boundary will trap conducting carriers and serve as a potential barrier, which will be harmful to the MILC-TFT's performance.

In our work, a smart "U-shape" double-gate structure was designed not only to prevent the re-crystallization fronts merging at the center of the channel, but also to reduce the leakage current. Figure 5 shows the top-view of a "U-shape" double-gate MILC-TFT. The corresponding cross-sectional view is shown in Fig. 6. It is similar to conventional double-gate TFT's, but the changed is the pattern of active layer instead of gate electrode. Both $NiSi_2$ fronts from opposite Source/Drain pads lead the crystallization along the "U-shape" pattern, and merges away from channel region. If the conventional single-gate structure is adopted, both $NiSi_2$ fronts will merge at the center of the channel, which will result in an unpredictable variation in TFT performance. In addition, the extra bonus is that the large electrical field near drain junction can be half reduced because the "U-shape" structure undoubtedly behaves as a real double gate [11]. Thus, the leakage current is effectively controlled.

Figure 7 shows the transfer characteristics of the MILC-TFT's with a "U-shape" structure and a conventional single-gate structure. The leakage current is reduced two order of magnitude at V_{GS}= -10V, which is due to the reduction of electric field near drain junction. V_{th} is reduced 35%, which can be attributed to the elimination of the metal-silicide merging boundary [6]. When the singal-gate MILC-TFT's turn on, the merging boundary traps conducting carriers, which finally leads to an increase of threshold voltage. The inset Table in the Fig. 7 clearly shows the improvements in ON- and OFF-states.

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六、圖表

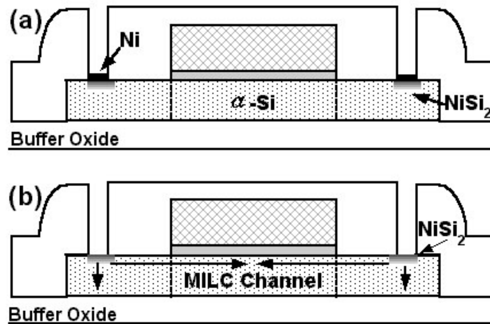

Fig. 1

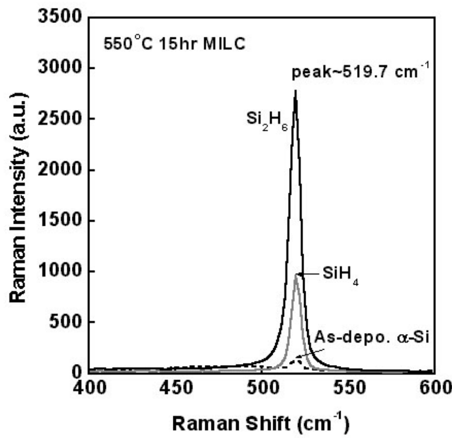

Fig. 2

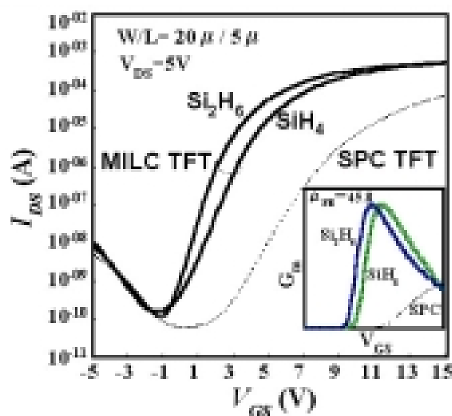

Fig. 3

TFT	Swing (V/dec)	I_{on}/I_{off} (10^6)	V_{th} (V)	μ_{FE} ($cm^2/V\cdot sec$)	N_t (cm^{-2})
SiH_4	0.76	3.8	2.22	45.5	3.1×10^{12}
Si_2H_6	0.64	4.7	1.28	45.8	2.0×10^{12}
SPC	1.71	0.8	11.9	7.7	1.3×10^{13}

Table I

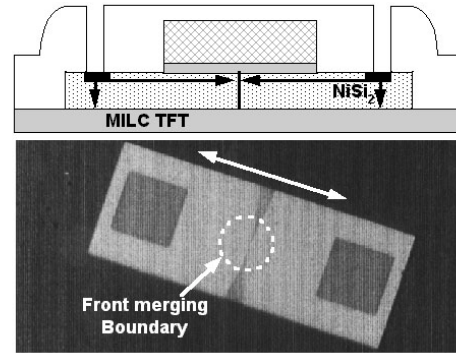

Fig. 4

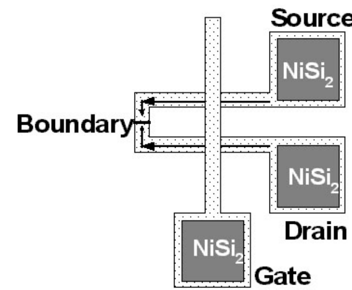

Fig. 5

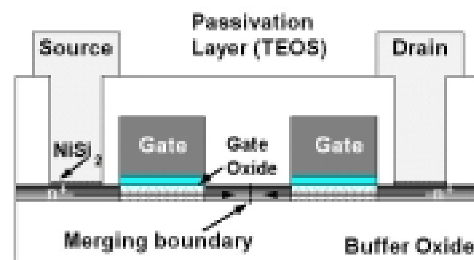

Fig. 6

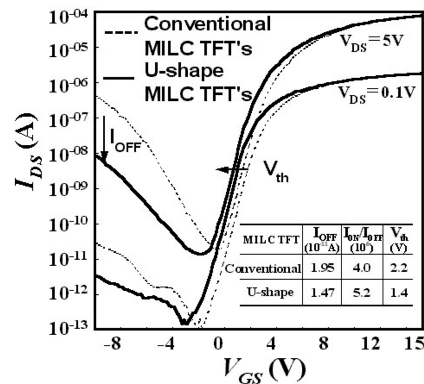

Fig. 7