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Integration schemes and enabling technologies for three-dimensional integrated circuits

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Abstract: Various integration schemes and key enabling technologies for wafer-level three-dimensional integrated circuits (3D IC) are reviewed and discussed. Stacking orientations (face up or face down), methods of wafer bonding (metallic, dielectric or hybrid), formation of through-silicon via (TSV) (via first, via middle or via last) and singulation level (wafer-to-wafer or chip-to-wafer) are options for 3D IC integration schemes. Key enabling technologies, such as alignment, Cu–Cu bonding and TSV fabrication, are described as well. Improved performance, such as lower latency and higher bandwidth, lower power consumption, smaller form factor, lower cost and heterogeneous integration of disparate functionalities, are made possible in the next generation of electronics products with the realisation of 3D IC.

1 Introduction

In recent decades, higher performance, smaller form factor and lower cost are a few basic requirements in electronic products to meet insatiable consumer needs and to survive in an increasingly competitive market. Conventional integrated circuits (IC) are fabricated on planar silicon wafers and therefore the level of integration is limited to a two-dimensional (2D) plane. To meet IC growth as described by Moore's law [1], chip makers are doubling the number of transistors per unit chip area in every 18–24 months which results in historical performance improvement in IC. Going forward, however, this scaling path is facing with fundamental and economic barriers. The gate length and gate dielectric thickness of the transistor are both approaching the physical limits rendering a non-commensurate improvement in transistor performance. The introduction of various performance boosters, such as strain engineering and high-k/metal gate, has been highly successful but at a higher cost and complexity. Higher leakage current in the transistors has also increased the overall power consumption in IC. Migration to a new technology node has also placed tremendous economic pressure on the chip makers as the fab cost is skyrocketing. It is a consensus in the industry that when conventional planar IC is unable to meet future demands, a paradigm shift to explore the vertical dimension in 3D IC is a promising path.

Even though dimensional scaling improves the device performance in terms of gate switching speed, it has a reverse effect on global interconnect latency [2]. In addition, the global interconnect may dominate the operating frequency in some cases. Three-dimensional integration is one of the options that can potentially meet the future projection described by Moore's law and provides a solution to the latency issue in long global interconnects. In 3D IC, large chip can be partitioned into smaller blocks, vertically stacked and interconnected as shown in Fig. 1 to shorten the global interconnect length and improve the signal propagation delay.

Another bottleneck in future computing power is related to the 'memory wall' challenge. As the computing power in processor increases in each generation, the limited bandwidth (due to pin count limitation) between processor core and main memory places a severe limitation on the overall system performance [3]. The problem is even more pressing in multi-core architecture as every core will demand for data supply. To close this gap, the most direct way is to shorten the connections and to increase the number of data channels. By placing memory directly on processor, the close proximity shortens the connections and the density of connections can be increased by using more advanced complementary metal-oxide semiconductor (CMOS) processes (as opposed to packaging/assembly processes) to achieve fine-pitch through-silicon via (TSV). This massively parallel interconnection is shown in Fig. 2 and it is popularly touted as a way to combat the memory wall challenge in future micro-processors.

The basic concept of 3D integration is the IC with more than one plane of devices and metals, connected by vertical interconnects (TSVs), as shown in Fig. 3. The bonding interface between the IC layers provides mechanical support and electrical connections in 3D IC. This 3D architecture provides a remedy to latency and memory wall issues as described above. Besides, 3D integration scheme can integrate different IC layers that are fabricated from their respective optimum processes without the need to use complicated and serial fabrication flow which may lower the efficiency and the yield [4–6]. This allows heterogeneous integration of disparate chips, such as IC (digital or analogue), memory,

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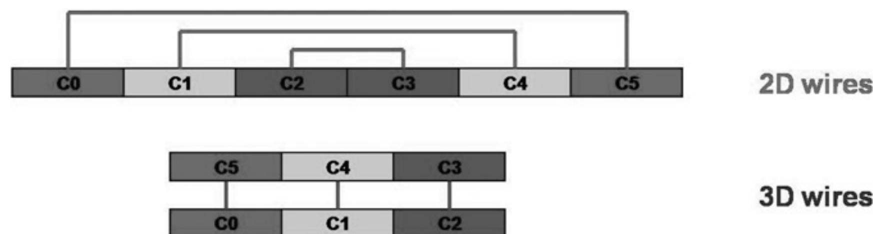

Fig. 1 *Long global wires on IC can be shortened by chip partitioning and stacking*

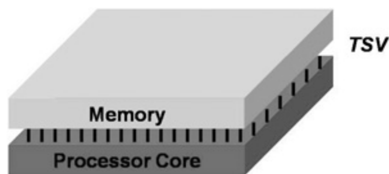

Fig. 2 *Direct placement of memory on processor improves the data bandwidth*

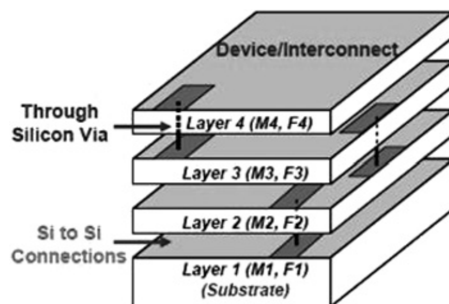

Fig. 3 *Concept of three-dimensional integration*

microelectromechanical system (such as sensor), photonics and so on, to achieve functional diversification in future integrated systems.

Although 3D integration has a long string of advantages, challenges such as reliability, heat dissipation, test methodology and supply chain are currently being identified as the most urgent ones that need to be solved for full realisation of 3D IC. This paper reviews and provides a summary on the emerging area of wafer-level 3D IC. The contents focus on various 3D integration schemes and also describe key enabling platform technologies. The intent is to provide information and references for researchers who are interested in this exciting field.

2 Classification of wafer-level 3D integration technology

The basic concept of 3D integration is the IC with more than one plane of devices and metals, connected by vertical interconnects. This provides another dimension for IC integration and one is along limited to the $X-Y$ plane anymore. Given the long list of benefits offered by 3D IC as briefly described above, a wide range of new applications can now be made possible.

Over the years, the rapid development in 3D IC research and development has resulted in a myriad of architectures and forms for 3D IC. Classification of 3D IC is therefore not a straightforward endeavour as there is no clear boundary between 3D packaging and wafer-level 3D IC. In general, wafer-level 3D integration is different from 3D package technology in terms of interconnect density, infrastructures and application drivers. 3D package technology focuses on final chip/die stacking after the completion of foundry processes. On the other hand, processes in wafer-level 3D integration such as TSV formation is completed as part of the foundry processes. As a number of fundamental concepts of wafer-level 3D integration technologies are similar as those of 3D packaging, this paper will only focus on wafer-level 3D integration. Broadly, wafer-level 3D integration can be classified into different categories based on the following differentiators:

Singulation level: chip-to-chip, chip-to-wafer or wafer-to-wafer;
Stacking orientation: face-to-face or back-to-face stacking;
Bonding medium: metal-to-metal, dielectric-to-dielectric (oxide, adhesive etc.) or hybrid bonding;
TSV formation: via first, via middle or via last;
Wafer types: bulk, silicon-on insulator (SOI) or glass wafers.

2.1 Singulation level

Depending on the level of chip singulation, 3D integration can take place at three different stages: chip-to-chip, chip-to-wafer and wafer-to-wafer stacking. In wafer-level 3D integration, permanent bonding can be done either in chip-to-wafer (C2W) or wafer-to-wafer (W2W) stacking. A comparison of these two methods is summarised in Table 1. As shown in Fig. 4, the option of C2W or W2W depends on two key requirements on chip size and alignment accuracy. When high precision alignment is desired in order to achieve high density layer-to-layer interconnections, W2W is a preferred choice to maintain acceptable

Table 1 Comparison between wafer-to-wafer and chip-to-wafer stacking

	Wafer-to-Wafer	Chip-to-Wafer
wafer/die size	wafer/die of common size in order to avoid silicon area wastage	dissimilar wafer/die size is acceptable
throughput	wafer scale	die scale
yield	lower than lowest yield wafer, therefore high yield wafer must be used	known good die can be used if pre-stacking testing is available
alignment accuracy	<2 μm global alignment	~ 10 μm for >1000 dph <2 μm for <100 dph

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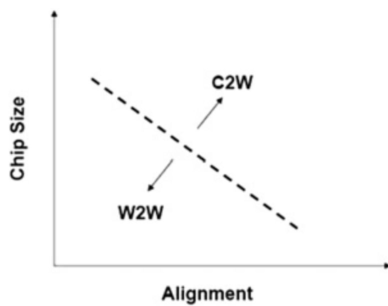

Fig. 4 *Choice between C2W and W2W depends on the chip size and the required alignment accuracy*

throughput by performing a wafer-level alignment. W2W is also preferred when chip size gets smaller.

2.2 Orientation of wafer stacking

Based on the stacking orientation of two device wafers, there are two different ways of wafer stacking: face-to-face (F2F) and face-to-back (F2B). The effects of wafer stacking orientation are clearly seen in terms of circuit symmetry, fabrication complexity, capacitance of interconnection and alignment consideration. Both types of stacking methods have been applied in 3D integration applications. A combination of stacking orientations in 3D integration is also possible [7].

2.2.1 Face-to-face: In face-to-face (or 'face down') stacking orientation, two wafers are aligned and bonded such that the circuitries are facing each other as shown in Fig. 5. From the fabrication technology point of view, this type of integration is easy to apply and does not require an additional handle wafer. However, the circuit symmetry aspect needs to be taken into consideration at the design stage. During the design stage of the top circuit, the action of circuit mirroring is required. At the same time, the symmetry and proper placement of alignment marks on both wafers should be carefully considered as well.

2.2.2 Face-to-back: For face-to-back (or 'face up') wafer stacking, the top wafer (or upper wafer) should be thinned from the substrate while the wafer's front side is temporarily attached to an additional handle wafer. When the required final thickness of the top wafer is achieved, it is bonded to the substrate wafer and the handle wafer is released. Comparing with the face-to-face version, this approach increases the process complexity. However, the wafer-to-wafer symmetric issues are eliminated. When the handle wafer used is transparent and the wafer is sufficiently thinned, the alignment process becomes transparent and much easier. This scheme is shown in Fig. 6.

2.3 Methods of wafer bonding

Bonding technology is a key technology in 3D integration, both in wafer-level and chip-level. This process allows two or more IC layers stacking in the *Z*-direction. Based on the bonding medium, wafer bonding can be achieved via several options:

2.3.1 Metal-to-metal: Metal-to-metal bonding is an attractive technique that provides (i) mechanical support that holds IC layers together, (ii) electrical connections between IC layers and (iii) thermally conductive path to assist heat removal in 3D IC. These characteristics are due to the excellent properties of the metal used in bonding. Copper, tin and gold are the usual metals of choice in metal bonding [8–11]. Copper is the most popular and natural choice of metal for 3D IC bonding since it is the material used in the formation of back-end interconnects in standard CMOS process [8, 9]. Metal bonding is usually accomplished via parallel application of heat and contact pressure between two wafers, this process is commonly known as thermo-compression bonding. The bonding temperature during metal-to-metal bonding is limited by the thermal budget of existing devices and circuits and therefore low temperature metal bonding is an active area of research. Discussion on Cu–Cu bonding will follow in Section 3.2

2.3.2 Oxide-to-oxide: Since silicon oxide is the standard dielectric material used in semiconductor processing, this material naturally becomes the choice as the bonding medium [12–15]. The advantage of silicon oxide bonding is that it is CMOS process compatible and one can achieve high interconnect stacking density when an SOI wafer is used. Unlike thermo-compression bonding, oxide-to-oxide bonding is accomplished via fusion bonding of hydrophilic surface at room temperature and atmospheric ambient followed by thermal annealing to strengthen the bond. The throughput is higher as fusion bonding can be completed in a much shorter duration. However, the oxide surfaces of

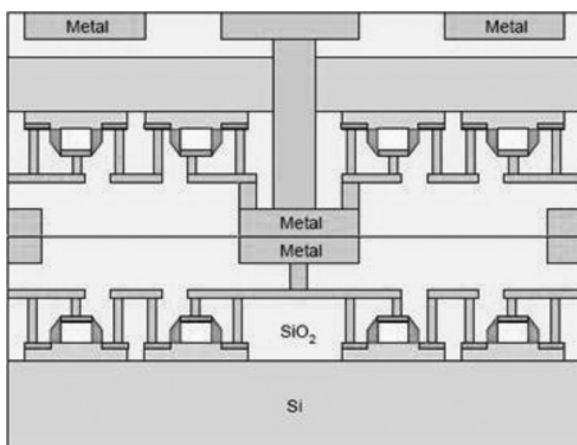

Fig. 5 *Face-to-face wafer stacking*

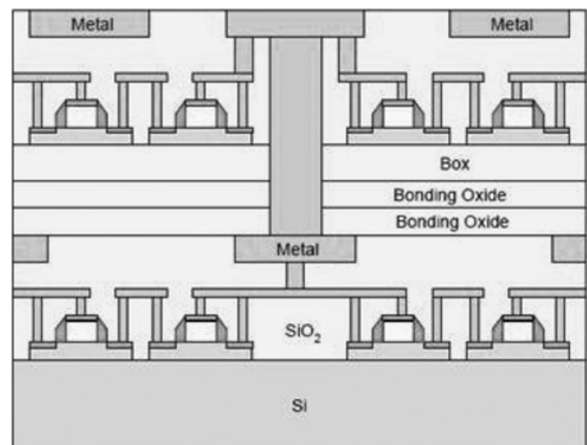

Fig. 6 *Face-to-back wafer stacking*

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both wafers must be extremely clean and flat; usually an extra processing step (planarisation) is required.

2.3.3 Polymer-to-polymer: Polymer-to-polymer bonding technique, such as using benzocyclobute (BCB), has better adhesive strength because the polymer material is more compliant than silicon oxide [16–20]. This advantage is significant for wafer-level bonding. Besides, this method is also more forgiving in terms of surface cleanliness and particles control. However, the fusion point or glass transition temperature (T_g) of polymer is usually lower than 400°C, which restricts the subsequent process temperature. The use of polymer could be problematic as the polymer may pollute other wafers or instruments due to decomposition.

The types of wafer bonding potentially suitable for wafer-level 3D integration are depicted in Fig. 6. Dielectric-to-dielectric bonding is most commonly accomplished using silicon oxide or BCB polymer as the bonding medium. These types of bonding provide primary function as a mechanical bond and the inter-wafer via is formed after wafer-to-wafer alignment and bonding (Fig. 7*a*). When metallic copper-to-copper bonding is used (Fig. 7*b*), the inter-wafer via is completed during the bonding process; note that appropriate interconnect processing within each wafer is required to enable 3D interconnectivity. Besides providing electrical connections between IC layers, dummy pads can also be inserted at the bonding interface at the same time to enhance the overall mechanical bond strength. This bonding scheme inherently leaves behind isolation gap between Cu pads and this could be a source of concern for moisture corrosion and compromise the structural integrity especially when IC layers above the substrate is thinned down further. Fig. 7*c* shows a bonding scheme utilising a hybrid medium of dielectric and Cu. This scheme in principle provides a seamless bonding interface, which consists of dielectric bond (primarily a mechanical bond) and Cu bond (primarily an electrical bond). However, very stringent requirements with regards to surface planarity (dielectric and Cu) and Cu contamination in the dielectric layer due to misalignment are needed.

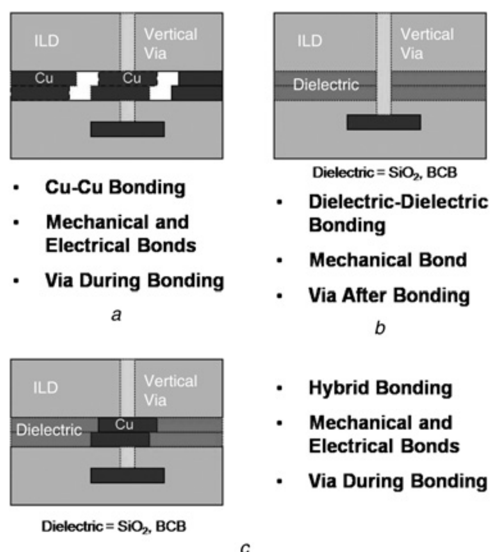

Fig. 7 *Wafer bonding techniques for wafer-level 3-D integration*

a Dielectric-to-dielectric
b Metal-to-metal
c Dielectric/metal hybrid

2.4 TSV formation

TSV is the vertical electrical interconnection for ICs on different planes. Forming TSV usually involves drilling a via in the wafer and filling conductance into the via. The order of TSV fabrication and insertion in a 3D IC process is related to interconnect density, material selections and applications. TSV can be formed at various stages during the 3D IC process as shown in Fig. 8. When TSV is formed before any CMOS processes, the process sequence is known as 'via first'. One is restricted to use materials such as doped poly-Si as the conductor material for TSV filling in view of the subsequent high temperature front-end processes. It is also possible to form the TSV when the front-end processes are completed. In this 'via middle' process, back-end processes will continue after the TSV process is completed. When TSV is formed after the CMOS processes are completed, it is known as 'via last' process. TSV can be formed from the front side or the back side of the wafer.

The above schemes have different requirements in terms of process parameters and materials selection. The choice depends on final application requirements and infrastructures in the supply chain. Via first and via middle approaches offer higher TSV density compared to the via last approach. In the via middle and via last approaches, Cu plating can be used to fill the TSV resulting in more conductive TSV.

2.5 Wafer types

2.5.1 Bulk Si: Most commonly, bulk Si wafer is used in wafer-level 3D IC integration. Besides the cost factor, the process maturity is another main reason for the wide spread use of bulk wafer for 3D IC application. Even when other types of wafers are used as the top wafer, the bottom substrate wafer is almost exclusively bulk wafer.

2.5.2 Silicon-on insulator (SOI): SOI wafer, with a buried oxide layer, can be thinned uniformly to achieve ultra-thin silicon layer because the buried oxide layer acts as an etch stop layer [7]. The etching process usually consists of a combination of mechanical grinding, chemical–mechanical planarisation (CMP), wet etching and dry etching. Most importantly, because the final thickness can be uniformly thin, the use of SOI wafer can potentially achieve high density interconnect for 3D IC. The SOI structure also offers good latch-up immunity [21]. However, the ESD capability might be compromised in the 3D-stacked structures and the dense device layers have potential heat dissipation concern.

2.5.3 Glass: The role of a glass wafer in 3D integration is usually as the temporary carrier to hold the top wafer during thinning and handle in a back-to-face wafer stacking

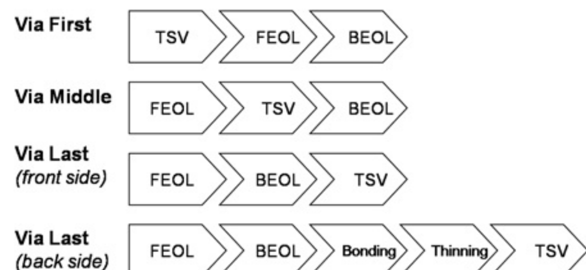

Fig. 8 *TSV can be formed at various stages of IC processing*

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process. Therefore the glass wafer for this purpose is also called a handle wafer. After the top wafer is temporarily attached to the glass wafer using adhesive, the substrate of the top wafer can be thinned to the required thickness. Finally, the glass wafer is removed after the thinned top wafer is bonded to the bottom substrate wafer. Using glass wafers also offers good alignment capability because of the transparent characteristic of glass.

3 Key enabling technology for wafer-level 3D IC integration

Wafer-level 3D IC integration is a novel concept to increase the circuit density and reduce the form factor. 3D IC can be realised in a variety of forms with a number of enabling techniques. In this section, the three most important key enabling technologies are introduced and discussed.

3.1 Alignment

Poor alignment leads to circuit malfunction or degradation in reliability. Therefore alignment tolerance dominates the contact area and the yield of 3D IC stacking. The accuracy of alignment correlates to the design of aligner and alignment marks. It is also decided by the experience of the operator. Alignment overlay can usually be enhanced by aligning two live images directly as enabled by infrared (IR) transmission or the use of transparent substrate. Fig. 9 shows an example of IR image showing typical misalignment results [22]. Another method is indirect alignment of a live image to a stored image.

3.2 Copper wafer bonding

Copper is widely used as the metal of choice for interconnects in mainstream CMOS fabrication. Therefore copper lends itself as the natural candidate to from the connections between two device layers or wafers in 3D IC. Technically, the principle of copper wafer bonding is based on thermo-compression bonding via parallel application of heating and contact pressure to bond two wafers using Cu as the bonding medium. During bonding, copper atoms from the Cu thin layers on two wafers inter-diffuse and out of plane grain growth is promoted. When the process is properly optimised, the two Cu layers fuse together to form a homogeneously bonded Cu layer. The quality of the bonded Cu interconnects can be correlated to the cleanliness of the wafer surface and the bonding process parameters (such as temperature and duration).

The author (K.N. Chen) has conducted a series of detailed fundamental researches about Cu bonding at MIT, IBM and NCTU. Generally, bonding temperature of at least ~300–400°C is required to complete the copper bonding. This temperature range is usually required to overcome surface oxide barrier on the Cu surface in order to achieve complete bonding in a reasonable time scale. Although high temperature and pressure may improve the bonding quality, the corresponding cost and possible degradation of device characteristics are major concerns. Therefore low temperature and pressure bonding method is essential for 3D integration [8, 9]. Fig. 10 shows the scanning electron microscopy (SEM) image of Cu interconnect bonding to Cu pad [22].

There is strong motivation to move the bonding temperature to even lower range primarily from the point of view of thermal stress induced due to coefficient of thermal expansion (CTE) mismatch of dissimilar materials in a multi-layer stack and temperature swing. A number of approaches have been explored:

1. *Surface activated bonding* [23]: In this method, a low energy Ar ion beam is used to activate the Cu surface prior to bonding. Contacting two surface-activated wafers enables successful Cu–Cu direct bonding. The bonding process is carried out under an ultra-high vacuum (UHV) condition. No thermal annealing is required to increase the bonding strength. Tensile test results show that high bonding strength equivalent to bulk material is achieved at room

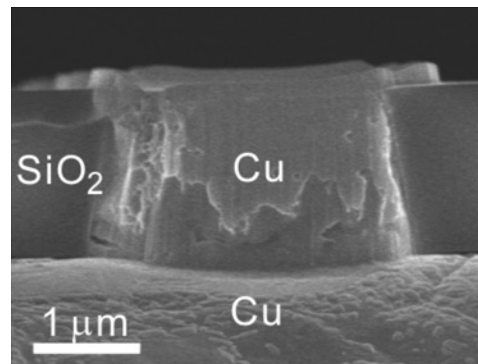
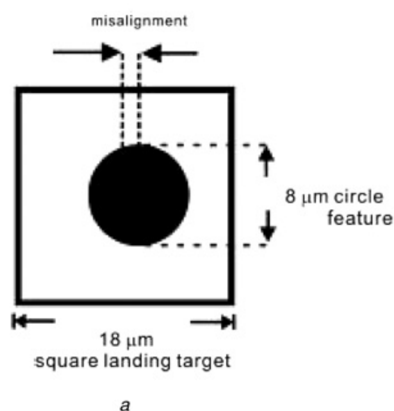


Fig. 10 *SEM image of Cu interconnect bonding to Cu pad [22]*



a

b

Fig. 9 *Example of IR image showing typical misalignment results [22]*

a Schematic diagram
b IR image

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temperature. In [24], adhesion of Cu–Cu bonded at room temperature in UHV condition was measured to be about ~3 J/m^2 using atomic force microscopy tip pull-off method.
2. *Cu nanorod* [25]: Recent investigation on surface melting characteristics of copper nanorod arrays shows that the threshold of the morphological changes of the nanorod arrays occurs at a temperature significantly below the copper bulk melting point. With this unique property of the copper nanorod arrays, wafer bonding using copper nanorod arrays as a bonding intermediate layer is investigated at low temperatures (400°C and lower). Silicon wafers, each with a copper nanorod array layer, are bonded at 200–400°C. The FIB/SEM results show that the copper nanorod arrays fuse together accompanying by a grain growth at a bonding temperature of as low as 200°C.
3. *Solid–liquid inter-diffusion bonding* (SLID) [26]: This method involves the use of a second solder metal with low melting temperature such as tin (Sn) in between two sheets of Cu with high melting temperature. Typically a short reflow step is followed by a longer curing step. The required temperature is often slightly higher than Sn melting temperature (232°C). The advantages of SLID are that the inter-metallic phase is stable up to 600°C and the requirement of contact force is not critical.
4. In the DBI™ technology described in [27], a moderate post-oxide bonding anneal may be used to effect the desired bonding between Cu. Owing to the difference in coefficient of expansion between the oxide and Cu and the constraint of the Cu by the oxide, Cu compresses each other during heating and metallic bond can be formed.
5. Direct Cu–Cu bonding at atmospheric pressure is investigated by researchers at LETI [28]. By means of CMP, the roughness and hydrophily (measure by contact angle) of Cu film are improved from 15 to 0.4 nm and from 50 to 12°. Blanket wafers were successfully bonded at room temperature with impressive bond strength of 2.8 J/m^2. With a post-bonding annealing at 100°C for 30 min, the bonding strength was improved to 3.2 J/m^2.
6. A novel Cu–Cu bonding process has been developed and characterised to create all-copper chip-to-substrate input/output (I/O) connections [29]. Electroless copper plating followed by low temperature annealing in a nitrogen environment was used to create an all-copper bond between copper pillars. The bond strength for the all-copper structure exceeded 165 MPa after annealing at 180°C. While this technique is demonstrated as a packaging solution, it is an attractive low temperature process for Cu–Cu bonding;
7. In the author's (C.S. Tan) research group at Nanyang Technological University, a method of Cu surface passivation using self-assembled monolayer (SAM) of alkane-thiol has been developed. This method has been shown to be effective to protect the Cu surface from particle contamination and to retard surface oxidation. The SAM layer can be thermally desorbed in situ in the bonding chamber rather effectively hence providing clean Cu surface for successful low-temperature bonding. Cu wafers bonded at 250°C present significant reduction in micro-void and substantial Cu grain growth at the bonding interface [30–32].

3.3 TSV process

Fig. 11 is a generic process flow of TSV fabrication flow using Cu as the core metal. It begins with high aspect ratio deep etching of Si. Dielectric liner layer is then deposited on the via sidewall followed by barrier and Cu seed layers deposition. Liner layer, which is made of dielectric layer such as silicon dioxide, provides electrical isolation between Cu core and Si substrate. The liner thickness must be chosen appropriately to control leakage current and capacitance between Cu core and Si substrate. Cu super conformal filling is then achieved with electro-plating process. Super conformal filling is required to prevent void formation in the Cu TSV. Finally, Cu over-burden is removed by chemical mechanical polishing. Fig. 12 shows an image of high aspect ratio TSVs [33]. More information on TSV fabrication can be found in literatures such as [34, 35].

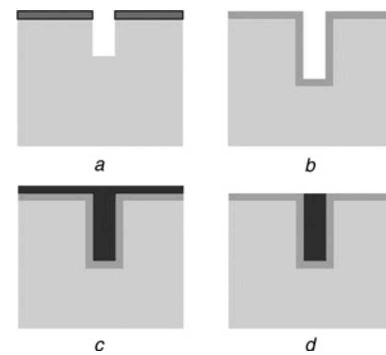

Fig. 11 *Generic process flow of Cu-filled TSV fabrication*

a High aspect ratio Si deep etching
b Linear deposition followed by barrier and seed layers deposition
c Super conformal Cu filling
d Removal of Cu over-burden

Copper, tungsten and poly-silicon are typical options as filling materials for TSV. Among these materials, copper and tungsten can be used after the front-end processes, while poly-silicon can be used in the via-first process. TSV filled with Cu has better electrical performance due the lower resistivity of Cu. Cu filling in high aspect ratio via hole using electroplating is usually very challenging due to non-conformal filling (which results in voids formation) and slow filling rate. Excessive Cu over-burden requires post-filling polishing. The industry has made significant progress in process optimisation in the last several years. Recent progress in alternative filling method such as electro-grafting has attracted a lot of interest. TSV filled with Cu suffers from severe thermo-mechanical stress due to the large mismatch in CTE between Cu and Si. This issue can cause variation in device characteristics in the proximity of the TSV as well as mechanical integrity of 3D IC. This issue needs to be studied carefully.

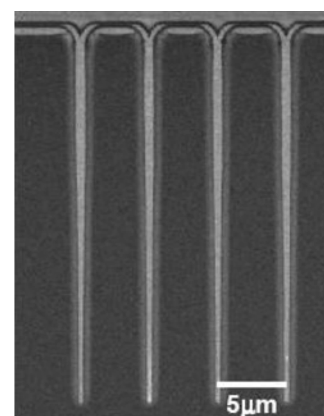

Fig. 12 *SEM image of high aspect ratio TSV [33]*

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On the other hand, tungsten filling is easier in via holes with high aspect ratio as one can use the chemical vapour deposition process which is more conformal. However, high residual stress can still be an issue. Poly-silicon is the option for via-first TSVs but its resistance is higher than metals. With the advantages and disadvantages of each material, the selection and choice of TSV filling material is an important consideration in wafer-level 3D IC.

In the author's (K.N. Chen) previous research group at IBM, a 300-mm wafer-level 3D integration process using tungsten (W) TSV and hybrid Cu/adhesive wafer bonding is demonstrated [36, 37]. The adhesive used here is polyimide. The bonding approach uses the so-called transfer-join method. The initial reliability evaluations, including the interface bonding strength, via chain resistance as a function of deep thermal cycles, ambient permeation oxidation and the temperature and humidity tests, all show favourable results.

4 Example of wafer-level 3D IC integration

The effective way to understand wafer-level 3D IC integration process is to examine an example of such process. In this section, a 3D IC integration flow initially proposed and developed by MIT is described [36]. This novel process flow includes several key technologies and therefore is suitable as an introductory study to understand wafer-level 3D IC integration technology.

The MIT three-dimensional integration is based on direct Cu–Cu wafer bonding at low temperature. Two device wafers, with Cu interconnects for electrical connections and Cu pads for structural support, are bonded to each other in a face-to-back orientation using Cu as the bonding medium. The process flow is illustrated in Fig. 13. The salient features and key steps shown in Fig. 7 are described as follows [38]:

1. Fabrication of device layers on an SOI wafer (top wafer) and a bulk substrate wafer;
2. In order to stack the top device layer on the substrate device layer, the substrate of SOI wafer has to be removed. The top SOI wafer is attached temporarily to a handle to provide mechanical support during wafer thinning;
3. The thinning process to remove the Si substrate of SOI wafer is a combination of mechanical grinding and chemical etching, which stop selectively on the buried oxide of the SOI wafer;
4. Once the removal of SOI substrate is completed, interlayer vertical vias (similar to TSV) are created by etching the buried oxide, SOI and ILD;
5. PECVD oxide sidewall passivation and via filling using damascence process are performed;
6. Cu interconnects are deposited on the top of the vias for electrical connectivity. In this step, the device layer that is attached to the handle wafer is treated as the upper wafer for the next bonding process;
7. Fabrication of device layers, including the patterning of Cu interconnects and pads, on a bulk Si substrate wafer follows next. This bulk Si wafer with device layer is treated as the bottom wafer. Then, the upper wafer and bottom wafer are aligned and bonded at the optimised bonding conditions;
8. Handle wafer release is the final step of the 3D integration process. The handle wafer is released from the bottom wafer. The top device layer is bonded permanently to the device layer at the bottom wafer.

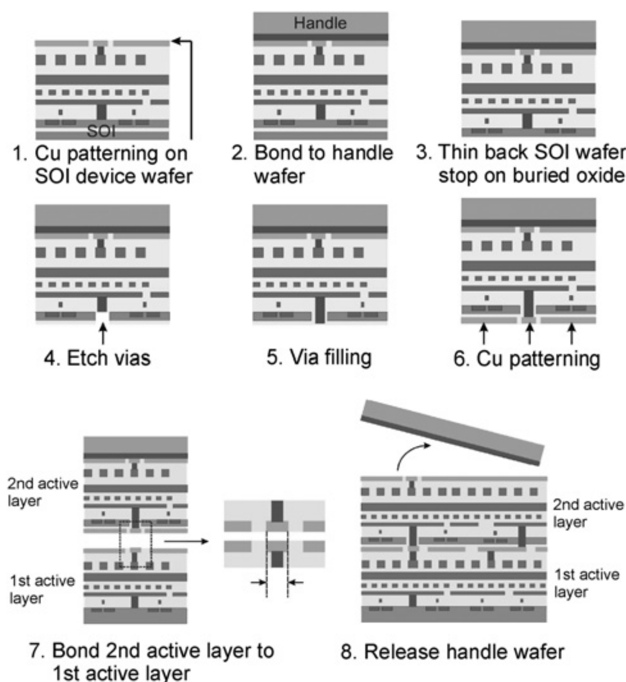

Fig. 13 *MIT process flow for fabricating 3D IC [38]*

5 Challenge, applications and outlook

Unlike conventional 2D technology, wafer-level 3D integration offers more advantages, including (a) higher interconnect density; (b) lower interconnect RC leads to lower power consumption and higher operation speed [39, 40] and (c) lower integration cost. The main drivers for 3D applications include (i) form factor, such as replacing wire bond with TSV in CMOS image sensor, (ii) high density, such as stand-alone memory stack, (iii) performance, such as bandwidth enhancement in memory on logic and (iv) heterogeneous integration of disparate chips. Regardless of the main driver, the feasibility and key consideration of any 3D application for consumer products has always been low cost manufacturing.

Broadly, applications enabled by 3D technology can be classified into three categories, as shown in Fig. 14. The first group of products only utilises TSV such as CMOS image sensor (at the time of writing, there are commercial products from companies such as ST Microelectronics, Toshiba, OKI, etc.), backside ground (e.g. SiGe power amplifier by IBM) and silicon interposer. In this class of devices, chip-to-chip bonding is not required. In another group, 3D devices are implemented by bonding chip on chip in a face-to-face fashion. Chip-to-chip electrical connections can be established with micro-bump or bumpless metal–metal

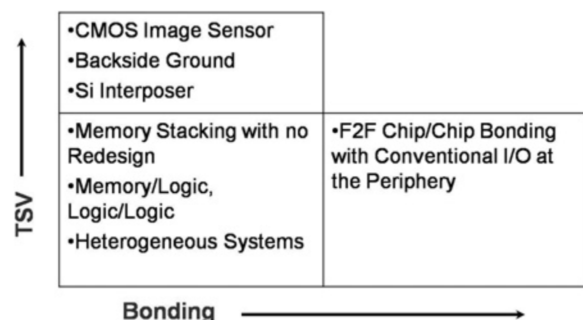

Fig. 14 *Applications enabled by 3D technology*

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bonding. I/O is formed using conventional wire bond or flip chip at the non-bonding periphery area. One such example is the Sony Play Station featuring memory on logic. The real 3D devices that make use of both TSV and bonding include stand-alone high density memory stack, memory on logic, logic on logic and heterogeneous systems. At the time of this writing, there has been announcement from Elpida on a multi-layer DRAM stack using 3D stacking technology.

For more than 40 years, performance growth in IC is realised primarily by geometrical scaling. In more recent nodes, performance boosters are used to sustain this historical growth. Moving forward, 3D integration is an inevitable path. There have been significant investment in 3D technology by various sectors and the development has been both rewarding and encouraging. While 3D technology is not without it challenges, it is likely to see wider adoption of 3D technology in the future when solutions for thermal management, EDA tools, testing and standardisation are made available in the IC supply chain.

6 Summary and conclusion

As we are approaching the physical limitation in conventional scaling [41], the semiconductor industry can no longer integrate more transistors on integrated circuits as readily as before. 3D IC technology offers a novel and practical paradigm shift that allows extension of Moore's law. In addition, 3D IC provides a viable solution to achieve heterogeneous integration and form factor requirements of today and future electronic products. With the concerted efforts from academia and industry, research and development in wafer-level 3D IC integration is making significant progress and this can potentially lead to high volume production of the next generation of integrated electronics products that offer enhanced performance and functional diversification that we can never imagine. This review provides a brief introduction on this emerging field of wafer-level 3D IC and it covers various integration schemes and key enabling technologies.

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