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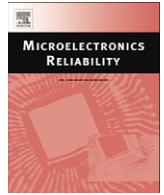

Design to suppress return-back leakage current of charge pump circuit in low-voltage CMOS process

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ABSTRACT

A new charge pump circuit has been proposed to suppress the return-back leakage current without suffering the gate-oxide reliability problem in low-voltage CMOS process. The four-phase clocks were used to control the charge-transfer devices turning on and turning off alternately to suppress the return-back leakage current. A test chip has been implemented in a 65-nm CMOS process to verify the proposed charge pump circuit with four pumping stages. The measured output voltage is around 8.8 V with 1.8-V supply voltage to drive a capacitive output load, which is better than the conventional charge pump circuit with the same pumping stages. By reducing the return-back leakage current and without suffering gate-oxide overstress problem, the new proposed charge pump circuit is suitable for applications in low-voltage CMOS IC products.

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1. Introduction

Charge pump circuits can generate the voltage higher than the normal power supply voltage (VDD) or lower than the ground voltage (GND) in a chip, which were usually consisted of diode-connected MOSFET, switches, or level shift circuits. Moreover, charge pump circuits are often used to write or erase data in the nonvolatile memory [1,2] and also applied in the power management blocks of driver ICs for liquid-crystal-display (LCD) panels [3].

Fig. 1a shows the earlier Cockcroft–Walton voltage multiplier [4], which can generate steady potential nearly 800,000 volts to power the particle accelerator, performing the first artificial nuclear disintegration in the history. This circuit is composed of capacitors, diodes, and clocks (CLK and CLKB) to form the voltage multiplier. The voltage gain, which means the ratio between the open circuit output and VDD, can be expressed with pumping capacitors and parasitic capacitors [5]. When the pumping stage is increased, it is decreased because the large parasitic capacitors degrade the output voltage in each stage. Hence, the Cockcroft–Walton voltage multiplier became inefficient due to its large stray capacitance and high output impedance which could not be easily integrated into the standard CMOS process.

In order to overcome the limitation for integrating into a chip, the Dickson charge pump circuit was proposed to create a new voltage multiplier, as that shown in Fig. 1b composed by NMOS [6,7]. The diode-connected NMOS is utilized to transfer charge from input to output in each stage, and clocks are out-of-phase. When the CLK is low (CLKB is high), m1, m3, and m5 are turned on (m2 and m4 are kept off), the charge is transferred from VDD to node 1, the charge in node 2 is transferred to node 3, and the charge in node 4 is transferred to V_{out}. On the other hand, when the CLK is high (CLKB is low), m2 and m4 are turned on (m1 and m3 are kept off), the charge is transferred from node 1 to node 2, and charge in node 3 is transferred to node 4. The voltage fluctuation of each pumping node can be simplified as

$$\Delta V \approx V_{\mathrm{clk}} = \mathrm{VDD}, \quad (1)$$

where V_{clk} is the clock amplitude (which usually equals to the supply voltage VDD), when the effect of loading current and parasitic capacitance of each node are ignored. Therefore, the output voltage of Dickson charge pump circuit can be expressed as

$$V_{\mathrm{out}} = \sum_{i=1}^{N+1} (\mathrm{VDD} - V_{\mathrm{ti}}), \quad (2)$$

where V_{ti} denotes the threshold voltage with the body effect of the ith diode-connected NMOS and N is the stage number. When each node is pumped higher, the threshold voltage in each NMOS becomes larger due to the body effect. Thus, the efficiency of this circuit will be decreased as the stage increases. In addition, it suffers overstress voltage across the gate oxide of devices, 2VDD-V_{ti}, with the ith device in the ith stage. Moreover, it will suffer the junction breakdown when stage nodes are pumping higher. To avoid the gate-oxide overstress problem, the high-voltage device with thick gate oxide was required for implementing such Dickson charge

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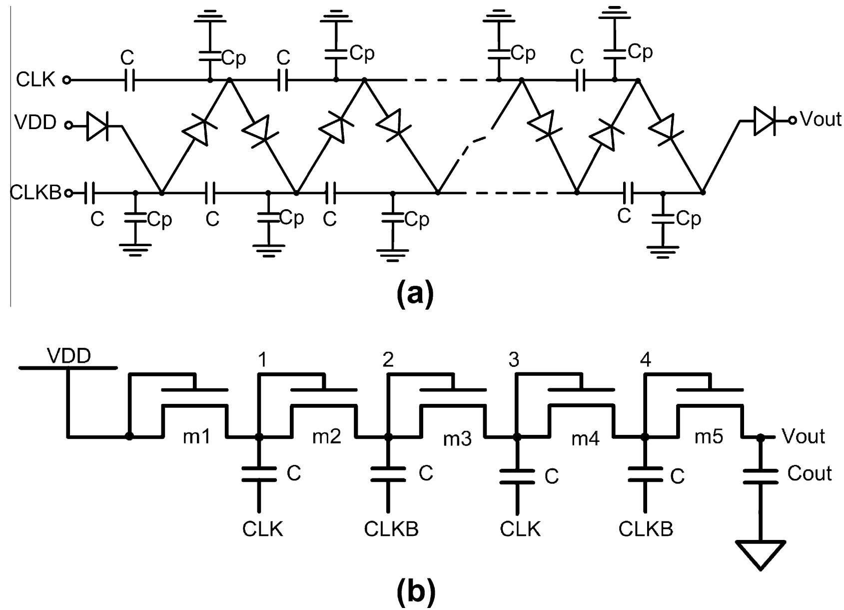

Fig. 1. The schematics of (a) Cockcroft–Walton voltage multiplier [4] and (b) Dickson charge pump circuit [5].

pump circuit. However, the thick gate-oxide NMOS often has a high threshold voltage which somehow degrades the pumping efficiency. Due to the fact that the CMOS technology is continuously scaled down, some modified charge pump circuits [8–22] based on Dickson charge pump circuit were invented to eliminate the body effect, to overcome the threshold drop and the gate-oxide overstress problem, and to improve the efficiency.

The charge pump circuit proposed in [8] has similar concept as Dickson charge pump circuit. It utilizes four-phase clock to control the gate voltage of the charge-transfer devices to eliminate the threshold drop issue except the diode-connected transistor at the output stage. A bootstrapped circuit [9] and auxiliary circuits [10,11] used in the charge pump circuits could elevate the pumping voltage of Dickson voltage multiplier, yet these charge pump circuits occupied more silicon area and wasted more extra power in the systems. The floating-well technique [12] was used to reduce the influence of the body effect on the diode-connected MOSFET, but the substrate current generated due to the floating-well connection might affect other circuits in the same chip. The modified design [13] could transfer the charge from input to output completely by using switches, although it also suffered the body effect and the threshold drop in the final stage. The dynamical operation decides the conducted connection of the bulk terminals of the charge-transfer devices by using auxiliary small MOSFET [14]. However, it could generate the parasitic capacitors and substrate current when the bulk terminals of the charge-transfer devices were floating during the clock transitions. Besides, above charge pump circuits all suffer the gate-oxide overstress problem. The charge pump circuits consisted of all PMOS can eliminate the body effect without extra layers [15,16]. Nonetheless, the implementation of all PMOS devices causes larger area and parasitic capacitance, and more devices connected to the pumping nodes degraded the efficiency of charge pump circuits. Charge pump circuits [17–22] can eliminate the threshold drop by using switches and overcome the gate-oxide overstress problem with two-branch structure. However, the circuit [17,18] has serious leakage current generated in bulk-diodes of PMOS since the bulks of PMOS in these circuits are connected to the drain terminals of NMOS in the same pumping stage. The enhanced charge pump circuit [19] could be turned on easily due to the decrease for the turn-on resistors of the charge-transfer devices. Nevertheless, it occupied more silicon area because of extra capacitors needed. Multi-stage charge pump circuits [20–22] have higher voltage gain than previous works. Nonetheless, the leakage current is generated during the clock transitions, and it is particularly serious as the clock signals are not ideal [23].

2. Charge pump circuit without gate-oxide overstress problem

Fig. 2a shows the charge pump circuit of the prior art [22] designed with low-voltage devices and without suffering the gate-oxide overstress problem. CLK and CLKB are out-of-phase with the amplitude of VDD. This circuit uses two branches to avoid the gate-oxide overstress, where the voltage difference between the drain/source and the gate in each MOSFET is not over VDD. This circuit has no threshold drop through using switches to transfer charge from input to output. However, in this charge pump circuit, the return-back leakage current during the transition of clocks causes some degradation on the output voltage (V_{out}).

For example, when CLK is from low to high (CLKB is from high to low), the voltage of node 4 becomes 5VDD from 4VDD, the voltage of node 8 becomes 4VDD from 5VDD, and the voltage of node A still holds in 4VDD. Hence, it is expected that mp8 in Fig. 2a has to be turned off and simultaneously mn8 and mp7 in Fig. 2a have to be turned on. Actually, mp8 could not be turned off immediately while mn8 and mp7 have been turned on already. Thus, mp8, mn8, and mp7 would provide a leakage path such that the charge at the output will return back through mp8, mn8, and mp7 to node 7. Similarly, if mp4 is already turned on and mn4 as well as mp3 could not be turned off immediately, it also provided a leakage path from output to node 3. The simulated results are shown in Fig. 2b, where the leakage currents are generated in these devices during the clock transitions. For PMOS (mp4, mp8), the return-back leakage current is positive, with peak current around 100 μA. Similarly, the return-back leakage current is negative in NMOS (mn4, mn8), and the peak current is also around 100 μA.

3. Newly proposed charge pump circuit

In this work [24], the new charge pump circuit is proposed to suppress the return-back leakage current in the previous work

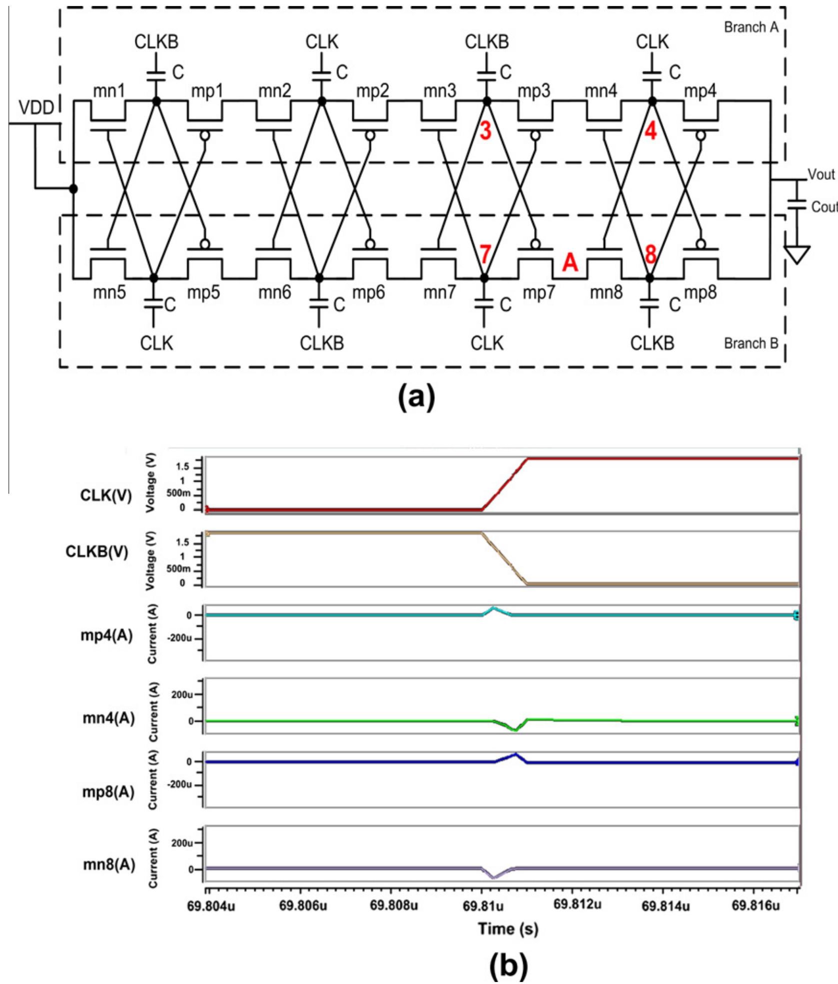

Fig. 2. (a) The charge pump circuit reported in the prior art [22] to solve the gate-oxide overstress problem in low-voltage CMOS process and (b) the return-back leakage current generated in mp4, mn4, mp8, and mn8 in the final stage during the transitions with 1.8-V amplitude of clock signals.

[22] during clock transitions. Therefore, pumping efficiency of the new design is further improved for implementation in the low-voltage CMOS processes. Fig. 3a shows the newly proposed charge pump circuit with the corresponding clock waveforms (CLKA, CLKB, CLKC, and CLKD) shown in Fig. 3b. In the schematic diagram, C represents the main pumping capacitor, and Cs is the auxiliary pumping capacitor with a small capacitance. Each stage also contains Branch A and Branch B, which have identical structures but are turned on alternately to pump output voltage to high. By using the clock signals (CLKA to CLKD) as depicted in Fig. 3b to create four operation periods, PMOS (mc1, mc2, mc3, mc4, md1, md2, md3, and md4) of small dimensions and the auxiliary Cs capacitors control the main charge-transfer devices (mp1, mp2, mp3, mp4, mp5, mp6, mp7, and mp8) turning off properly. Thus, return-back leakage current during the clock transitions can be avoided. More details about circuit operation in the four separate periods are introduced in the following.

3.1. During the period T_1

During the period T_1, CLKA, CLKB, CLKC, and CLKD are high, low, high, and high to low, respectively. At this moment, the voltage difference V15 (V37) between node 1 and node 5 (node 3 and node 7) is –VDD. Hence, mn1 and mc1 (mn3 and mc3) are turned on to transfer charge from input node of VDD to node 1 (node 2 to node 3) and transfer charge from node 5 (node 7) to node c1 (c3). At the same moment, mp5 and mn6 (mp7 and mn8) are turned on to transfer charge from node 5 to node 6 (node 7 to node 8). Simultaneously, mn5 (mn7) is kept off to cut off the leakage path from node 5 back to input node of VDD (node 7 back to node 6), and mp1 and mn2 (mp3 and mn4) are kept off to cut off the leakage path from node 2 back to node 1 (node 4 back to node 3).

For the last output stage, mp4 and mn8 are turned on (mn4 and mp8 are kept off), and the pumping voltage will be transferred from node 4 to the output.

3.2. During the periods T_2 and T_4

During the periods T_2 and T_4, CLKA, CLKB, CLKC, and CLKD are low, low, high, and high, respectively. At this period, the main charge-transfer devices (mn1, mn2, mn3, mn4, mn5, mn6, mn7, and mn8) are turned off because all the voltage differences from gate to source of charge-transfer devices are zero. In the meantime, the small-size PMOS (mc1, mc2, mc3, mc4, md1, md2, md3, and md4) are turned on to raise the node voltages of c1/d1, c2/d2, c3/d3, and c4/d4 to the level of 2VDD, 3VDD, 4VDD, and 5VDD, respectively. Therefore, the gate voltages of all charge-transfer PMOS devices (mp1, mp2, mp3, mp4, mp5, mp6, mp7, and mp8) are higher than their corresponding source voltages to keep themselves off.

3.3. During the period T_3

During the period T_3, CLKA, CLKB, CLKC, and CLKD are low, high, high to low, and high, respectively. At this moment, the

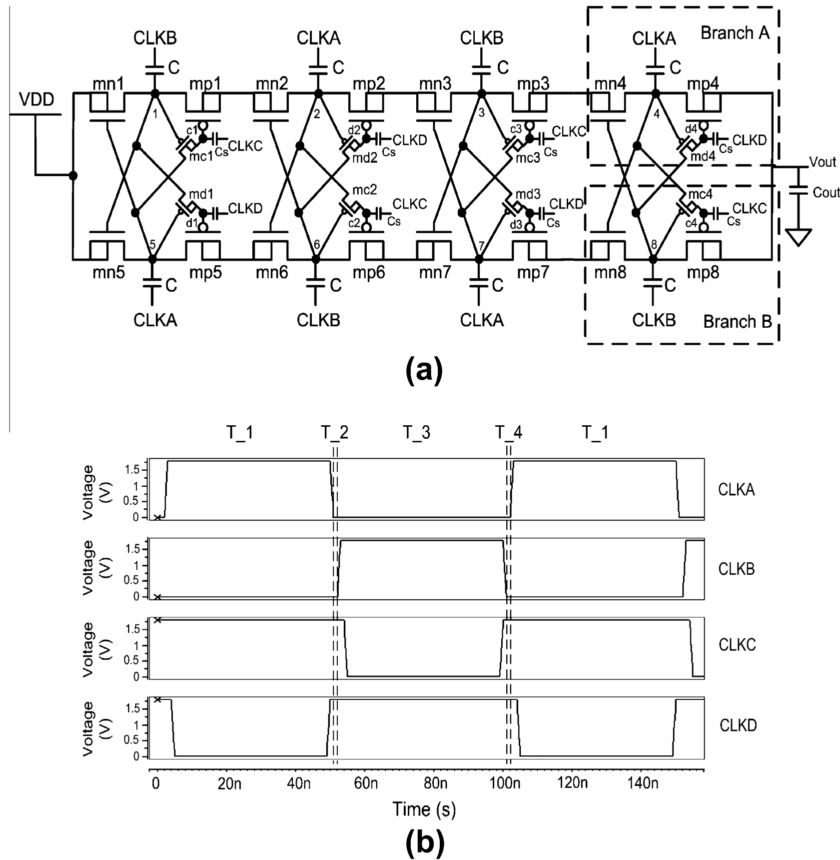

Fig. 3. (a) The schematic of newly proposed charge pump circuit and (b) the corresponding clock waveforms with 1.8-V amplitude and 10-MHz frequency to create four separate operation periods (T_1, T_2, T_3, and T_4).

voltage difference V15 (V37) between node 1 and node 5 (node 3 and node 7) is VDD. Hence, mn5 and md1 (mn7 and md3) are turned on to transfer charge from the input node of VDD (node 6) to node 5 (node 7) and transfer charge from node 1 (node 3) to node d1 (d3). At the same moment, mp1 and mn2 (mp3 and mn4) are turned on to transfer charge from node 1 to node 2 (node 3 to node 4). Simultaneously, mn1 (mn3) is kept off to cut off the leakage path from node 1 back to the input node of VDD (node 3 back to node 2), and mp5 as well as mn6 (mp7 and mn8) are kept off to cut off the leakage path from node 6 back to node 5 (node 8 back to node 7). For the last output stage, mp8 and mn4 are turned on (mn8 and mp4 are kept off), and the pumping voltage will be transferred from node 8 to the output.

4. Experimental verification

4.1. Simulation

A 65-nm CMOS process model with 2.5-V devices is used to simulate and verify the performances of newly proposed charge pump circuit (this work) and the previous work of Fig. 2a (for comparison). Fig. 4 shows the simulated result of the return-back leakage current of the newly proposed charge pump circuit during the clock transitions. The peak currents are around 2 μA for NMOS and PMOS in the final stage. As the result, the newly proposed charge pump design is effective to suppress the return-back leakage current in the conventional charge pump circuits. Fig. 5 shows the voltage waveforms of each node to verify the newly proposed charge pump circuit without gate-oxide overstress problem. From this simulation, the voltage difference is not over 1VDD (1.8 V).

To have a fair comparison, the newly proposed charge pump circuit (this work) and the previous work [22] of Fig. 2a are designed under same condition which contains 2-pF pumping capacitor, 1.8-V supply voltage, 10-MHz clock frequency, 20-pF output loading capacitor, and the same sizes of charge-transfer devices. Additionally, the auxiliary capacitor (Cs) in the newly proposed charge pump circuit is designed with 25 fF. Fig. 6 compares the simulated output voltages of the previous work [22] and this work under different voltage levels of VDD. In Fig. 6, the output voltages of these circuits are degraded when the input VDD is decreased. The simulated output voltage of the newly proposed charge pump circuit is 8.85 V, but that of previous work (Fig. 2a) is only 8.3 V with 1-ns rise/fall time of all clock signals and 1.8-V supply voltage. Moreover, the return-back leakage current will be essentially reduced when the VDD voltage level is reduced. The output voltages of previous work and this work are close at ~5 V in the simulation results of Fig. 6 under the condition of 1-V supply voltage and tiny rise/fall time.

The overshooting/undershooting ripples at the simulated output voltage waveforms of the previous work [22] and the newly proposed charge pump circuit in the steady state are shown in Fig. 7a and b, respectively. The value of the output ripple is calculated by

$$\text{Ripple}(\%) = \frac{V_{\text{pp}}}{V_{\text{out}}} \cdot 100\%, \tag{3}$$

where V_{out} is the average output voltage and V_{PP} is the peak-to-peak ripple voltage in the output voltage waveforms. If the supply voltage (VDD) increases, the quantity of the return-back leakage current will also increase because the output voltage becomes higher. Hence, the ripple will increase under higher supply voltage (VDD).

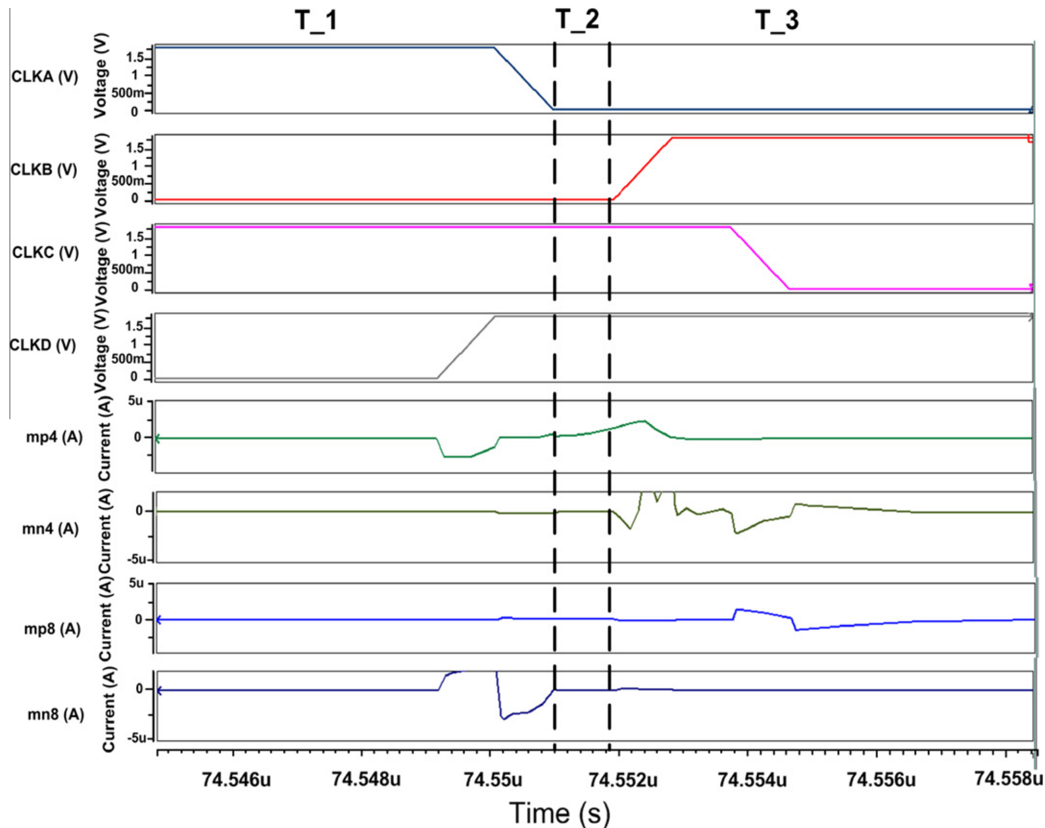

Fig. 4. The simulated results of return-back leakage current and corresponding clock transition in the newly proposed charge pump circuit with four-phase clocks of 1.8-V amplitude and same device sizes compared with the previous work [22].

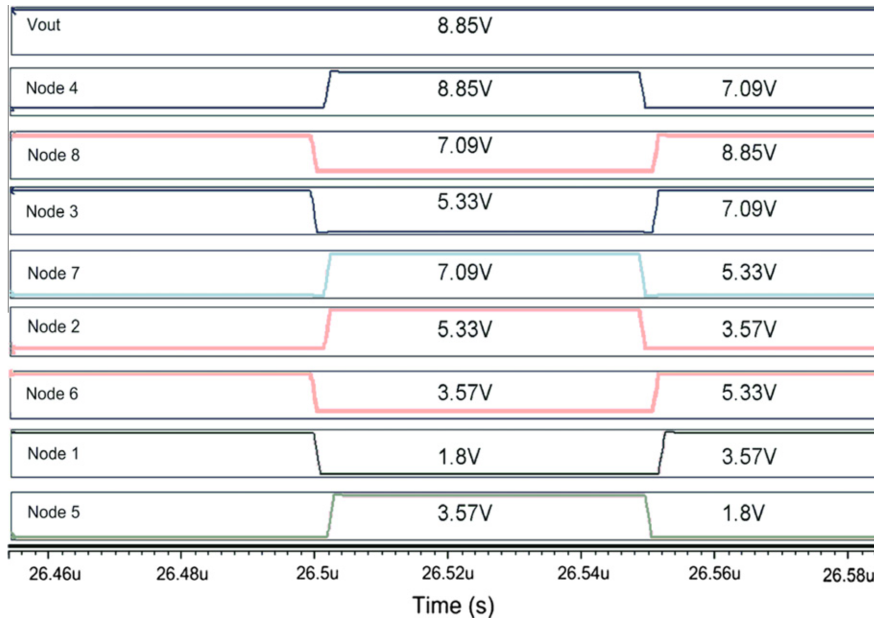

Fig. 5. The simulated voltage waveforms at the nodes 1 to 8 and the output voltage (V_{out}) in the newly proposed charge pump circuit with VDD of 1.8 V.

The relative simulated results are shown in Fig. 8. From this figure, although the output value of this work (8.85 V) is higher than the previous work [22] (8.3 V) under the supply voltage of 1.8 V, the output ripple of this work is still smaller than that of the previous work [22].

When the rise/fall times of clock signals are increased, the time periods of the return-back leakage current will become longer, so the quantity of return-back leakage current will also increase during the clock transitions. Fig. 9 shows the method to estimate the return-back leakage current from the observed simulated waveforms. For the PMOS, the return-back leakage current is positive. Two cases about the newly proposed charge pump circuit are depicted in this figure for clock signals with 1-ns and 12-ns rise/fall time. The quantity of the leakage charge in one transition can be approximately calculated, with its peak current value (H) and the major duration (W) when leakage is generated, by using the for-

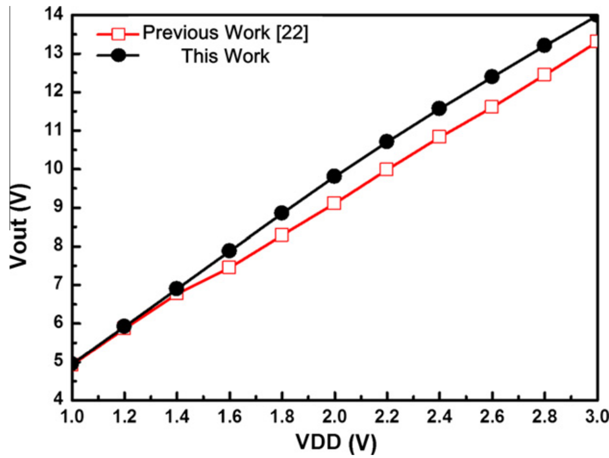

Fig. 6. The simulated output voltages of the four-stage charge pump circuits with 10-MHz clock frequency, 1-ns rise/fall time, and 20-pF capacitive loading under the different supply voltages (VDD).

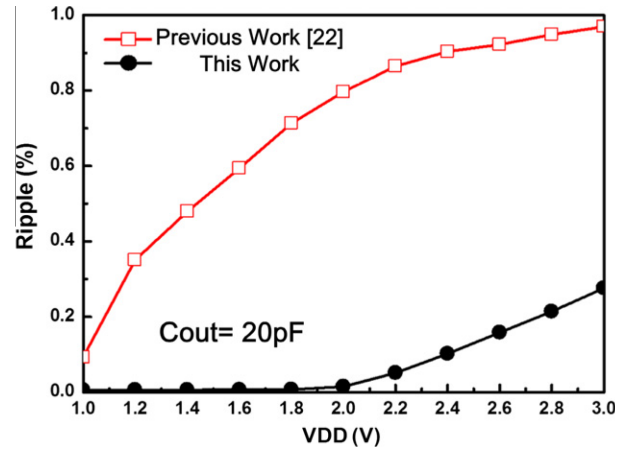

Fig. 8. The simulated output ripples of this work and the previous work [22] with different supply voltages (VDD).

mula of triangle area. Finally, the estimated return charge is the sum of all leakage currents (all the triangles) during the same period. For the NMOS with negative return-back leakage current, the same method can still be applied. The estimated results of the simulated return charge are shown in Fig. 10 with the clock signals of different rise/fall times. From this figure, the newly proposed charge pump circuit has smaller return charge than that in the previous work [22] of Fig. 2a. Fig. 11 shows the simulated output voltages of the charge pump circuits with different rise/fall times in the clock signals. In Fig. 11, when the clock signals are not ideal, with increased rise/fall times of clock signals, the time period for the happening of leakage current is also increased so that the output voltages of the previous work [22] is significantly decreased. However, by using this newly proposed design, the degradation on the output voltages of charge pump circuit due to the long rise/fall times in the clock transition can be alleviated.

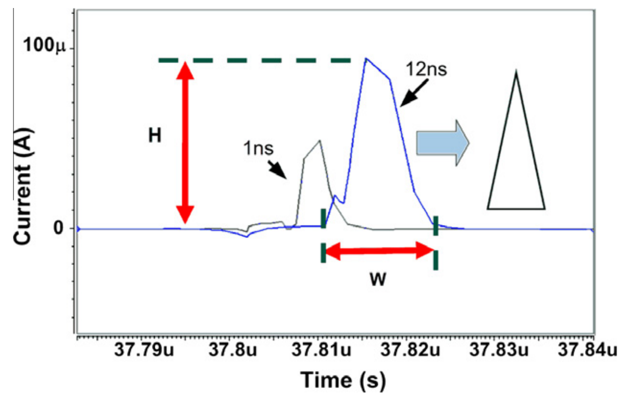

Fig. 9. The method used to estimate the return charge of PMOS by approximately calculating the quantity as the triangle area during the clock transitions in the charge pump circuits.

4.2. Measurement in silicon chip

A test chip has been fabricated in a 65-nm CMOS process to verify the newly proposed charge pump circuit (this work) and the previous work [22] (Fig. 2a). The chip photographs of the fabricated circuits are shown in Fig. 12. With the main pumping capacitor (C) of 2 pF, the auxiliary capacitor (Cs) of 25 fF, supply voltage of 1.8 V,

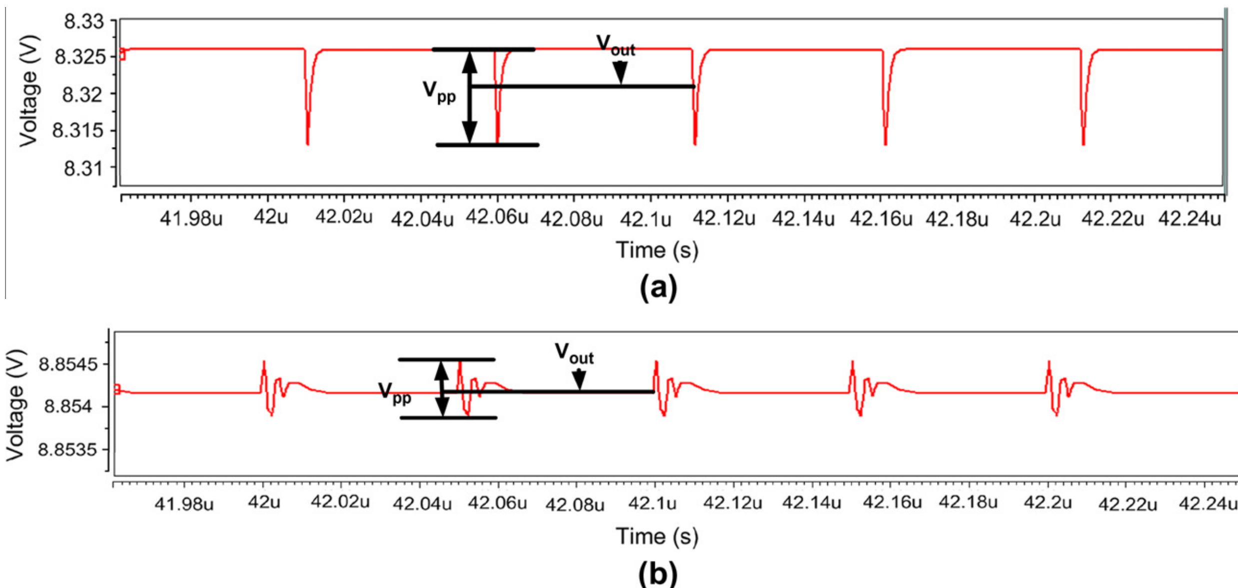

Fig. 7. The simulated output voltage waveforms of (a) the previous work [22] and (b) this work with supply voltage of 1.8 V, frequency of 10 MHz, and capacitive loading of 20 pF.

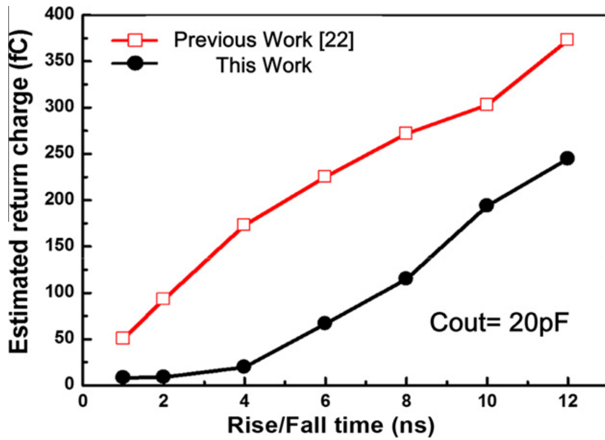

Fig. 10. The estimated return charge of the charge pump circuits under the clock signals with different rise/fall times (f = 10 MHz, VDD = 1.8 V).

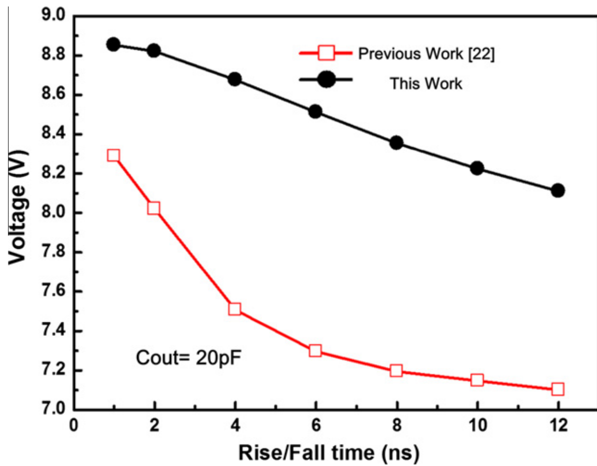

Fig. 11. The simulated output voltages of the charge pump circuits with different rise/fall times in the clock signals (f = 10 MHz, VDD = 1.8 V).

and clock frequency of 10 MHz, the measured output voltage of the newly proposed charge pump circuit is around 8.8 V and that of the prior art [22] is around 7.9 V when no loading resistor (R_{out}) is added to the output (V_{out}).When the R_{out} of different resistances is added to the output node of the fabricated charge pump circuits,

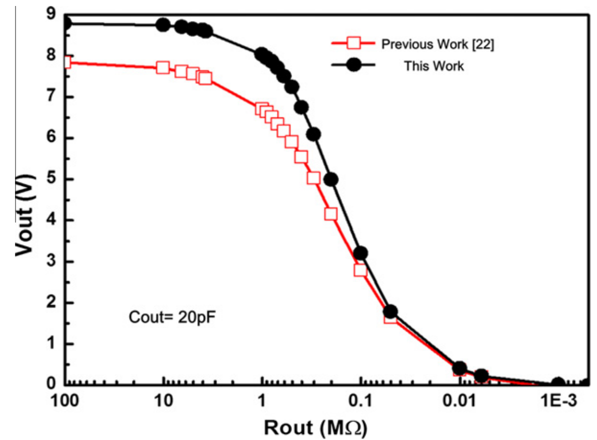

Fig. 13. The measured output voltages of this work and the previous work [22] (f = 10 MHz, VDD = 1.8 V, rise/fall time of ~2 ns) with different loading resistances (R_{out}) at the output node.

the output voltages (V_{out}) will be degraded due to the limited charges generated from the pumping capacitors at each clock cycle, as the measured results shown in Fig. 13. When the clock generated by the clock generator is not ideal, such as the rise/fall times of clocks increases or it generates overlapping situation, the efficiency of a charge pump circuit will be poorer because of the return-back leakage current generated. By inserting a short turn-off period into the circuit operation of charge pump circuit to stagger the turn-on time of the charge-transfer devices, the return-back leakage current during the clock transitions can be successfully suppressed in the newly proposed charge pump circuit. Fig. 14 shows the measured results to verify the simulated results in Fig. 11 about the output voltages under different rise/fall times when no loading resistor (R_{out}) is added. The measured output voltages of the newly proposed charge pump circuit are still higher than that of the previous work [22] with the same device dimensions and capacitors. Thus, the newly proposed charge pump circuit has been successfully proved to suppress the return-back leakage current during the clock transitions. Fig. 15 shows the measured output voltages corresponding with different supply voltages of the newly proposed charge pump circuit and the prior art [22] when no loading resistor (R_{out}) is added. The output voltages of these circuits cannot be higher (over 9 V) with the supply voltage over 1.8 V, because the junction breakdown voltage of these devices in the given CMOS process is about 9 V. From the fact

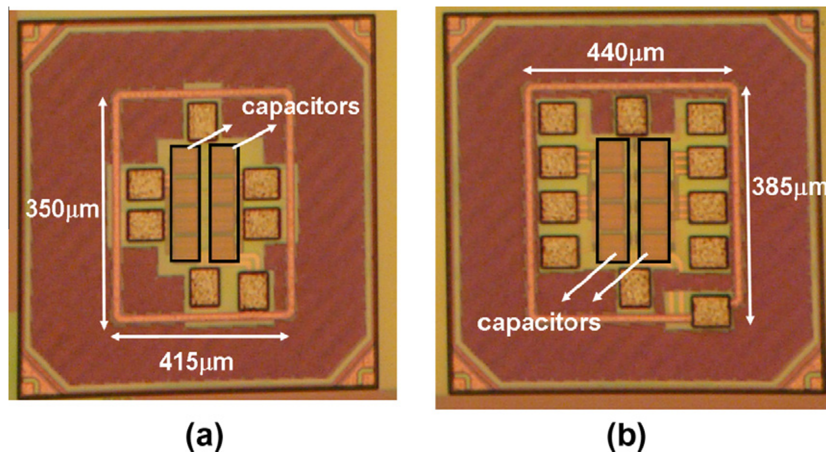

Fig. 12. Chip photographs of (a) the previous work [22], and (b) the newly proposed charge pump circuit, fabricated in a 65-nm CMOS process.

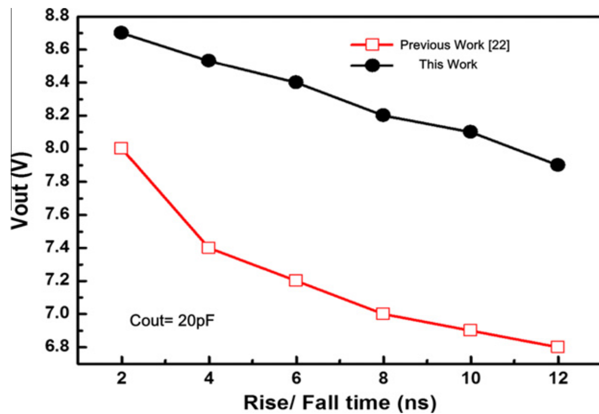

Fig. 14. The measured output voltages of this work and previous work [22] (f = 10 MHz, VDD = 1.8 V) with different rise/fall times of clock signals.

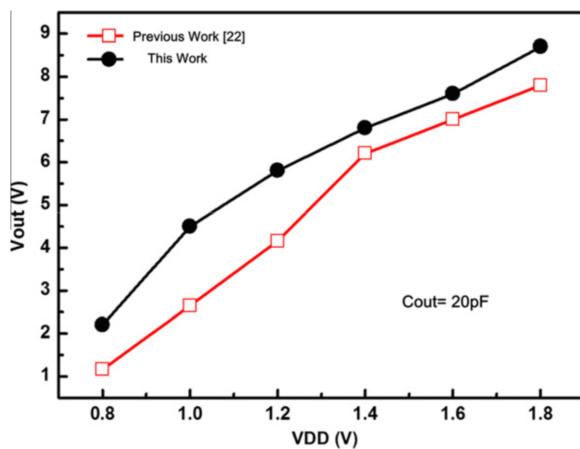

Fig. 15. The measured output voltages of the newly proposed charge pump circuit and the previous work [22] with the 20-pF capacitor loading and ~2-ns rise/fall time in different the supply voltages (VDD).

that the newly proposed design provides output voltage closer to the ideal value, the newly proposed charge pump circuit is more suitable to be used in low-voltage process than the previous work [22].

5. Conclusion

A new charge pump circuit with the design to suppress the return-back leakage current in low-voltage CMOS process has been proposed and successfully verified in silicon. During the clock transitions, it is difficult to control the devices turning on or turning off definitely, the return-back leakage current thus generated to cause the decrease of output voltage. Similarly, if the clock signals are not ideal or the pumping capacitors are too large, the rise/fall times of clock signals are increased, and the return-back leakage current will increase to degrade the output voltage. Since the turn-on times of the devices in the newly proposed charge pump circuit are separated completely, the leakage current path can be obstructed, and the output voltage will be maintained in a high value without degradation. Furthermore, by using the two-branch structure, the newly proposed charge pump circuit is also free from suffering the gate-oxide overstress problem. As a result, the newly proposed charge pump circuit by reducing the return-back leakage current has better efficiency than that of the prior designs, and also without suffering the gate-oxide overstress problem in a low-voltage CMOS process.

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