A Novel Array-Based Test Methodology for Local Process Variation Monitoring

Tseng-Chin Luo, Mango C.-T. Chao, Michael Shien-Yang Wu, Kuo-Tsai Li, Chin C. Hsia, Huan-Chi Tseng, Philip A. Fisher, Chuen-Uan Huang, Yuan-Yao Chang, Samuel C. Pan, *Member, IEEE,* and Konrad K.-L. Young

***Abstract*—As process technologies continually advance, local process variation has greatly increased and gradually become one of the most critical factors for integrated circuit manufacturing. To monitor local process variation, a large number of devices-under-test (DUTs) in close proximity must be measured. In this paper, we present a novel array-based test structure to characterize local process variation with limited area overhead. The proposed test structure can guarantee high measurement accuracy by application of the test techniques proposed in this paper: hardware IR compensation, voltage bias elevation, and leakage-current cancelation. Furthermore, the DUT layout need not be modified for the proposed test structure. Thus, the measured variation exactly reflects the reality in the manufacturing environment. The measured results from the few most advanced process-technology nodes demonstrate the effectiveness and efficiency of the proposed test structure in quantifying local process variation.**

***Index Terms*—Automatic test equipment, measurement techniques, mismatch, process variation, test structures, test structure design, transistor array.**

I. Introduction

As the feature size of devices scales down, the device variability imposed by each process step does not scale accordingly. As a result, the process variation of advanced process technology nodes has greatly increased and has become a critical factor in both integrated circuit (IC) design and manufacturing [1]. In order to design and manufacture in the presence of process variation, much research effort has focused on the areas of measurement, analysis, and modeling of variation during the past decade [2]–[10]. As the relative impact of process variation has continued to increase and become more randomized, research interest has shifted from *global process variation* toward *local process variation*, where the device characteristics within a close proximity vary randomly, since the sources of global and local process variation are different [1], [12]. This focus on local process variation has led to increased importance of array-based test structures, including decode logic, which are capable of characterizing a large number of individual transistors. However, the utility of such array-based test structures is limited by: 1) the loss of accuracy due to voltage drop from parasitic resistance, and 2) the leakage current (including junction leakage) from the control circuitry. To overcome these challenges, we propose a novel test structure design and test methodology including *hardware IR compensation* to address the IR drop from parasitic resistance, and the combination of *voltage bias elevation* and *leakage current cancelation* to eliminate both leakage currents from control circuitry and diode leakage related to hardware IR compensation.

In the typical measurement of global variation, a conventional test structure, a process control monitor (PCM) testline, is used on a wafer's scribe line. The PCM testline places its devices-under-test (DUTs) and IO pads in a straight line and uses four IO pads to measure each DUT. Thus, the height of a PCM testline is limited by the pad size, and so is the required spacing in a scribe line. To accurately measure local variation, a large number of DUTs need to be placed in close proximity and measured individually, or the measured results may misrepresent the process variation as a measurement outlier. However, using test structures such as PCM testlines to place a large number of DUTs within a small neighborhood is not feasible since the density of IO pads of such a structure would become too high (4 IO pads for each DUT) and would easily exceed the practical limit of a probe card. In order to place a large number of DUTs close enough to one another and measure them individually, several array-based test structures have been proposed to share IO pads among DUTs and hence reduce the number of the required IO pads in between the DUTs [11], [13], [14]. These array-based test structures use row and column decoders to select an individual DUT in the DUT array and employ various techniques to address the IR drop imposed by the transmission gates on a DUT's selection path. The test methodology of [13] addressed the IR drop with some success, by employing an operational amplifier placed directly on the probe card, and utilizing an Agilent 4156 SMU in a force/sense circuit, similar to the hardware IR compensation technique we propose in this paper. Though demonstrating the validity of this approach, this valuable work did not address the impact of the op-amp internal resistance on the voltage measurement error or the potential diode leakage through transmission gates. Here-

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T.-C. Luo, M. S.-Y. Wu, K.-T. Li, C. C. Hsia, H.-C. Tseng, P. A. Fisher, C.-U. Huang, Y.-Y. Chang, S. C. Pan, and K. K.-L. Young are with Taiwan Semiconductor Manufacturing Corporation, Hsinchu 300, Taiwan (e-mail: tclo@tsmc.com).

M. C.-T. Chao is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: mango@faculty.nctu.edu.tw).

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in, we explicitly consider the impact of the source/measure unit (SMU) internal resistance and introduce voltage bias elevation and leakage-current cancelation to minimize leakage through the transmission gates. The array-based structure of [14] suffers from large background leakage from the DUTs. Reference [12] used a ROM-like DUT-array design, which shares a common poly gate and a common drain among DUTs to avoid the usage of decoders. However, such a gate-sharing array design results in a DUT layout different from the device layout used in real products. Therefore, the measured process variation may not be representative of an actual product, which greatly limits the application of such ROM-like test structures. In addition, the ROM-like test structure may result in a large junction leakage current due to common drain/gate buses.

In this paper, we propose a novel array-based test structure utilizing decoders to access the DUT array, where all the peripheral circuits, such as decoders and latches, are implemented by I/O devices (thick gate oxide and long channel devices) and thus are not sensitive to process variation. In the proposed test structure, we develop a hardware IR-compensation technique to eliminate the impact of the IR drop imposed by the selection circuits. Also, we apply a voltage-bias-elevation technique to eliminate a possible negative voltage resulting from the IR-compensation hardware. Further, we develop a leakage-current-cancelation technique to reduce the background leakage when measuring a DUT's off-state current. Experimental results based on advanced process technologies demonstrate that the proposed array-based test structure can effectively measure hundreds of DUTs within a close proximity and the measurement accuracy of each DUT is almost the same as that measured by the traditional testline, on which only 8–20 DUTs can be measured. These experimental results also demonstrate the significant improvement of the measurement accuracy achieved by applying the proposed techniques. Also, compared to a ROM-like array-based test structure, the measured results of the proposed test structure can indeed reflect the reality of a manufacturing environment. The DUTs used in the experiments include single devices for discrete transistor characterization, and paired, identical adjacent devices for measurement of local mismatch.

II. BACKGROUND

A. Traditional Testline (PCM)

Fig. 1 shows the overall architecture of a conventional PCM testline, which consists of DUTs and IO pads arranged in a straight line. Each DUT is connected to 4 IO pads (one each for source, drain, gate, and bulk connections). Each IO pad is connected to the forcing and sensing node of a SMU during testline measurement through the probe card (Fig. 2). In this architecture, the voltage at the connection of forcing and sensing paths, commonly referred to as the *compensation point*, must be equal to V_{set} since no current runs through the sense path. Therefore, the IR drop caused by parasitic resistance from the tester to the compensation point is completely eliminated. However, the voltage at the drain node of the DUT may drop significantly because no voltage compensation exists between the compensation point and the drain node of the DUT. This results in a degradation of the measured current, especially when the width of the DUT's MOSFET is large ($W > 2\,\mu$m). This degradation of the DUT's measured current strongly depends on the parasitic resistance from the compensation point to the DUT. Four possible sources of parasitic resistances in a conventional PCM testline and their approximate values for the process technologies and test equipment of interest are listed below.

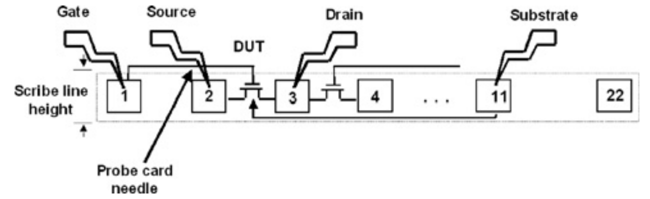

Fig. 1. Configuration of a conventional PCM testline.

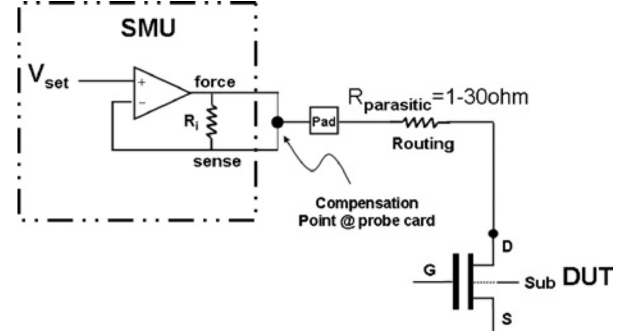

Fig. 2. Voltage compensation mechanism used in a conventional PCM testline.

1) Cable resistance from tester switch matrix to probe card $< 1\,\Omega$.
2) Contact resistance between probe card needle and testline pad = 1–20 Ω, depending on factors such as: 1) probe-card cleanliness and quality; 2) whether the top surface of the probe pads on the wafer is Al or Cu; and 3) queue time and storage ambient before probing.
3) Metal routing resistance from testline pad to DUT source/drain. For a representative example, we consider 50 μm pad spacing, metal sheet resistance Rs = 0.2 Ω/square (a typical value for M1), and routing layout consisting of 3 μm wide metal for most of the routing distance in series with three parallel metal lines 0.1 μm wide and 3 μm long to connect to the DUT. The routing resistance will then be of order 0.2 Ω [25 μm/3 μm + 3 μm/(0.1 μm $\times$ 3)] $\sim -10\,\Omega$. Of course, the exact value for a given PCM depends on the specific metal process and routing layout.
4) Resistance from source/drain contact to active silicon. For example, for a contact process having contact resistance of 60 Ω/contact and seven parallel contacts to a DUT with 1 μm channel width, this resistance will be of order 60/7 = 8–10 Ω, where the exact value depends on details of the contact and salicidation processes.

Typically, the total parasitic resistance from the compensation point to a DUT is approximately 1–30 Ω in a conventional PCM testline configuration, and in the worse case a significant

error in the measured current can be generated. In addition, a large number of DUTs are required to monitor local process variation. However, this testline architecture can only contain around 8–20 DUTs in a $\sim 60 \times 2200\,\mu\text{m}^2$ scribe line, which greatly limits the sample size of the measured DUTs and is hence not suitable for device variation modeling or process monitoring of advanced process technology nodes.

B. Transistor Array Test Structures and Adaptive Voltage Compensation

Test structures based on transistor arrays consistently must address two challenges: the IR drop along the electrical path to the DUT, and leakage current due to whatever DUT selection circuitry is employed. Here, we briefly review key representative works in the field [11], [13]–[15] and describe past efforts to address these challenges in test structures utilizing transistor arrays. The test structure of [11] is array based, utilizing transmission gates; however its use of common gate and drain connections renders it susceptible to large leakage currents similar to the ROM-like architecture. The work of [13] addressed the IR drop by placing an operational amplifier directly on the probe card, and utilizing an Agilent 4156 SMU in a force/sense circuit, similar to the hardware IR compensation technique we describe below; however, [13] did not address the impact of the op-amp internal resistance on the voltage measurement error or the diode leakage through transmission gates. Approaches to these issues will be discussed in our work in the sections that follow. The array-based structure of [14] suffers from large background leakage from the DUTs themselves. The voltage bias elevation and leakage current cancelation techniques we introduce substantially alleviate the leakage current issues suffered by the works list above. An innovative approach to voltage compensation was introduced by [15], where-in iterative adaptive voltage compensation was employed to compensate for the IR drop to the DUT. We describe this approach further below.

For array-based test structures, the IR drop from the compensation point to the DUT may become even larger due to the extra parasitic resistance of the added transmission gates and routing paths used for the decoding and selection scheme. To reduce the measurement error caused by this large IR drop, an adaptive voltage-compensation scheme was proposed in [15], which utilizes two SMUs for each node of the measured MOSFET, as shown in Fig. 3. For each terminal of the DUT, one SMU (e.g., SMU1 for D, SMU3 for G, SMU7 for S, and SMU5 for sub) is used for forcing the voltage, which is then sensed by the other SMU (e.g., SMU2 for D, SMU4 for G, SMU8 for S, and SMU6 for sub). Fig. 4 lists the adjustment algorithm for finding a proper compensation voltage at each measured node. The approach of this algorithm is to incrementally increase the forcing voltage each time by a small step, and stop when the sensed voltage is equal to the reference voltage. The number of sweep steps of the forcing voltage determines the runtime and the accuracy of the adaptive voltage-compensation scheme. A small sweep step may result in a more accurate measurement, but it will also require longer runtime.

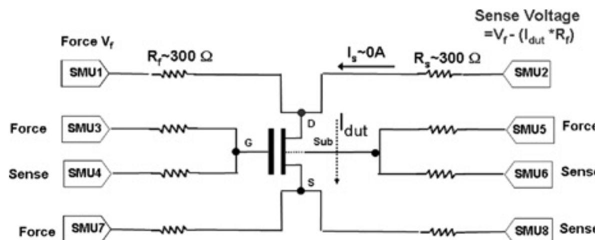

Fig. 3. Schematic of the adaptive voltage compensation for one DUT.

```
V_smu1= 1V , V_smu3= 1V , V_smu5= 0V , V_smu7= 0V
FOR I=1 TO N
    Force_v(smu1,V_smu1), Force_v(smu3,V_smu3)
    Force_v(smu5,V_smu5), Force_v(smu7,V_smu7)
  { Measure_V(smu2,V_d)
  { Measure_V(smu4,V_g)
  { Measure_V(smu8,V_s)
    V_ds=V_d-V_s
    V_gs=V_g-V_s
    V_bs=V_b-V_s
    if(V_ds== 1 && V_gs==1 && V_bs==0)
    then goto Start_Measure
    V_smu1= V_smu1 + 0.001
    V_smu3= V_smu3 + 0.001
NEXT I
Start_Measure Ion ...
```


Fig. 4. Pseudo code of adaptive voltage compensation algorithm for Ion measurement.

This adaptive voltage-compensation scheme is straightforward and easy to implement. However, it requires 8 SMUs per DUT and results in a high test-hardware overhead. Also, its adjustment algorithm may require too much time to search for the proper compensation voltages and may even be unable to converge. In fact, this adaptive voltage-compensation scheme only converges easily when the number of measured nodes is equal to two, such as for a diode or resistor. The difficulty of convergence increases when the number of compensation nodes increases. However, most FET characterization such as SPICE modeling is performed on discrete transistors, meaning that all four FET terminals (drain, gate, source, and bulk) need to be compensated. Therefore, the adaptive voltage-compensation scheme may not be practical for the applications described in this paper.

C. ROM-Like Transistor Array

Several test structures using ROM-like transistor arrays have been proposed in the past to measure a large number of DUTs within a close proximity [6], [12]. A ROM-like transistor array requires no periphery circuit for DUT selection and can avoid the extra parasitic resistance of the transmission gates as described in the previous subsection. Fig. 5 shows a ROM-like transistor array design in which transistors on a given column share a common drain bus, while each row of transistors shares a common gate bus. All transistors' source and bulk nodes are tied together with wide metal layers to minimize IR drop. The FET array layout permits each individual transistor to be accessed without periphery

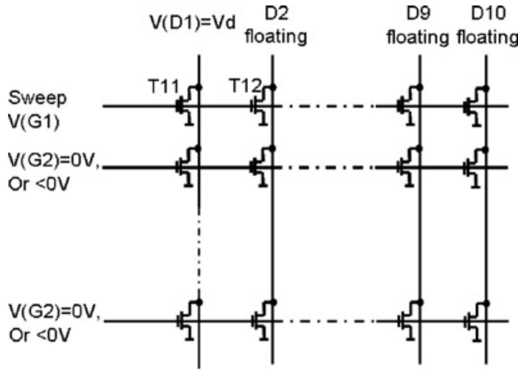

Fig. 5. Architecture of a ROM-like transistor array using shared common gate and drain buses [12].

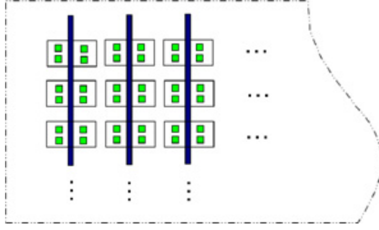

Fig. 6. Layout of a ROM-like DUT array using straight poly lines for gate connections [12].

circuitry. For example, while measuring FET T11, column 1 is biased and other drain columns are floating to reduce the diode leakage of the other transistors of columns 2 through 10. The voltages on other gate rows connected to T11 are biased at 0 V or a small negative voltage to turn off transistors and minimize the leakage in column 1 [12]. However, this design and biasing scheme still exhibits a major DC leakage current problem due to the use of common gate and drain busses, which results in an incorrectly measured value of Vt which is lower than the correct value obtained from a conventional single transistor testline. Traditionally, ROM-like open/short test structure arrays have been commonly used as test vehicles for defect monitoring during yield ramp [6]. The only ROM-like array structures which avoid this issue are open/short test structures evaluated by a strict pass/fail criteria, where the criteria for a short is a current level of order at least $\sim\mu$A. In addition, the layout style of a ROM-like transistor array, as shown in Fig. 6, cannot represent the end shortening and rounding effects of a poly gate used in actual product devices. Therefore, its measurement results may substantially deviate from the reality encountered in a product circuit.

III. Design Methodology

A. Design Architecture

Fig. 7 shows the proposed transistor array with 4 × 64 = 256 test units. Each test unit consists of eight transmission gates and one DUT. The DUT (usually a MOSFET) can be measured by selecting the corresponding test unit through the X-decoders and Y-decoders. In total, 8 address inputs (`X1-X2` and `Y1-Y6`) are used to select the 256 test units. Each test unit is designed with a stand-alone connection to its DUT, which means each of the drain, gate, source, and bulk nodes is connected to a SMU. This stand-alone connection can be used for the measurement of Isoff, Iboff, Igoff, or body bias of a DUT. Therefore, this test-unit design can also be modified to adapt to any type of device such as diode, resistor, pMOS, or nMOS, as long as the number of terminals connected to pads is less than or equal to four. The terminals `F1-F4 and S1-S4` are the SMU's forcing and sensing ports which are connected to the drain, gate, source, and bulk of a DUT, respectively. The proposed test structure with 256 DUTs can fit into a regular 1 × 22 pad frame used for a standard PCM testline. Also, the array size of the proposed test structure can be extended to 16 × 64 = 1024 to increase the sample size for statistical SPICE modeling or other applications requiring large sample size. However, the extended array cannot be placed in the scribe line for production variation monitoring due to its larger area.

Fig. 8 shows the test-structure layout in a $60 \times 2200\,\mu\text{m}^2$ region, where the size of each test unit is $30 \times 10\,\mu\text{m}^2$. Note that the shaded square in Fig. 8(c), representing the $\sim 10 \times 10\,\mu\text{m}^2$ area immediately surrounding the DUT, may be designed with a layout representing a typical circuit environment, or with a layout deliberately varying one or more layout parameters. This can be accomplished without compromising the low series resistance of the wiring to the DUT terminals. Because most stress-related layout effects occur over length scales less than $\sim 5\,\mu$m, the layout-induced stress on the DUT can easily be made identical to a typical circuit layout. In this proposed test structure, the circuit-under-pad (CUP) design technique is used to increase the number of DUTs placed in this $60 \times 2200\,\mu\text{m}^2$ region. Note that this CUP design technique requires a process with at least four metal layers. By using the CUP design, the bottom few metal and via layers (metal-1 to metal-4) in the pad frame are removed. The active circuitry including test devices are all placed under the bond pads. Using the CUP design, the number of placed DUTs is increased by a factor of 2.5. In addition, all periphery circuits, such as latches and decoders, are designed with I/O devices rather than core logic transistors so that their background leakage can be reduced and their performance will not be affected by the process variation of the advanced process under study. For the technologies under study, V_{dd} = 1.0 V for the core logic transistors, and V_{dd} = 2.5 V (or optionally 1.8 V) for the IO devices. In the examples discussed in this paper, we focus on the case where the DUT is a core logic transistor, but the techniques are equally applicable to the case where the DUT is a 2.5 V (or 1.8 V) IO device as long as the periphery circuits are overdriven to 3.3 V (or 2.5 V).

B. Hardware IR Compensation

A hardware IR-compensation technique is used in the proposed array-based test structure to reduce measurement error caused by the large parasitic resistance of the added transmission gates and routing paths. The key concept of this hardware IR compensation is to separate the forcing and sensing paths originally connected at the probe card (as shown Fig. 2), and reconnect them at a position very close to the DUT. Such a connection can reduce the parasitic resistances between

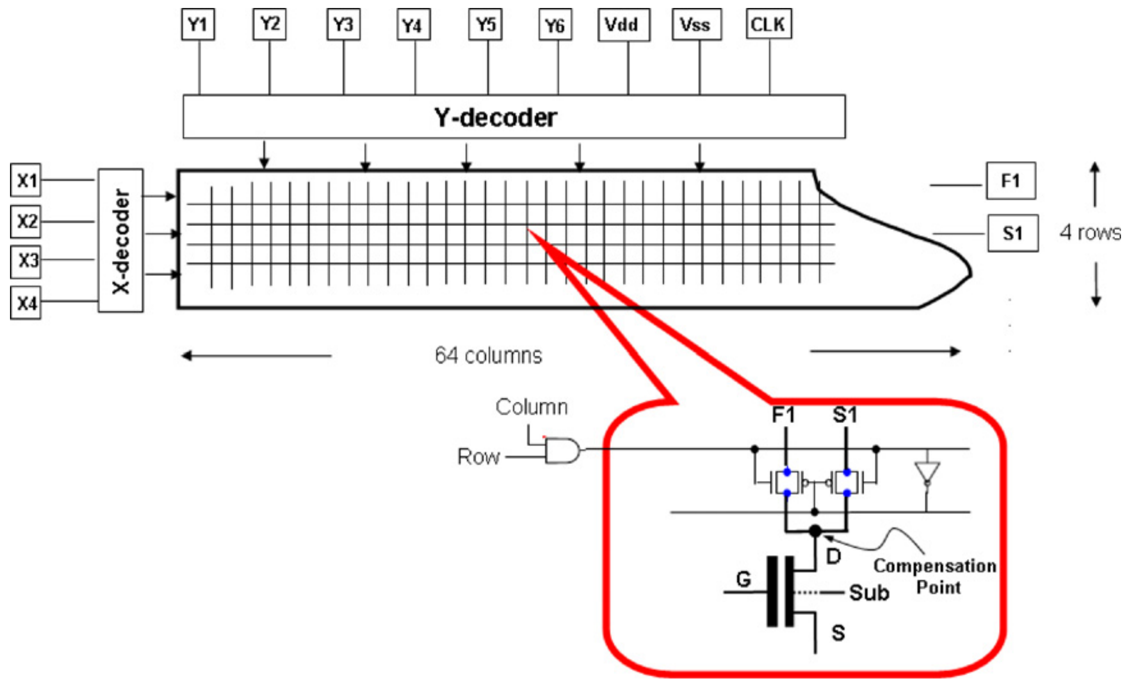

Fig. 7. Architecture of the proposed transistor array with 4 × 64 DUTs for scribe-line-compatible footprints.

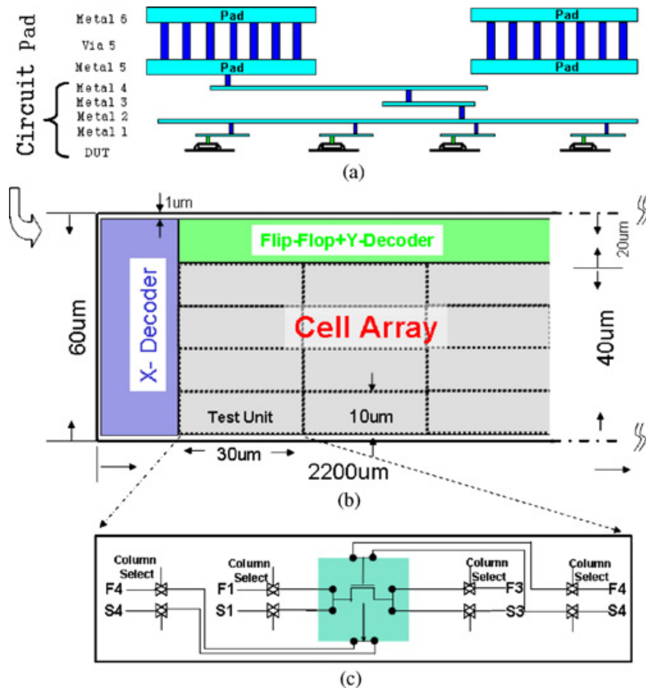

Fig. 8. Layout of the proposed test structure using circuit-under-pad design (CUP) for scribe-line compatible footprints. (a) Cross-section view of CUP design. (b) Top view of the proposed test structure. (c) Schematic inside each test unit.

a compensation point and its corresponding DUT. In our test structure, the approximate distance between the compensation point and DUT is less than 2 μm. Thus, the parasitic resistance between compensation point and DUT is significantly lowered. For example, using typical metal resistance values, the parasitic resistance for each connection can easily be reduced to $\sim 0.2\,\Omega$ which is substantially lower than 1–30 Ω for a conventional PCM test-line as described in Fig. 2. Fig. 9 shows the whole configuration of the proposed setup, which contains the enhanced Kelvin connection, Agilent 407X SMUs, and a redesigned compensation point. All the DUT's terminals including drain, source, gate, and bulk are compensated by this enhanced Kelvin connection to ensure measurement accuracy. The measurement error for the configuration of Fig. 9 can be calculated by the following equations. We note that because R_i is much larger than R_s and R_f, to simplify the calculation, the negligible current flowing through R_i is taken to be zero

$$V_{sense} = V_{set} \tag{1}$$

$$\begin{aligned} Error &= V_{set} - V_{dut} \\ &= V_{drops} \\ &= V_{dropf} \cdot \frac{R_s}{R_s + R_i} \\ &= I_{dut} \cdot R_f \cdot \frac{R_s}{R_s + R_i}. \end{aligned} \tag{2}$$

As (2) shows, the compensation error increases as I_{dut} increases. In order to address this compensation error when I_{dut} is high, we can either reduce the parasitic resistances R_s and R_f by layout engineering, or increase the internal resistance R_i at the SMU. To reduce R_s and R_f, we can increase the size of a transmission gate such that its channel resistance is reduced, or increase the metal routing width. However, a larger transmission gate results in larger leakage [14], and wider metal routing requires more layout space. Therefore, in our hardware compensation, we choose to increase the SMU's internal resistance R_i to limit the measurement error.

Increasing R_i lowers the difference between V_{dut} and V_{set}. Typically, the SMU's internal resistance in an Agilent 407X tester is a few kiloohms. For instance, with V_{dut} of 1 V, the error percentage with a 10 kΩ R_i and a 300 Ω R_s is

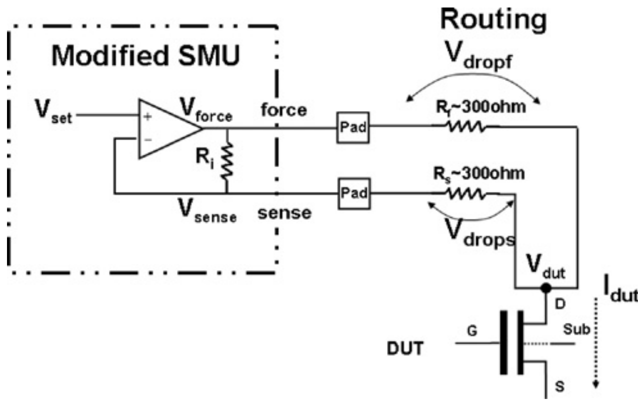

Fig. 9. Schematic of the proposed hardware IR-compensation mechanism.

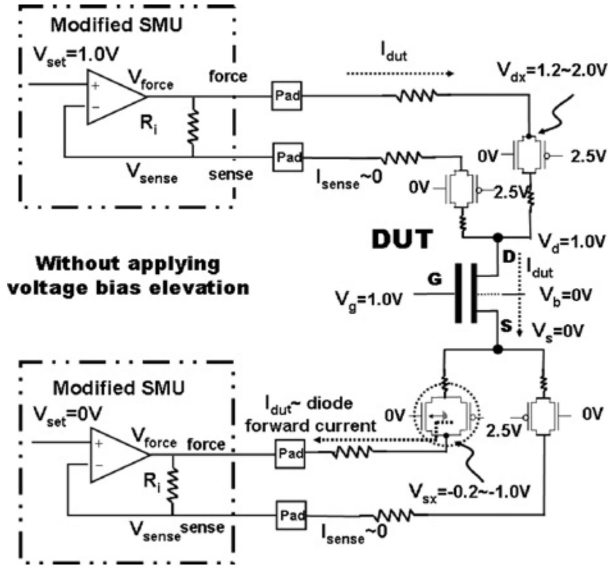

Fig. 10. Example of the negative node created without applying the proposed voltage bias elevation technique.

approximately 870 $\Omega\,(I_{dut}/1\,\mathrm{V})\%$. This error percentage can be reduced to 45 $\Omega\,(I_{dut}/1\,\mathrm{V})\%$ if R_i is increased to $200\,\mathrm{k}\Omega$. Since the maximum I_{dut} for most typical device measurements is approximately 2 mA, the worst case error percentage can be improved from 1.57% to less than 0.09%, if R_i is increased from $10\,\mathrm{k}\Omega$ to approximately $200\,\mathrm{k}\Omega$. The error percentage slightly increases with I_{dut} for wide device width (>2 μm). However, a 2 mA maximum current level is adequate for most applications such as SPICE modeling, process diagnostics, stress, DFM, and variation characterization. For a worst case of DUT measurement with $I_{dut} = 10\,\mathrm{mA}$, $R_i = 200\,\mathrm{k}\Omega$, and $R_s = R_f = 300\,\Omega$, the error will be smaller than 0.44%, which is superior to either a conventional PCM or adaptive voltage compensation. However, increasing R_i results in larger voltage convergence time. This technique should, therefore, be used with caution.

C. Voltage Bias Elevation for Measuring Ion

In the previous subsection, we introduced the use of the proposed hardware IR compensation to achieve high measurement accuracy, especially when I_{dut} is high. However, as shown in

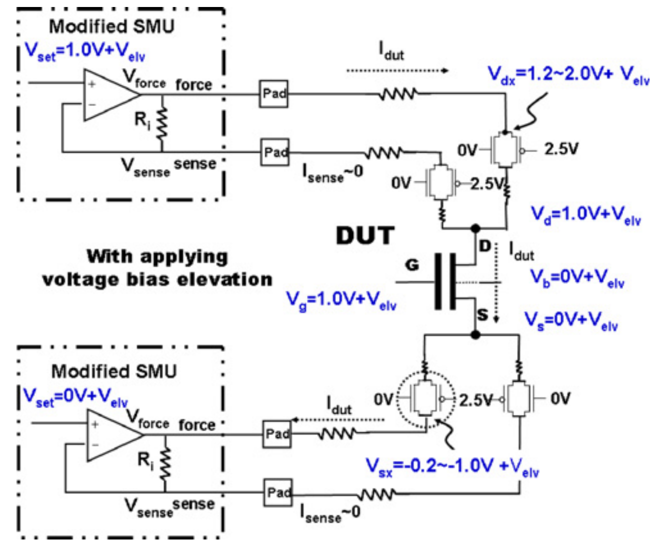

Fig. 11. No forward biased current on the transmission gate is generated after applying voltage bias elevation (V_{elv} = 0.5 V).

Fig. 10, the proposed IR compensation technique may create a negative node V_{sx} beside the transmission gate on the force path of the DUT's source side. During the IR compensation, the value of V_{sx} depends on I_{dut} and the parasitic resistance of metal routing and transmission gates, R_s. V_{sx} is in the range of ~ -0.2 to ~ -1.0 V in the example of Fig. 10. Thus, if I_{dut} or R_s become too large, V_{sx} at the transmission gate's input node will become a large negative voltage, which may turn on the diode from source to substrate on the transmission gate and result in malfunction if V_{sx} is below -0.6 V.

Considering the case of I_{on} measurement for a core logic transistor with V_{dd} = 1.0 V for example, before the OP Amp settles, the voltage at the drain compensation point would initially be below 1.0 V due to the IR drop. V_{force} would continue increasing until the voltage of the compensation point V_{dut} reaches 1.0 V. V_{force} would be elevated to approximately 1.0 V + $I_{dut}*R_f$. This does not present a problem on the forcing path of the DUT's drain side as long as V_{dx} is still below V_{dd} (i.e., 2.5 V). However, it would cause a negative node on the force path of the DUT's source side. The source-voltage setting of the DUT is 0 V for Ion measurement. The voltage at the input of the transmission gate would thus be decreased below the diode's turn-on voltage (about -0.6 V) due to the parasitic resistance of metal routing and transmission gates, especially when I_{dut} is high. This would turn on the transmission gate's drain to bulk diode. As shown in the following equation, V_{sx}, and a corresponding "elevation" voltage V_{elv}, can be roughly calculated given I_{dut}, the diode's turn-on voltage V_{dt}, and the transmission gate resistance R_{TG}

$$
\begin{aligned}
V_{sx} &= I_{dut} \cdot 2 \cdot R_{TG} > -V_{dt} \\
V_{elv} &= -V_{sx}.
\end{aligned}
\tag{3}
$$

If $V_{sx} < -V_{dt}$, the current measured by the SMU would be the diode's forward biased current, not the DUT current. To prevent this, the voltage biases of all the DUT's terminals are elevated to a positive voltage V_{elv} during I_{on} measurement to eliminate the negative voltage at the source path. This

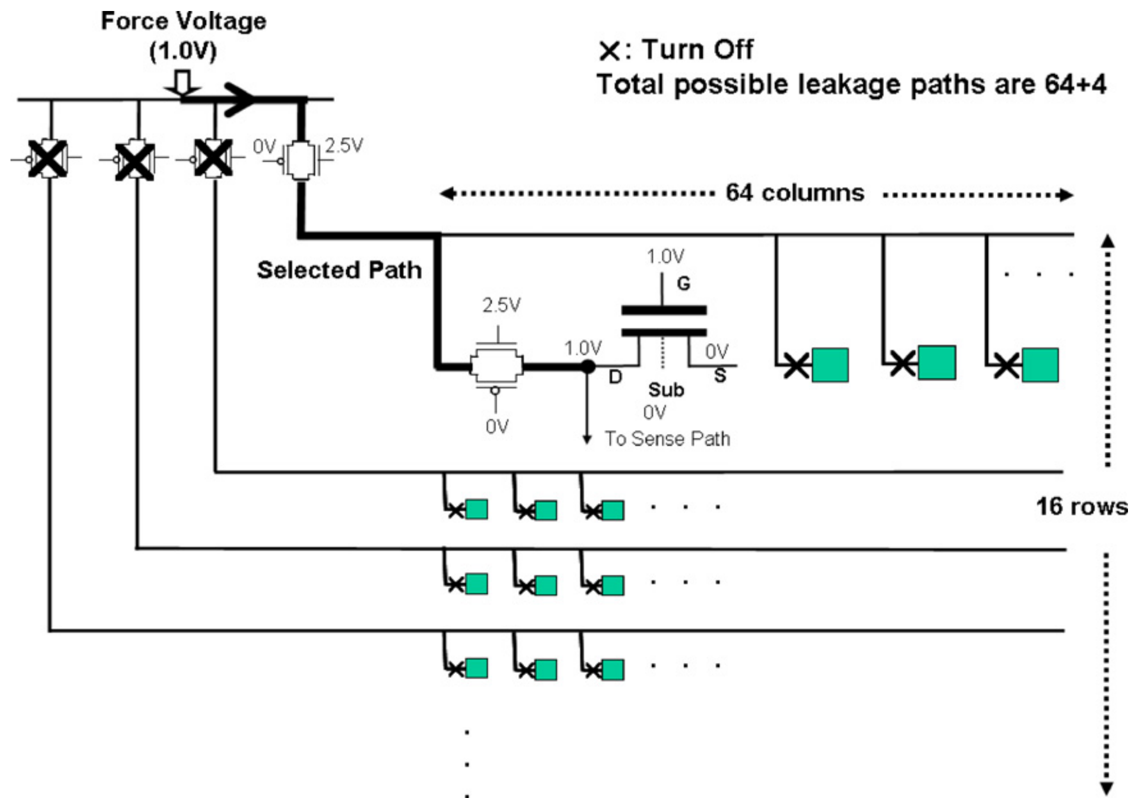

Fig. 12. Possible leakage paths in the proposed array-based test structure. The thick line indicates the selected path. The background leakage current includes the leakage from both the selected and unselected paths.

bias voltage V_{elv} is applied to V_{set} (thus also increasing V_{dx}), V_g, V_d, V_s, and V_b. The elevated voltage does not affect the electrical behavior of the measured DUT because the same voltage elevation is applied to all terminals concurrently. In addition, the power supply of the periphery circuitry can be overdriven to 3.3 V to enlarge the compensation margin, i.e., 3.3/2.5 V V_{DD} for a 2.5/1.8 V I/O process. Figs. 10 and 11, respectively, show an example without and with application of voltage bias elevation.

D. Leakage-Current Cancelation for Measuring I_{off}

Another important MOSFET parameter to be measured is the off-state leakage current I_{off}. When measuring current, a SMU senses not only the DUT current, I_{dut}, but also the leakage current from periphery circuitry. For I_{on} measurement, the leakage current from peripheral circuitry does not affect the measurement accuracy since this leakage current is much smaller than I_{on}. However, this leakage current can significantly affect the accuracy of I_{off} measurement. The sources of this leakage current include: 1) the leakage from peripheral circuitry transistors, and 2) the leakage from the transmission gates on selection paths. The second of these typically dominates the total leakage current. The leakage current from the transmission gates may result from the N+/PW and P+/NW junction leakage, and gate to drain leakage on both the pMOS and nMOS of the transmission gates. There are $64+4$ leakage current paths created by the transmission gates in the proposed test structure as shown in Fig. 12 (64 gates for each column and 4 gates for each row).

In order to reduce the current from these leakage paths, we use I/O devices (having relatively thicker gate oxide and longer channel length) for designing the periphery circuitry. Also, we propose a leakage-current-cancelation technique for our array-based test structure. This leakage-current cancelation elevates all the DUT's terminals to an optimal voltage, similar to the voltage elevation technique described in the previous subsection. The operating principle of this leakage-current cancelation is to set the voltage of the DUT's drain node such that leakages from the nMOS and pMOS of each transmission gate on the 68 leakage paths can be balanced. Figs. 13 and 14, respectively, illustrate the leakage current before and after employing the voltage elevation technique. Before voltage elevation, the voltage difference from the DUT's drain to both the nMOS gate and the pMOS substrate is 1.5 V, but the voltage difference from the DUT's drain to both the nMOS substrate and the pMOS gate is only 1.0 V. This unbalanced voltage difference may result in a large current on this transmission gate as shown in Fig. 13. After the voltage of the DUT's drain is elevated to an optimal value, the voltage differences from the DUT's drain to each nMOS or pMOS gate, or to the substrate, are all equal, such that the leakage currents from this transmission gate cancel out one another as illustrated in Fig. 14.

If all transmission gates were perfectly fabricated, all nMOS and pMOS should be completely symmetric. In this ideal case, the optimized voltage at the DUT's drain should be half of the transmission gate V_{DD}, i.e., 1.25 V in our example. However, in reality the fabrication of each transmission gate

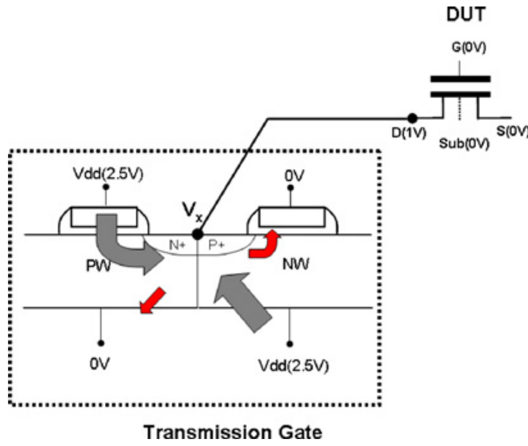

Fig. 13. Larger background leakage due to unbalanced leakage paths before applying voltage bias elevation.

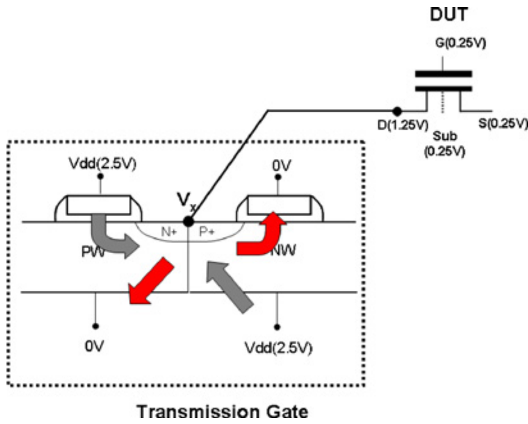

Fig. 14. Reducing the leakage current by balancing the leakage paths with optimized voltage bias elevation.

is also affected by process variation. Thus, when measuring I_{off}, the values of both V_{DD} and the elevated voltage at the DUT's terminals may be swept to find an optimal voltage to minimize the leakage current from the 68 leakage paths during the measurement. The background leakage can be optimized by offsetting the drain voltage slightly from half V_{DD}. Fig. 15 plots I_{off} as a function of the drain voltage offset from half V_{DD} for the 64 DUTs in the array for one wafer (9 die tested on each wafer, with 1 array in each die). Typically, the minimum DUT off current can be obtained at a drain voltage fairly close to half V_{DD}. In this example, the sweep confirmed that the optimal voltage was quite close to half V_{DD}, as I_{off} is observed to significantly increase with a non-zero offset voltage. However, the optimal drain voltage might not be exactly half V_{DD} for all processes. It might be slightly above or below half V_{DD} for different processes depending on the difference between the NMOS and PMOS gate and junction leakage in the transmission gates, and sweeping the offset voltage as done in Fig. 15 permits confirmation or correction of the optimal offset voltage. Of course depending on the range and resolution of the offset voltage sweep, additional test time will be required to obtain this data. In this example, based on the data of Fig. 15, a voltage of half V_{DD} was determined to be adequate. We further emphasize that because long-

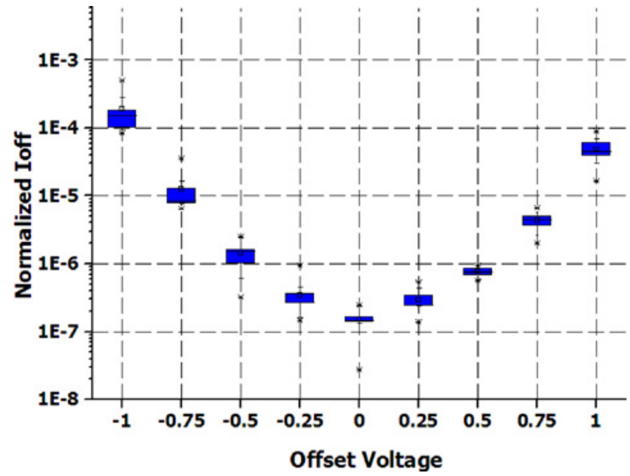

Fig. 15. Background leakage reduction by offset voltage from half V_{DD} for the 64 DUTs in the array for 1 wafer (9 die/wafer with 1 array/die).

channel thick-oxide IO transistors are used in the transmission gates, the offset voltage is relatively insensitive to process variation. In practical applications, a quick confirmation of the optimal offset voltage can be obtained with two additional I_{off} measurements, i.e., for positive and negative values of a single offset voltage. Further adjustment of the offset voltage needs only be performed if it is shown to be necessary by these two measurements, in which case the offset voltage can be adjusted iteratively to minimize I_{off} to the desired precision, at the cost of 2 additional I_{off} measurements for each successive iteration. Because the need for offset voltage adjustment results from leakage imbalance in the periphery circuits, and these are long wide IO devices relatively less susceptible to local process variation, if such adjustment is necessary, it is likely to only be needed once for each DUT array. Local process variation causes variation in I_{off} for different DUTs in the same array, but it is unlikely to affect the offset voltage which must be applied to the periphery to minimize the measured I_{off} value.

IV. Experimental Results

A. Proposed Test Structure Versus Traditional PCM Testline

In the first experiment, a traditional PCM testline is fabricated adjacent to the proposed array-based test structure in a mature, relatively old process technology. In traditional PCM testlines, several types of devices with different dimensions are fabricated, such as MOSFET, RC, RS, and diode. We choose a DUT from the proposed DUT array closest to the DUT with the corresponding device type and dimension in the PCM testline, and then measure both of these two DUTs. The electrical properties of these two DUTs should be similar since the local process variation of this mature process technology is small.

Fig. 16 plots the drain current (I_d) versus the gate voltage (V_g) of the chosen DUT measured by each test structure. Curve A represents the I_d measured by the traditional PCM testline, which is considered as the reference measurement result. Curve B represents the I_d measured by the proposed array-based test structure. As shown by curves A and B, the I_d

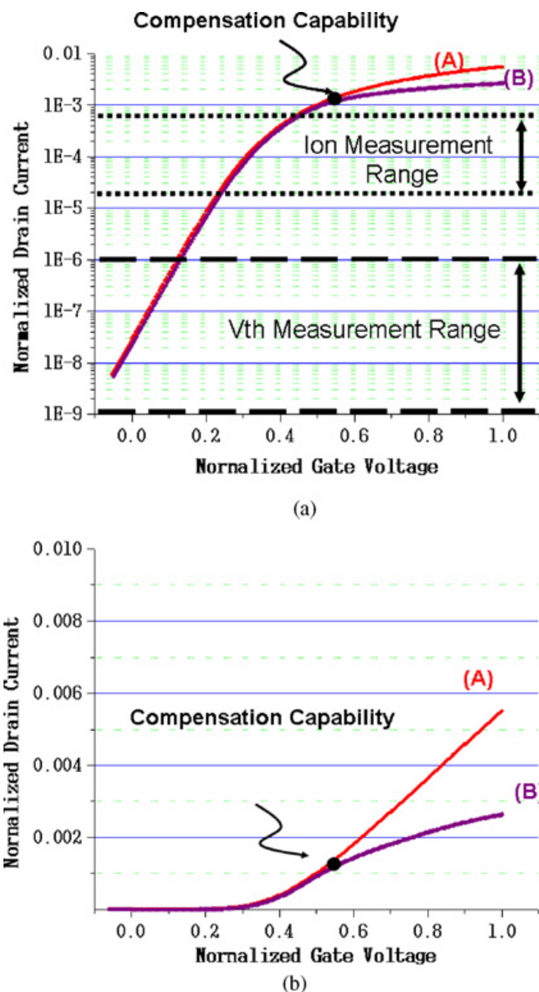

Fig. 16. I_d versus V_g measured by (a) a PCM testline and (b) proposed array-based test structure with log scale (upper figure) and linear scale (lower figure).

measured by the proposed test structure closely matches the I_d measured by the traditional testline when the normalized I_d is smaller than 10^{-3}(A.U), which covers the I_d range for measuring both the threshold voltage V_{th} and the saturation current I_{on}. Thus, the result shown in Fig. 16 demonstrates the measurement accuracy of the proposed array-based test structure for measuring V_{th} and I_{on}. Note that the I_d range for measuring I_{on} is in general below 1 mA for advanced technologies. The proposed test structure can allow I_d measurement up to 2 mA.

Next, we fabricate both test structures on an advanced, newly developed process technology and measure 9 traditional PCM testlines and 9 replicates of the proposed test structure over a wafer as shown in Fig. 17, which represents the typical sampling distribution of measured PCM testlines. On each chip, the proposed test structure is placed adjacent to the measured PCM testline. Fig. 18 plots I_{on} versus V_{th} for the DUTs measured from each PCM testline and from the proposed test structure. As shown by Fig. 18, the I_{on} and V_{th} measured by PCM testlines are all within the distribution of the I_{on} and V_{th} measured by the proposed test structure, meaning that the measurement accuracy of the proposed test structure is very close to that of the traditional PCM testlines.

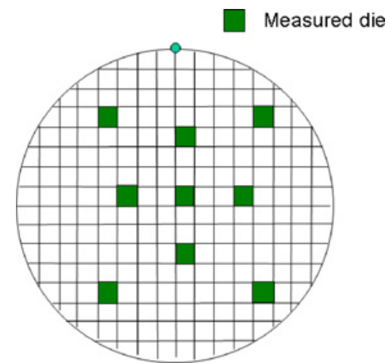

Fig. 17. Locations of measured test structures.

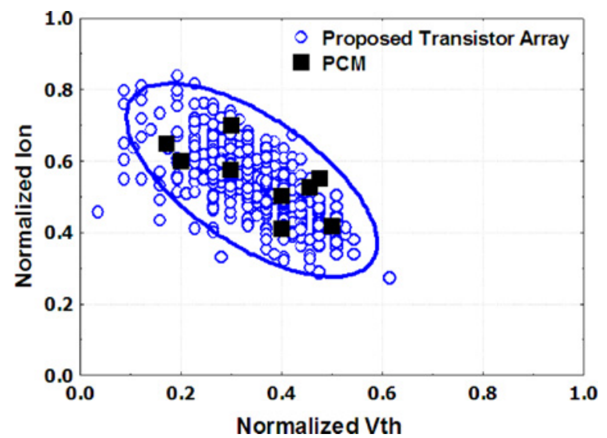

Fig. 18. I_{on} and V_{th} of each DUT measured by 9 PCM testlines and 9 proposed test structures. The curve is an elliptical fit of the 95% confidence interval of the data set.

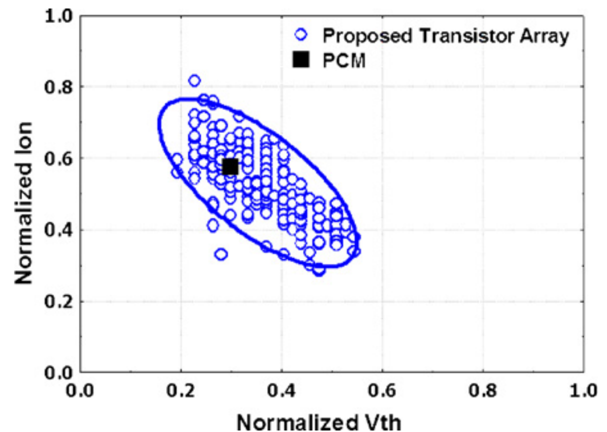

Fig. 19. I_{on} and V_{th} of each DUT measured by only one PCM testline and one proposed test structure. The curve is an elliptical fit of the 95% confidence interval of the data set.

In addition, by using only the PCM testlines, the extent of the global variation on this wafer can be roughly observed, which is also one of the objectives of traditional PCM testlines.

However, the traditional PCM testlines fail to capture the local process variation. Fig. 19 plots I_{on} versus V_{th} of DUTs measured from only one PCM testline and its adjacent proposed test structure, demonstrating that the variation of

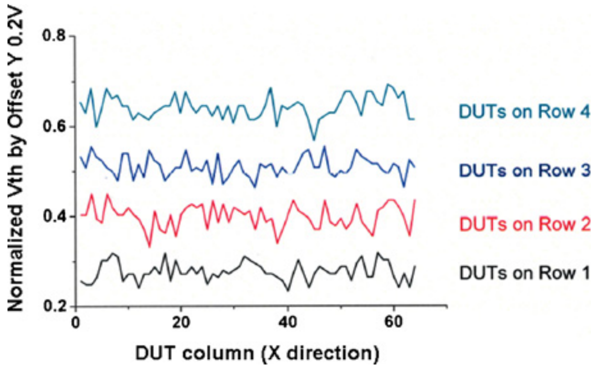

Fig. 20. V_{th} versus DUT column (x-axis) for all four rows of the structure, with each row shifted by a fixed offset along the y-axis.

the DUT's I_{on} and V_{th} within the proposed DUT array is significant, but the PCM testline can only measure one sample from this distribution. This result further shows the necessity of an effective array-based test structure to measure a large number of DUTs in close proximity, such that local variation can be accurately characterized. In Fig. 20, we plot V_{th} versus DUT column (x-axis) for all four rows of the structure. No spatial dependence is evident, indicating that the data truly characterizes the local random variation of the process.

B. Effectiveness of Hardware IR Compensation

In the following experiment, we measure the same DUT using the same proposed array-based test structure as that in Fig. 21 but without applying the hardware IR compensation introduced in Section III-B, i.e., we use the SMUs' connection shown in Fig. 9, but the internal resistance of the SMUs remains unchanged. In Fig. 21, curve C represents the I_d measured by the proposed test structure without hardware IR compensation. As curve C shows, its measured I_d matches the reference result in the sub-threshold region. However, its measured I_d deviates from the reference result when the normalized I_d is larger than 10^{-4}, which falls in the current range required for measuring I_{on}. This measurement error results from the parasitic resistance of the transmission gates on the selection paths. Thus, without applying hardware IR compensation, the measured error of I_{on} can be quite large.

Fig. 22 further illustrates this error in I_{on} by plotting I_{on} versus V_{th} for each DUT measured by the proposed test structures with and without applying hardware IR compensation. As shown in Fig. 22, the V_{th} distributions measured with and without hardware IR compensation are similar (see their X-coordinates). However, the I_{on} values measured without hardware IR compensation are significantly lower than those obtained using hardware IR compensation (see their Y-coordinates). This is because the I_d for measuring I_{on} is much higher than that for measuring V_{th} and may result in a significant IR drop if no IR compensation is applied. The result shown in Fig. 22 again demonstrates the importance of applying the proposed IR-compensation scheme.

C. Effectiveness of Leakage-Current Cancelation

As discussed in Section III-D, the proposed leakage-current cancelation can significantly reduce the background leakage

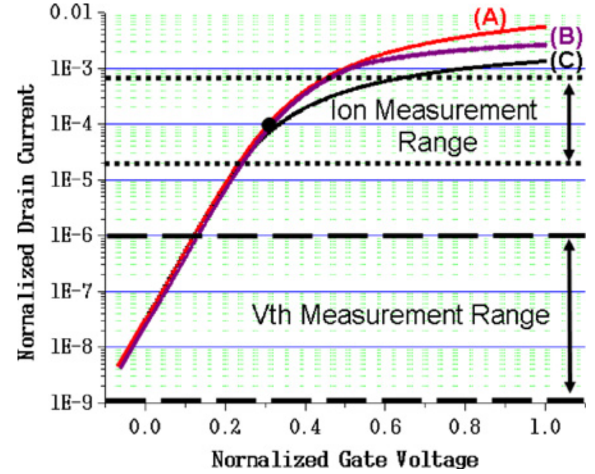

Fig. 21. I_d versus V_g measured by (A) a PCM testline, (B) a proposed array-based test structure, and (C) a proposed array-based test structure without applying hardware IR compensation.

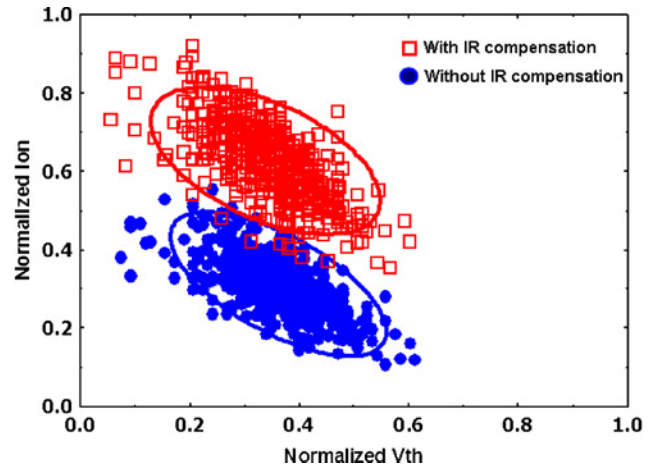

Fig. 22. I_{on} and V_{th} of each DUT measured by proposed test structures with and without the hardware IR compensation. The curves are elliptical fits of the 95% confidence intervals of the two data sets.

from transmission gates by elevating the voltage at each terminal of a DUT to an optimized value. Fig. 23 plots the I_{on} and I_{off} of each DUT measured by the proposed test structures with and without applying the current-cancelation technique. As shown in Fig. 23, the I_{off} measured with current cancelation applied ranges over a wide interval (from −8 to −4 A.U.). However, the I_{off} measured without current cancelation is uniformly high, in a small interval (from −5 to −4 A.U.). This result shows that if the current-cancelation technique is not employed, the leakage current from the transmission gates may dominate the I_{off} measurement and hence the true I_{off} distribution cannot be measured.

D. Proposed Array Versus ROM-Like Array

In the following experiment, we fabricate the proposed array-based test structure next to a ROM-like array-based test structure, using a mature, relatively old process technology. Both test structures can be placed into a standard scribe line for monitoring process variation. Similar to Fig. 16, we choose two nearby DUTs for measurement, one from each test

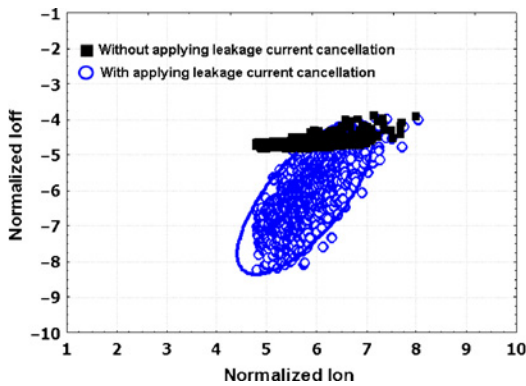

Fig. 23. I_{on} versus I_{off} of each DUT measured by the proposed test structures with and without applying the current-cancelation technique.

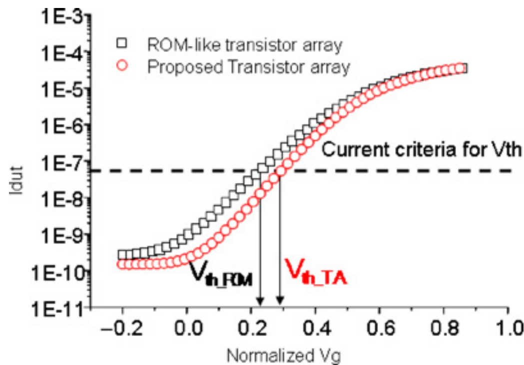

Fig. 24. I_d versus V_g measured by a ROM-like DUT array and a proposed DUT array.

structure. Fig. 24 plots the I_d versus V_g of the chosen DUT measured by each test structure. Compared to our proposed test structure, the I_d measured by the ROM-like test structure is larger, and hence its measured V_{th} is smaller. This difference results from the larger leakage current of the common-gate and common-drain buses in the ROM-like transistor array, which shows the potential measurement error from modifying a DUT's layout for characterization of process-variation.

Next, we fabricate these two array-based test structures in an advanced, newly developed process technology. Fig. 25 plots the I_{on} and V_{th} measured on each DUT of both test structures. The median and variance of V_{th} measured by both test structures are listed in the upper-right corner of Fig. 25. Compared to the proposed test structure, the V_{th} measured by the ROM-like test structure is approximately 10% smaller, which is consistent with the result shown in Fig. 24. Also, the V_{th} variation measured by the ROM-like test structure is about 12% smaller. This smaller V_{th} variation results from the fact that the long straight poly line gate busses used in the ROM-like transistor array do not suffer the shortening and rounding effects which occur in the short poly gates of both the proposed transistor array and typical real product circuits. Therefore, the V_{th} variation measured from a ROM-like test structure may be unrealistically smaller than the variation which occurs in a real circuit.

E. Hardware IR Compensation Versus Adaptive Voltage Compensation

Hardware IR compensation is one key technique to ensure the measurement accuracy of an array-based test structure. In

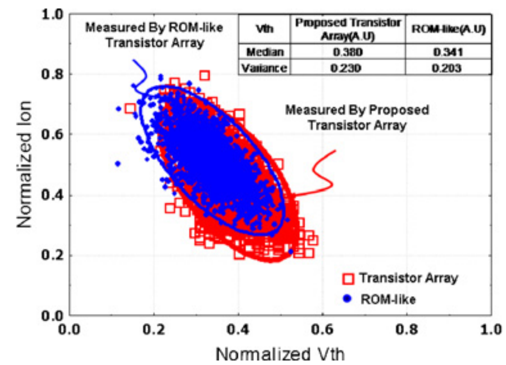

Fig. 25. I_{on} versus V_{th} of each DUT measured by a ROM-like DUT array and a proposed DUT array.

TABLE I
COMPARISON BETWEEN HARDWARE IR COMPENSATION AND ADAPTIVE VOLTAGE COMPENSATION

	Adaptive Voltage Compensation	Hardware IR Compensation
# of SMU required	8 (each MOSFET)	4 (each MOSFET)
Accuracy	Depends on sweep step	>99.991%
Convergence time	Slow	Fast
Testing time	~500 ms	~10 ms

this subsection, we compare the proposed hardware IR compensation with the adaptive voltage compensation introduced in Section II-B. Table I summarizes the comparison between the two IR compensation schemes. First, the hardware IR compensation requires half as many SMUs per DUT compared to adaptive voltage compensation. Second, the measurement accuracy of hardware IR compensation can be calculated by (2) and further controlled by modifying the internal resistance of the SMUs. The measurement accuracy of the adaptive voltage compensation is controlled by the size of the sweep step. A smaller sweep step can increase the measurement accuracy, but only at the cost of increased test time. Next, hardware IR compensation requires no sweeping of the forcing voltage and hence results in a faster convergence time. Last, the test time for measuring a DUT with hardware IR compensation is around 10 ms, which is 50× smaller than that with adaptive voltage compensation. This short test time and high measurement accuracy further demonstrates the efficiency and effectiveness of the proposed hardware IR-compensation scheme. To illustrate the impact of this reduction of test time, we note that to obtain the 256 data points for each data set in Fig. 21, 128 s is required for measurement using adaptive voltage compensation, as compared to only 2.56 s using hardware IR compensation.

F. Local Mismatch Measured by Proposed Test Structure

Accurate matching of active and passive devices is critical for analog and mixed-signal circuits, which usually require a high level of precision. As process variation becomes larger in advanced process technologies, the degree of mismatch on devices actually determines and limits the performance of analog and mixed-signal circuits [16]–[18]. To measure mismatch in a process technology, two nominally identical

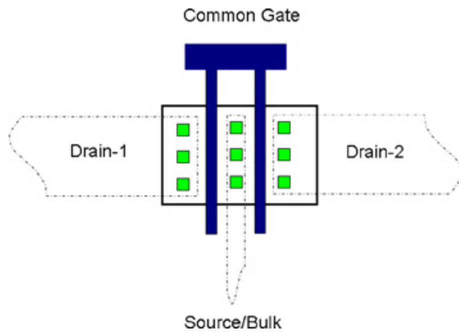

Fig. 26. Layout of a paired-transistor DUT.

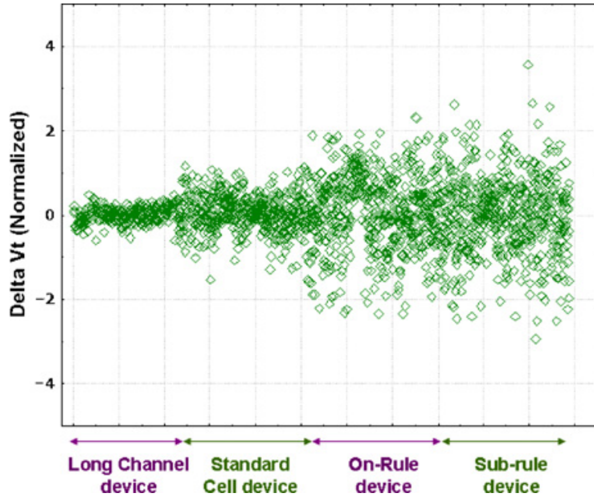

Fig. 27. V_{th} mismatch of paired MOSFETs measured by the proposed test structures for different W/L dimensions.

MOSFETs directly adjacent to each other are fabricated and then measured. The physical difference between these two nominally identical MOSFETs is defined as *local mismatch*. In this subsection, we utilize the proposed array-based test structure to collect mismatch data for a large number of pairs of adjacent MOSFETs.

In order to place a pair of identical MOSFETs into a test unit shown in Fig. 8, the number of DUT terminals connected to pads must be less than or equal to four. Fig. 26 shows the DUT design used in our array-based test structure for measuring local mismatch. As Fig. 26 shows, the two MOSFETs are symmetric and share a common gate and source. Also, the source and bulk of each MOSFET are tied together to save another terminal connection to a pad. When measuring the V_{th} of the left (right) MOSFET, we float Drain-2 (Drain-1), apply voltages to the common gate in a sweep step, ground the common source/bulk, and sense the current at Drain-1 (Drain-2).

In the following experiment, we fabricate the proposed array-based test structures to measure local V_{th} mismatch on an advanced process technology. Each test structure contains 256 paired MOSFETs, which include the following four device dimensions (listed in order of decreasing channel area): long-channel devices, standard-cell devices, on-rule devices, and sub-rule devices. For each dimension, 64 paired MOSFETs are included. Fig. 27 shows the difference of the normalized V_{th} between each of the paired MOSFETs for each dimension. The

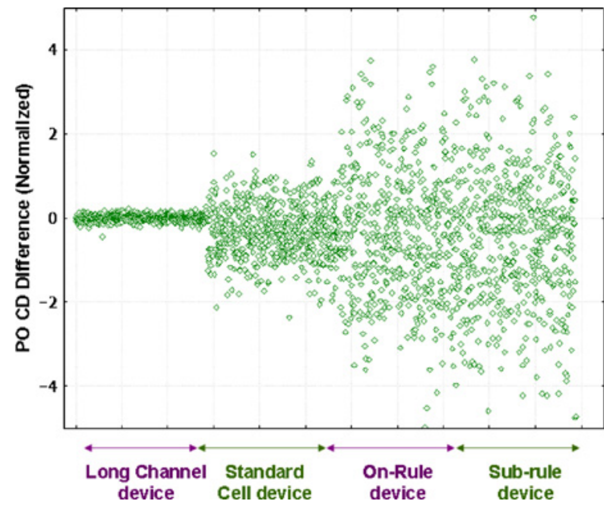

Fig. 28. Poly-CD mismatch of paired MOSFETs measured by scanning electron microscope for different W/L dimensions.

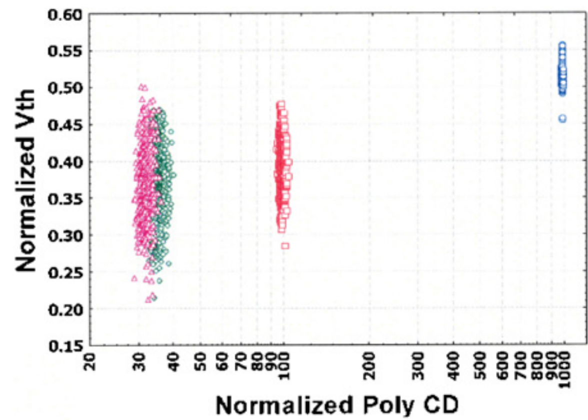

Fig. 29. V_{th} versus poly CD for all MOSFETs in the array of MOSFET pairs.

V_{th} mismatch significantly increases when the channel area decreases, consistent with the theoretical behavior of random dopant fluctuation [19].

V_{th} mismatch also depends strongly on the difference in the poly gate critical dimension (CD) between the two devices. We use an in-line scanning electron microscope to physically measure the poly CD difference between each of the paired MOSFETs. Fig. 28 plots this physically measured mismatch of poly CD for the same group of paired MOSFETs shown in Fig. 27. Fig. 29 in turn plots V_{th} versus poly CD for all MOSFETs in the group of MOSFET pairs. The physical poly-CD mismatch shown in Fig. 28 and the spread of the V_{th} populations in Fig. 29 indeed correlates with the electrical V_{th} mismatch shown in Fig. 27, which confirms that local poly CD difference is one of the sources of this V_{th} mismatch. The measurement results in Figs. 27 and 28 demonstrate that the mismatch between paired MOSFETs may significantly vary within a close proximity (note that the distance between two DUTs, i.e., two MOSFET pairs, in the proposed test structure is 30 μm). In addition, the strong correlation between our electrical and physical measurements again demonstrates the accuracy and effectiveness of the proposed array-based test structure.

V. Conclusion

In this paper, we successfully developed an array-based test structure and a corresponding novel test methodology for overcoming the IR-drop from parasitic resistance and the leakage current from the control circuitry, which are challenges inherent to any array-based characterization technique. We introduced the technique of hardware IR compensation to address the parasitic IR drop, and the combination of voltage bias elevation and leakage current cancelation to perform efficient, highly accurate current measurements on a large device array. The proposed array-based test structure can fit into the pad frame of a traditional PCM testline and can be placed on a scribe line for production process monitoring. Measurements with the proposed structure have demonstrated accuracy comparable to the PCM testline, but a much larger data volume can be gathered with the same pad frame area. Also, its DUT array size can be further extended for statistical SPICE modeling. A series of experiments were conducted on both mature and newly developed process technologies to validate the effectiveness and the superiority of the overall proposed test structure and methodology. As one example of the application of this technique to perform valuable process characterization, we demonstrate the use of a version of this structure to collect local V_{th} mismatch data for an array of MOSFET pairs.

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Tseng-Chin Luo received the M.S. degree in material science and engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1994, and is currently pursuing the Ph.D. degree in electrical engineering from the same university.

He joined Winbond Electronics Corporation, Hsinchu, in 1996, and then transferred to World-wide Semiconductor Manufacturing Corporation, Hsinchu, in 1997. His major focus was parametric testing and process integration during this period. Since 1998, he has been developing processes for 0.18 μm and 0.13 μm technology with the Logic Technology Research and Development Division, Taiwan Semiconductor Manufacturing Corporation (TSMC), Hsinchu. More recently, he has focused on developing test structures as well as fast test methodology for process characterization, design manufacturing, and yield optimization. Also, the corresponding infrastructures have been established to improve design effectiveness and analysis quality. He is currently the Project Manager of Fast Parametric Testing Solutions with TSMC.

Mango C.-T. Chao received the B.S. and M.S. degrees from the Department of Computer and Information Science, National Chiao Tung University, Hsinchu, Taiwan, in 1998 and 2000, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of California, Santa Barbara, in 2006.

He then joined the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Assistant Professor. His current research interests include memory testing, on-chip test compression/decompression, WAT test-structure design, power-related testing, and physical design automation.

Michael Shien-Yang Wu received the Ph.D. degree in electrical engineering from the University of Wisconsin-Madison, in 1992.

He has been with the Taiwan semiconductor industry for more than 18 years. After four years of work experience in the first DRAM joint venture of TI-Acer, Inc., Hsinchu, Taiwan, from 1993 to 1996, he joined the Research and Development Organization, Taiwan Semiconductor Manufacturing Corporation (TSMC), Hsinchu, participating in the development areas of device modeling and 130 nm/90 nm/65 nm advanced logic process technology. In 2004, he completed the EMBA Program in the Institute of Technology Management from National Tsing Hua University, Hsinchu. He is currently managing the 28 nm Low Power Process Technology Development Program, TSMC.

Kuo-Tsai Li, photograph and biography not available at the time of publication.

Chin C. Hsia, photograph and biography not available at the time of publication.

Huan-Chi Tseng was born in Hsinchu, Taiwan, in 1964. He received the B.S. and M.S. degrees from the Department of Material Science and Engineering, National Tsing Hua University, Hsinchu, in 1986 and 1991, respectively.

He was a Process Integration Engineer with Winbond Electronic Corporation, Hsinchu, in 1992, and joined Taiwan Semiconductor Manufacturing Corporation (TSMC), Hsinchu, in 1993. From 1993 to 1998, he worked in the memory technology area as a Process Integration Engineer for 0.8 μm EPROM, 0.5 μm EPROM, 0.5 μm DRAM, and 0.45 μm DRAM. He was a Section Manager and led the Integration Team which implemented Fujitsu's 0.22 μm DRAM technology in TSMC fab lines in 1998. In 1998, he served as a Section Manager of defectivity and supervised the Defect Technical Board. After 1999, he worked on CMOS logic process integration. He joined TSMC's 300 mm Pilot Line as an Integration Manager in 2000 and helped to establish the first 0.13 μm CMOS technology in the F12 300 mm fab line. Since 2003, he transferred to the Product Engineering Division as an Advance Product Engineering Department Manager. In this role, he collaborated with research and development teams to establish C011, N90, N80, N65, N55, N45, N40, N32, and N28 technologies and his team is responsible for advance technology EFA/PFA yield enhancement, DRM, DFM, and process window characterization. He is currently the Deputy Director of the New Technology Product Engineering Division, TSMC.

Philip A. Fisher received the B.S. degree in physics from the University of Washington, Seattle, in 1991, and the M.A. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, in 1994 and 1999, respectively. For his Ph.D. work, he performed research on the development of a thermoelectric micro-refrigerator based on superconducting tunnel junctions, work which was also reviewed in *The Economist*, March 21, 1998.

From 1999 to 2000, he was a Foundry Process Support Engineer with Analog Devices Corporation, Cambridge. From 2000 to 2008, he was employed in process integration and advanced silicon-on-insulator transistor development with Advanced Micro Devices Corporation, Sunnyvale, CA, during which time he advanced from a Senior Integration Engineer to a Senior Technical Staff Member in recognition of his contributions to the transistor development for the 130, 90, 65, 45, and 32 nm technologies. Since 2008, he has been a Manager with the Department of Advanced Device Technology, Taiwan Semiconductor Manufacturing Corporation, Hsinchu, Taiwan, where his work has focused on development and characterization of high performance and low power transistors. He is the author or co-author of 27 peer-reviewed publications and 27 U.S. patents.

Chuen-Uan Huang was born in 1974. He received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1996, the M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1999, and the Ph.D. degree in electronics engineering from National Tsing Hua University (NTHU), Hsinchu, in 2005.

He was a Post-Doctoral Researcher with the Nano Technology and MEMS Center, NTHU, from 2006 to 2007 for the development of microelectromechanical systems and nano imprinting technology. He joined Taiwan Semiconductor Manufacturing Company, Hsinchu, in August 2007, and is currently a Principle Engineer with the Department of Research and Development, where he works on the development of 28 nm high-K metal gate technology.

Yuan-Yao Chang was born in Pingtung, Taiwan, in 1982. He received the B.S. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 2004, and the M.S. degree in microelectromechanical system engineering from National Tsing-Hua University, Hsinchu, in 2006.

He joined Taiwan Semiconductor Manufacturing Company, Hsinchu, in August 2006, and is currently a Senior Engineer with the Advanced Technology Infrastructure Program, working on the design of test structures for advanced process characterization.

Samuel C. Pan (S'83–M'87) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana, in 1984 and 1986, respectively.

From 1983 to 1986, he was a Research Assistant with the Solid State Electronics Laboratory, University of Illinois. In 1987, he joined Intel Corporation, Santa Clara, CA, as a Senior Device Physicist, working on 0.8 μm Flash EPROM development and 0.6 μm CMOS process development. In 1995, he became a Staff Circuit Designer and worked on the 0.25 μm Pentium/Pro microprocessor focusing on cache memory and programmable logic array design. At the end of 1996, he moved back to Taiwan and joined Macronix International Company, Ltd., Hsinchu, as the QR Deputy Director. In 1999, he was named the Technology Development Director to lead process development for the 0.18–0.15 μm Flash and mask ROM memory technologies. In June 2003, he joined Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, as the Director of Advanced Product Engineering, focusing on yield during next-generation silicon technology development and production ramp. His current research interests include SRAM Vccmin, device physics, device reliability, failure analysis techniques, and methodologies for technology development and yield enhancement.

Dr. Pan is a member of Phi Kappa Phi and Eta Kappa Nu.

Konrad K.-L. Young received the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1986.

From 1986 to 1989, he was with the Lincoln Laboratory, where he worked on silicon-on-insulator device technology and the 193 nm lithography project. He joined Hewlett Packard, Palo Alto, CA, in 1989 to develop the 0.5 μm and 0.35 μm CPU technologies. In 1994, he was with Chartered Semiconductor Manufacturing, Ltd., Singapore, managing Fab1 yield enhancement and product engineering. He joined Winbond Electronics Corporation, Hsinchu, Taiwan, as a Research and Development Memory Technology Director in 1995, and then transferred to Worldwide Semiconductor Manufacturing Corporation as a Fab Engineering Director. He has been with Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, since 1998, in charge of 0.18 μm, 0.13 μm, and 65 nm platform technology development. He also established the TSMC Research and Development Infrastructure Program to improve operation effectiveness and SPICE model quality. He is currently the Director of Advanced Technology Support and Marketing with TSMC.