Effects of EUV Irradiation on Poly-Si SONOS NVM Devices

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***Abstract*—The effects of extreme-ultraviolet (EUV)-irradiation-induced damage on the characteristics of a silicon–oxide–nitride–oxide–silicon (SONOS) memory device are investigated. After EUV irradiation, changes in the memory window and program/erase speed indicate the generation of positive charges and new traps. Retention performance degrades after high-dose irradiation, which indicates that the tunneling layer is damaged. Endurance performance degrades severely because the damage in the blocking oxide results in serious electron back injection after cycling operations. These defects cannot be recovered after 600 °C annealing. It is recommended that in-process high-dose EUV irradiation on a SONOS stack after a front-end-of-line process should be avoided.**

***Index Terms*—Extreme ultraviolet lithography (EUVL), nonvolatile memory (NVM), radiation damage, silicon–oxide–nitride–oxide–silicon (SONOS) memory.**

I. INTRODUCTION

ACCORDING to the International Technology for Semiconductors, extreme ultraviolet lithography (EUVL) and electron-beam (e-beam) writing are the two most promising candidates for next-generation lithography technology with a resolution beyond 22 nm, whereas the other one is imprint lithography [1]. Among them, EUVL has achieved great progress in recent years, and several full-field EUVL technologies have been demonstrated [2], [3].

A wavelength of 13.5 nm of EUV light translates an energy value of 91.85 eV. Although this energy is lower than commonly considered highly energetic photons or particles such as gamma ray, X-ray, alphaparticles, and heavy ions, it is still higher than the bonding energy and energy band gaps of all dielectrics. Radiation damage on a dielectric can be recovered by postirradiation annealing at around 1000 °C [4]. Therefore, if EUV irradiation occurs at an early stage of front-end-of-line processes, EUV radiation damage may not be an issue. However, due to the uncertainty of process technology and integration schemes in future technology nodes, EUV irradiation damage should be considered carefully.

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In Flash-type nonvolatile memory (NVM) integrated circuits (ICs), several geometrical limitations such as tunneling oxide thickness, interpoly dielectric thickness, gate coupling ratios, and control gate filling stop the scaling down of floating-gate memory devices. Silicon–oxide–nitride–oxide–silicon (SONOS) memory devices may scale to beyond a 20-nm node, but the number of electrons becomes too few for multilevel operation. Then, a SONOS memory device with a 3-D stack would be a promising choice. Several major players in memory ICs have devoted efforts on poly-Si SONOS technology, such as Toshiba, Samsung, and Macronix International Company [5]–[9]. A poly-Si SONOS cell with a gate length as small as 18 nm has been demonstrated [9]. It has been shown that grain boundaries in a channel do not seem to affect multilevel cell distribution. No apparent tail distribution is observed, which means that F–N tunneling is not affected by grain boundaries. Although the effect of grain boundaries in thin-film transistor (TFT) NAND devices has not been fully understood and grain boundaries may still affect array performance in some ways, the poly-Si SONOS cell is a promising next-generation NVM cell. In this letter, we report our first work on EUV radiation damage on emerging devices using a poly-Si SONOS device as a test vehicle.

II. EXPERIMENTAL PROCEDURE

The process flow of the poly-Si SONOS memory device started on 6-in p-type wafers. A 150-nm SiO_2 layer was thermally grown as a back isolation insulator, and then, a 50-nm-thick amorphous Si layer was deposited by a low-pressure chemical vapor deposition system to be an active layer. The wafers were annealed at 600 °C in a N_2 ambient for 24 h to have solid-phase crystallization in the active layer. The active layer was further annealed at 900 °C for 30 min to stabilize grain size. Then, a 4/7/20-nm ONO stack was deposited as a tunneling oxide/charge-trapping layer (CTL)/blocking oxide, and a 110-nm-thick undoped amorphous silicon layer was deposited as a gate electrode. The gate electrode was heavily doped by BF_2^+ ion implantation at 40 keV to a dose of 5×10^{15} cm^{-2}. An 80-nm-thick SiO_2 layer was deposited as an antidoping protection layer during a source/drain doping process. Following the gate patterning and spacer formation, source/drain doping was performed by P_{31}^+ ion implantation at 20 keV to a dose of 5×10^{15} cm^{-2}, followed by rapid thermal annealing at 900 °C for 30 s in a N_2 ambient. After removing the gate hard mask, a 40-nm-thick NiSi was formed at the gate and source/drain regions. The final device structure is shown in Fig. 1.

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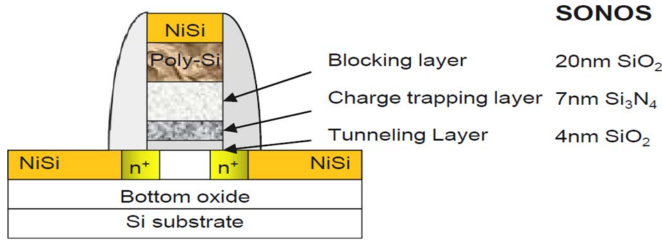

Fig. 1. Schematic structure of the poly-Si SONOS memory device used in this letter.

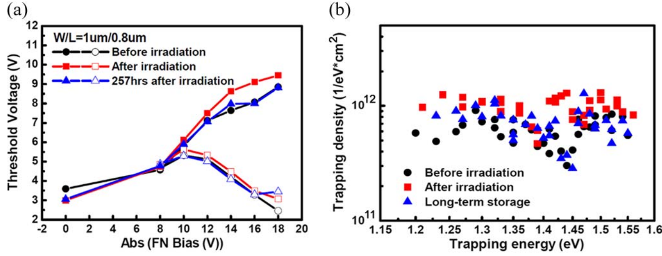

Fig. 2. (a) Threshold voltages of the SONOS memory device after P/E by F–N tunneling at various gate voltages for 0.1 s. (b) Charge trapping density in the Si_3N_4 charge trapping layer.

The EUV light source comes from a beamline constructed at the National Synchrotron Radiation Research Center, Taiwan. The intensity of the EUV beam is 6×10^{12} photons/s. About 16% of EUV light penetrates through the NiSi(40 nm)/p^+ poly-Si(110 nm) gate electrode and irradiates on the dielectric stack, which is equivalent to a dose of 52.9 mJ/cm^2 for 1-min irradiation. This dose is higher than a normal EUV lithography dose ($\sim$10 mJ/cm^2) in order to magnify the effects [1].

III. Results and Discussion

Fig. 2(a) shows the threshold voltages of the SONOS memory device after program/erase (P/E) operation by Fowler–Nordheim (F–N) tunneling at various gate voltages for 0.1 s. A slight decrease in the original threshold voltage $V_{\rm th}$ of the device after EUV irradiation indicates that a small amount of net positive charges is generated. This $V_{\rm th}$ shift does not change after 257-h room temperature storage and may be attributed to some kinds of fixed charges generated by EUV irradiation. Deep-level hole trapping is also possible because electron mobility in SiO_2 and Si_3N_4 is higher than hole mobility by several orders of magnitude [10].

After EUV irradiation, the $V_{\rm th}$ values in both P/E states increase. However, after the 257-h room temperature storage, $V_{\rm th}$ in either the program state or the erase state fully recover to the original situation. Fig. 2(b) shows the extracted trapping density in the CTL [11]. It is observed that EUV irradiation generates new traps, whereas these traps can be self-annealed gradually. It seems that slight erase saturation occurs at high erasing voltage. It is suspected that the blocking layer is damaged by EUV light such that electron back injection occurs. This postulation could be supported by the following results.

Fig. 3 shows the P/E speed of the SONOS memory device. The P/E voltage is +14 and −18 V, respectively. After EUV

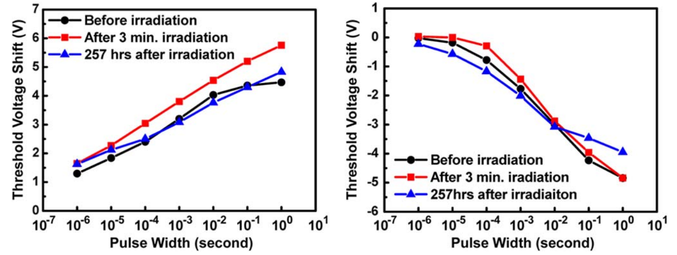

Fig. 3. Threshold voltage shift of the SONOS memory device after (left) programming at +14 V and (right) erasing at −18 V.

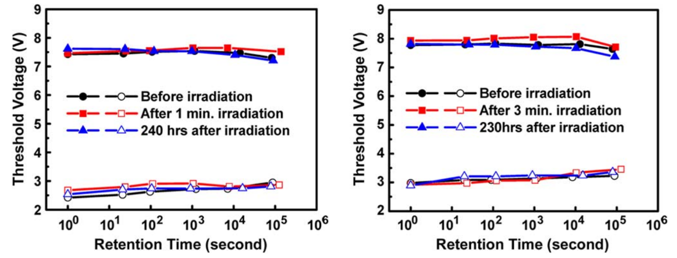

Fig. 4. Charge retention performance of the SONOS memory device. The EUV irradiation time is (left) 1 and (right) 3 min.

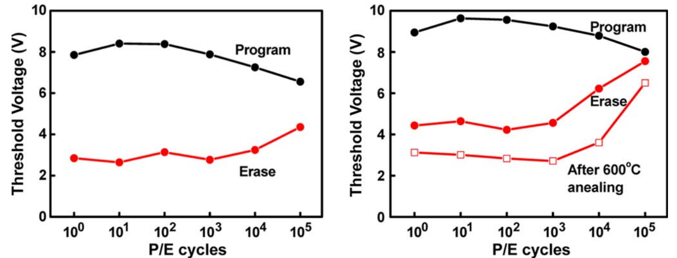

Fig. 5. Endurance characteristics of the SONOS memory device (left) before EUV irradiation and (right) after 3-min EUV irradiation. The data marked by an open square are from the samples with postirradiation annealing at 600 °C for 30 min.

irradiation, the program speed increases, but the erase speed decreases. The phenomena can recover after the 257-h room temperature storage but the suspected erase saturation occurs at longer erase time. These observations are consistent with those observed in Fig. 2.

The charge retention performance of the SONOS memory device is shown in Fig. 4. Neither the program state nor the erase state is affected for 1-min irradiation. As exposure time increases to 3 min, charge retention in the program state degrades. Examining the threshold voltage variation from 10^4 to 10^5 s in the program state, the variation after EUV irradiation (0.36 V) is larger than that before EUV irradiation (0.17 V). Since the main charge loss mechanism of the SONOS memory device is electron tunneling back to the channel through the tunneling layer, the integrity of retention performance indicates that the tunneling layer is not damaged severely during short EUV irradiation. Longer irradiation time would damage the tunneling oxide, so that retention performance degrades on the 3-min EUV irradiation device.

Fig. 5 shows the endurance performance before and after EUV irradiation. Before EUV irradiation, both the P/E states

degrade, and the memory window is reduced by 50% after 10^5 P/E cycles. After 3-min EUV irradiation, the degradation of the program state is similar to that before irradiation, whereas the erase state degrades severely. After 10^4 Hz, only a memory window of 30% is reserved, whereas the memory window almost diminished after 10^5 P/E cycle. The $V_{\rm th}$ shift during the endurance test depends on the degradation mechanism [12]–[15]. $V_{\rm th}$ in both P/E states shift upward as electrons trapped in the deep level cannot be erased completely in each cycle [14]. A memory window closure, i.e., $V_{\rm th}$ in the program state shifts downward, and $V_{\rm th}$ in the erase state shifts upward, can be observed due to tunneling oxide degradation [15]. A leaky blocking oxide can also results in a memory window closure because opposite charges can be injected into the CTL from the top gate. In Fig. 5, the memory window closure occurs on devices before and after EUV irradiation. However, after EUV irradiation, the degradation in the program state does not change, whereas the degradation in the erase state becomes much worse. Therefore, we postulate that the memory window closure before EUV irradiation is dominated by tunneling oxide degradation. After EUV irradiation, the blocking oxide is damaged much severely than the tunneling layer. The continuous high-voltage P/E operations show up the latent defects generated by EUV irradiation in the blocking oxide, and electron tunneling through the 20-nm-thick blocking oxide during the erase state would be enhanced by the trap-assisted tunneling mechanism, so that the device cannot be erased effectively. Because the hole tunneling barrier is higher than the electron tunneling barrier, the program state would be affected by the degradation of the blocking layer less significantly than the erase state. After the endurance test, the retention performance of devices with and without EUV irradiation exhibits similar degradation. This indicates that the main damage during endurance measurement in a tunneling oxide are generated by high P/E voltages. A 600 °C annealing process for 30 min cannot restore the endurance performance, which means that the EUV-irradiation-induced endurance degradation cannot be recovered at the typical poly-Si TFTs and back-end-of-line processes.

IV. Conclusion

In this letter, we have studied the effect of EUV-irradiation-induced damage on poly-Si SONOS memory devices. This is a possible in-line process damage source once EUVL is used in mass production. The memory window and P/E speed are slightly affected by EUV irradiation, and they recover automatically after several days. Retention performance also degrades slightly by high-dose irradiation. The most important damage mode is endurance performance. After irradiation, the memory window shrinks very fast with the increase in P/E cycles, and the mechanism is attributed to the damage in the blocking layer. Since a 600 °C annealing process cannot restore the endurance performance, EUV irradiation at the back-end-of-line process should be carefully avoided. Improving the EUV irradiation immunity of the blocking layer would be helpful. Since only dielectrics would be damaged by EUV light, the results can be applied to SONOS cells on a bulk Si substrate to certain extent.

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