Dynamic Characteristic Optimization of 14 a-Si:H TFTs Gate Driver Circuit Using Evolutionary Methodology for Display Panel Manufacturing

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***Abstract*—For thin-film transistor liquid crystal display (TFT-LCD) panel manufacturing, a gate driver circuit with amorphous silicon TFT plays an important role. In this paper, an amorphous silicon gate (ASG) driver circuit is optimized to improve circuit's dynamic characteristics. The adopted simulation-based evolutionary method integrates genetic algorithm and circuit simulator on the unified optimization framework. The circuit consisting of 14 hydrogenated amorphous silicon TFTs (a-Si:H TFTs) used in a large panel is optimized for the given specifications of the rise time < 1.5 μs, the fall time < 1.5 μs, and the ripple voltage <3 V with minimizing the total layout area. By optimizing the width and passive components of the 14 devices, the results of this study successfully meet the desired specifications, where the sensitivity analysis is further conducted to verify the characteristic variation with respect to the optimized parameters. To validate the results, the optimized circuit is fabricated with 4-μm a-Si:H TFT process, and the experimental result confirms the practicability of achieved design. The ripple voltage within 2.0 V is successfully obtained while the rise and fall times satisfy the required specifications for the fabricated sample. A 35% reduction of the optimized total devices width of a-Si:H TFTs is achieved.**

***Index Terms*—Amorphous silicon gate driver circuits (GDCs), dynamic characteristic, fabrication, fall time, genetic algorithm, liquid crystal display (LCD), measurement, panel manufacturing, ripple voltage, rise time, simulation-based optimization, thin-film transistor (TFT).**

I. Introduction

THIN-FILM transistor liquid crystal displays (TFT-LCDs) for the application of smart phones is being developed rapidly in points of resolution, pixels per inch (PPI), number of colors, and brightness. Thus, integrating a driver circuit on the TFT backplane is one of the fascinating challenges in a quarter video graphics array (QVGA) resolution LCD panel because of its many advantages, such as overall cost reduction, compactness, and mechanical reliability [1]–[5]. Diverse approaches, such as low temperature polycrystalline silicon (LTPS), hydrogenated amorphous silicon (a-Si:H) [6], [7], and zinc-oxide (ZnO) [8], [9] are proposed as an active channel material in n-channel TFTs, as well as gate driver circuits sequentially. However, additional processes which resulted in increasing cost are necessary in LTPS technology. Furthermore, there are several reliable problems of amorphous silicon gate (ASG) driver circuit that should be considered in ZnO film [10]. Therefore, nowadays, because of the cost merits due to simple process and high yield, a-Si:H process has been main stream in gate driver circuit of TFT-LCD for mobile application [11]–[13]. In general, the topology of ASG driver circuit is requested to achieve superior and stable output waveform. Therefore, dynamic characteristics are usually obtained empirically to meet the required specifications [14]–[16] for given ASG circuits. A trial-and-error method is generally adopted by circuit designers to tune circuit parameters including device geometry, biasing, etc. This design flow generally is a time-consuming task to meet all desired specifications in display circuit manufacturing. In addition, the methodology of simulation-based evolutionary approach has recently been proposed for optimizing device's doping profile [17]–[19] and equivalent circuit model parameter extraction [20] in our previous works. Optimization results of these studies have confirmed the robustness and efficiency of the proposed method. Systematical optimization approach, based upon simulation-based evolutionary methodology, will be an interesting study for optimal design of TFT-LCD panel circuits, and thus benefit their manufacturing.

In this work, we demonstrate an optimized gate driver circuit on glass substrate to improve dynamic characteristics. Then simulation-based evolutionary algorithm on the unified optimization framework [21] is successfully advanced on performing optimal design of the circuit on a-Si:H TFT-LCD panel. The circuit to be optimized consists of three pull-up control devices, three pull-down control devices, three pull-up output devices and five pull-down output devices, where all devices' widths are parameters to be designed for the specifications of the rise time < 1.5 μs, the fall time < 1.5 μs and the ripple voltage <3 V while we simultaneously consider the minimization of total layout area. As for the optimized solutions achieved by the method, the sensitivity analysis is simultaneously considered to verify how the variation in dynamic characteristics of optimized circuit. We analyze a set of solutions for optimized ASG driver circuit by varying ± 0.5 μm of each width and ± 0.2 μm of each length statistically. The

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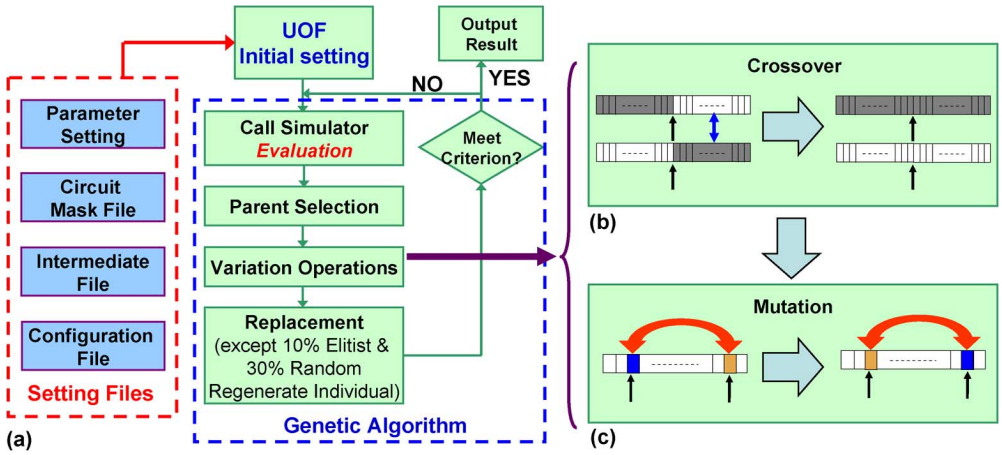


Fig. 1. (a) Illustration of the method for optimizing the ASG driver circuit. The replacement mechanism is age-based but with 10% elitist and 30% regenerate random individuals. The mechanism of the variation operators: (b) crossover and (c) mutation.

final optimized ASG driver circuit is further fabricated with 4-μm process a-Si:H TFT technology. The comparison of dynamic characteristics of measurement and simulation are disscussed in detail.

This paper is organized as follows. In Section II, the genetic algorithm and the implemented simulation-based optimization method are introduced. In Section III, the explored ASG driver circuit is optimized and discussed. In Section IV, the fabricated and measured results are shown to validate our theoretical results. Finally, we draw conclusions and suggest future work.

II. Optimization Technique and Simulation Results

The unified optimization framework (UOF) [21] enables us to implement the optimization method to design ASG driver circuit with the most suitable parameters. The UOF can evolve the parameter configuration of circuit by genetic algorithm (GA) [22]–[24] and achieve particular performance of the circuit with the parameter configuration as the basis to obtain fitness value by executing external circuit simulator [25]–[28]. The flow is shown in Fig. 1(a); for a script file of netlist depending on ASG driver circuit topology, we define the parameters of ASG driver circuit to be optimized in a circuit mask file. Then, the initial population, i.e., the group of parameter configurations, is generated by engineering design or random selection. Implementation of the evaluation mechanism is by putting the parameters into mask file to obtain the complete circuit netlist file (intermediate file), and then sending the file into circuit simulator to acquire the circuit characteristics automatically. As soon as evaluation is completed for all individuals (an individual indicates a specific configuration), the parents (relatively better individuals) are selected by the fitness proportional method and are ready to generate offspring—new individuals. Two variation operators are applied on the parents to attain this goal. The first is one-point crossover [29], [30]. The split point in one-point crossover is randomly determined, then the genes of offspring (here we treat the parameter configuration—individual—as a parameter array, and an element in the array is called gene, which means certain parameter) from beginning to split point will be inherited by one parent, and the rest will be inherited by the other parent, as disclosed in Fig. 1(b). After the crossover operator, the mutation operator enables to randomly choose two genes in one

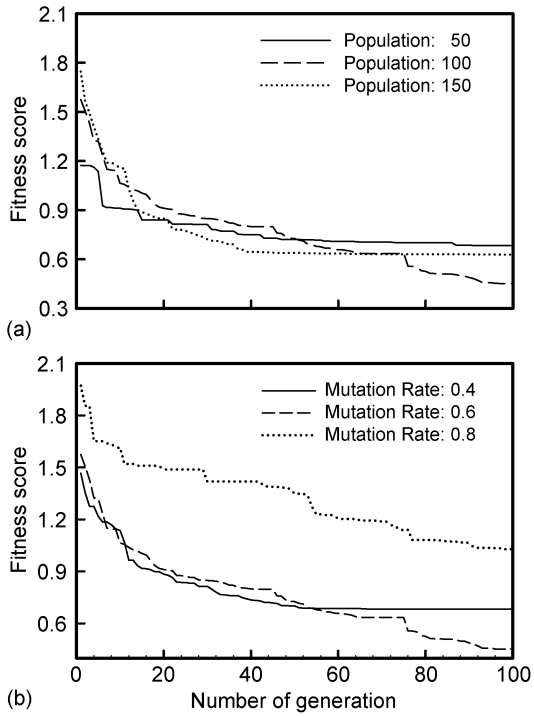


Fig. 2. Comparison of the score convergence behavior of the algorithm in ASG driver circuit among (a) population sizes, where the crossover and mutation rate are fixed at 0.6 and (b) and mutation rate, where the crossover is fixed at 0.6 and population size is fixed at 100, respectively.

individual and exchange them with mutation rate, as shown in Fig. 1(c). Notably, the mutation rate which influences diversity of GA must be carefully determined. Finally, except the best 10% individuals in last generation, which are called elitists, and 30% regenerate individuals, the other part of the population is substituted by the offspring after variation operators. If the characteristics meet the requirement prescribed by the circuit designer, we output the final optimized solution. If the error between the specifications and characteristics does not meet the convergence criterion, the UOF performs GA to execute next iteration (generation) from evaluation step. The process will be continued until the specifications are matched. The parameters

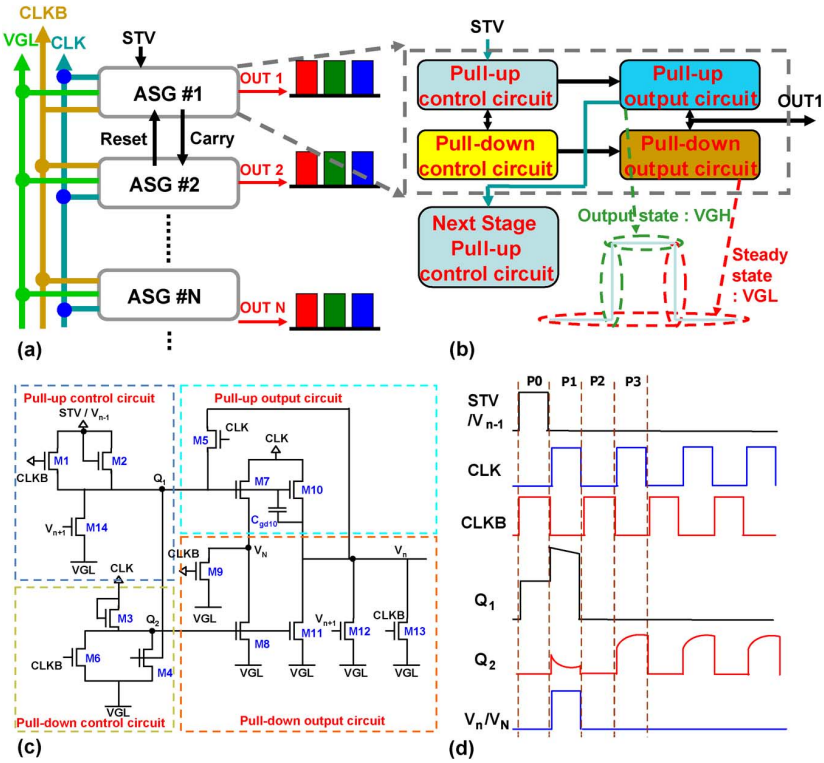


Fig. 3. (a) A schematic of active matrix LCD panel controlled by ASG driver circuit. (b) Components of one stage ASG driver circuit and the output waveform affected by corresponding component of ASG driver circuit. (c) Ffirst ASG driver circuit consists of 14 a-Si:H TFTs which used in large loading products such as monitor and screen of TV. (d) Timing diagram of 14-TFTs-ASG driver circuit.

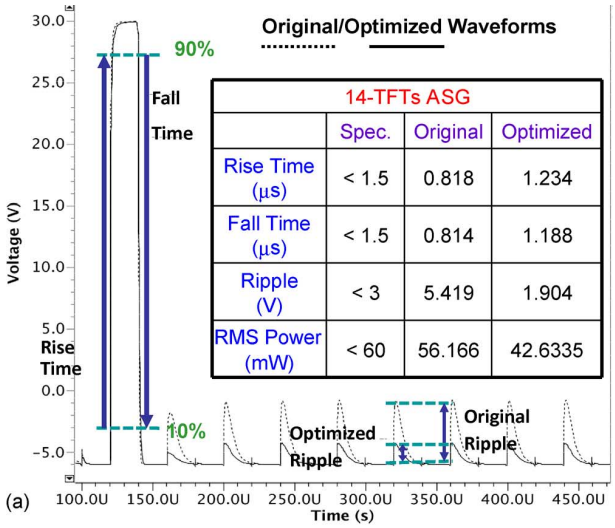
TABLE I
PARAMETERS SETTING OF GENETIC ALGORITHM IN OUR CIRCUIT DESIGN OPTIMIZATION

Parameters Setting of Genetic Algorithm	
Population Size	100
Max Generation	100
Crossover Rate	0.6
Mutation Rate	0.6

setting of GA in circuit design optimization is summarized in Table I, and be set in configuration file.

By considering the experiment, Fig. 2(a) shows a comparison of the fitness score convergence behavior among population sizes, where the crossover and mutation rate is fixed at 0.6. The fitness score versus the number of generation suggests that the score convergence behavior does not have a satisfied result if the population size is too small. However, large population size obviously cause high consumption of time and is not sure to achieve better results. According to our experience, the $\mathrm{populationsize} = 100$ is good for the optimal design of ASG driver circuit. In addition, Fig. 2(b) shows the fitness score convergence behavior for the circuit optimization with different mutation rate, where the population size and crossover rate are fixed at 100 and 0.6. An excessively high mutation rate makes the global search in GA similar to random search, whereas the lack of mutation chances may cause local convergence and lose the diversity. The results suggest that the $\mathrm{mutation} = 0.6$ keeps the population diversity and finally has better evolutionary results.

The original and optimization simulation results of proposed ASG driver circuit are discussed. At the first, we briefly introduce the operation of explored ASG driver circuit. Then the numerical experiments for the proposed explored ASG driver circuit are realized and discussed. Finally, the sensitivity analysis verifies the characteristic variations of optimized circuits. A schematic of active matrix LCD panel controlled by ASG driver circuit in product [31] is shown in Fig. 3(a); each stage of ASG driver circuit consists of pull-up and pull-down control circuits, pull-up and pull-down output circuits, as shown in Fig. 3(b). The output state, VGH, and rise time of output waveform are influenced by designed pull-up output circuit. The steady state, VGL, and fall time of output waveform are affected by designed pull-down output circuit, respectively. Fig. 3(c) and 3(d) shows one stage circuit of the proposed ASG driver circuit used in products and its timing diagram. The ASG driver circuit with 14 a-Si:H TFTs used in large loading products such as monitor and screen of TV. Then in circuit's topology, the CLK and CLKB denote the clock signal and clock bar signal; VGL is the steady-state voltage, and $\mathrm{STV/V}_{n-1}$ is inputted pulse signal. The V_n and V_N are the output signal which supply for the panel and next stage, respectively. Fig. 3(d) shows timing diagram of ASG driver circuit with 14 devices and the operation of 14-TFTs–ASG driver circuit is as follows. When the input signal is high, the Q_1 node is charged by the input signal $(\mathrm{STV/V}_{n-1})$; then, as CLK is changed from low to high, the Q_1 node voltage is boosted up due to the gate–drain capacitive coupling of M10. Therefore, the output driving ability (V_n and V_N) is achieved through M7 and M10. At this time, the high voltage of the Q_1



14-TFTs ASG	Spec.	Original	Optimized
Rise Time (μs)	< 1.5	0.818	1.234
Fall Time (μs)	< 1.5	0.814	1.188
Ripple (V)	< 3	5.419	1.904
RMS Power (mW)	< 60	56.166	42.6335

Original device width (um)			
M1	10	M8	8000
M2	500	M9	800
M3	80	M10	1000
M4	500	M11	1000
M5	500	M12	160
M6	80	M13	160
M7	160	M14	160

Total Devices' Width = 13110

35% Reduction

Optimized device width (um)			
M1	10	M8	4730
M2	110	M9	600
M3	80	M10	610
M4	430	M11	860
M5	330	M12	140
M6	50	M13	330
M7	130	M14	160

Total Devices' Width = 8570

(b)

Fig. 4. (a) Original and optimized simulation results of 14-TFTs ASG driver circuit. The inset table indicates demanded specifications. (b) Comparison of TFT widths between the original and optimized designs.

node is applied to the gates of M4 simultaneously. Therefore, M11 is turned off, and the high voltage is kept at the Q_1 node. After generating an output voltage, the Q_1 node voltage is discharged when the output signal of next stage (V_n) is applied to the gate of M12. After that, the Q_1 node is alternately discharged through M13 by using the CLKB signal.

The designed parameters of 14-TFTs ASG driver circuit are the widths of a-Si:H TFT devices, as shown in Fig. 4. The specifications, original, and optimized results of the output signal which contains the fall time, the rise time, and the ripple voltage in the ASG driver circuit are shown in the inset table of Fig. 4(a), respectively. The rise time is defined by the interval of time required for leading edge of a pulse raised from 10% to 90% in the peak pulse amplitude and the definition of fall time is contrary to rise time. The ripple voltage is defined by maximum peak-to-peak voltage after the pulse. These three electrical characteristics are the required specifications in the ASG driver circuit design generally. The inset table of Fig. 4(a) indicates the specifications, original and optimized results. The original result shows that the fall and rise times are within the given specifications; however, the ripple voltage compared with our setting criteria is extremely high. Therefore, the aforementioned evolutionary approach is activated to find the feasible configuration of device widths based on the netlist file of the initial circuit. Finally, the ripple voltage after optimization decreases significantly from 5.419 to 1.904 V while we keep the rise time and fall time satisfied the required specifications. Fig. 4(b) shows the original design by empirical experience and our optimization. There is 35% reduction of the optimized total devices width of a-Si:H TFTs compared with the initial one in this explored ASG driver circuit. For the given targets and specifications, it shows that this methodology provides an automatic mechanic to design the parameters of the explored ASG driver circuit.

Sensitivity analysis is a technique which considers how small changes in decision variables affecting the function outputs. For designed parameters which fulfill aforementioned specifications, we analyze a selected and modified solution for ASG driver circuit by ± 0.5 μm of each width and ± 0.2 μm of each length with optimized widths sequentially. In the mathematical statement, if $f_0(x^*)$ represents the function value in the analysis point, then we can observe the variation of the function with small perturbation of x^*, then the sensitivity of f_0 in x^* respect to x_i can be expressed as [32]

$$Z_i = \left| \frac{\partial f_0^* / f_0^*}{\partial x_i / x_i} \right| \times 100\% \tag{1}$$

where x_i is each decision variable. Fig. 5 shows the sensitivity of 14-TFTs ASG driver circuit which may result from process variation effects in the circuit, respectively. In Fig. 5(a), the sensitivity of 14 parameters is almost lower than 10%. However, the electrical characteristics are rather susceptible to the parameter W8 which controlled the charge ability of the TFT array devices of display panel. Therefore, the parameter W8 induces larger sensitivity. We further examine the sensitivity of length variation with optimized widths, as explored in Fig. 5(b). The same phenomena are observed in ASG driver circuit. The sensitivity of electrical characteristics is also dominated by W8 of 14-TFT ASG driver circuit. Moreover, due to parameter L11 is component of pull-down output circuit, the sensitivity of fall time is quite large. Finally, the result can guarantee the robustness of our optimized design and confirm promising characteristics of these ASG driver circuits which have benefits to manufacturing of TFT-LCD panel.

III. Sample Fabrication and Measurement Results

Standard process flow of TFTs is considered for the sample fabrication of optimized ASG driver circuits. The measurement results of rise time, fall time, and ripple voltage of samples are discussed in detail. The inverted-staggered back-channel etched (BCE) type of a-Si:H TFTs fabricated on glass substrate is used for gate driver circuit. First, the gate electrode of 300-nm-thick Mo/AlNd (GE) alloy is deposited by physical vapor deposition method on the glass substrate and patterned. Thereafter, 380-nm-thick silicon-nitride (SiN_x), 150-nm-thick undoped a-Si:H layer, 50-nm-thick n+ a-Si:H are deposited by chemical vapor deposition method and the a-Si:H layers are patterned. The silicon-nitride layer is served as the gate insulator and deposition temperature is about 300 °C–350 °C. The undoped a-Si:H layer is served as the active layer and deposition temperature is about 220 °C–350 °C. The n+ a-Si:H layer is used to form the ohmic contacts at source/drain (S/D) electrodes, which are deposited by physical vapor deposition method and then patterned. The n+ a-Si:H layer in TFT channel

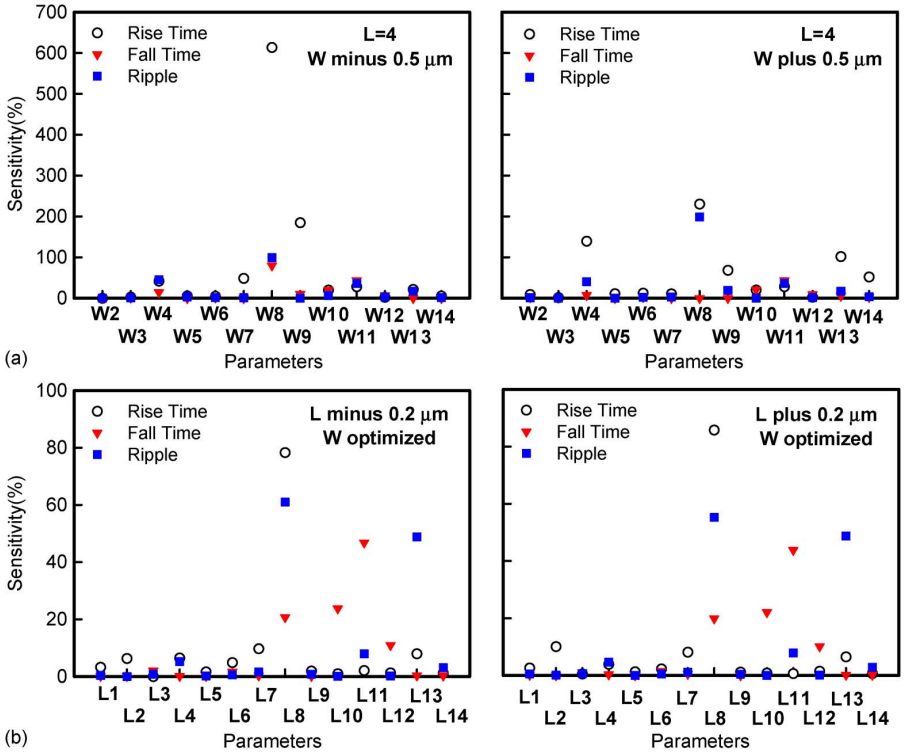


Fig. 5. Sensitivity analysis of the14-TFTs ASG driver circuits. (a) ± 0.5 μm of each width with $L = 4$ μm. (b) ± 0.2 μm of each length with optimized widths sequentially.

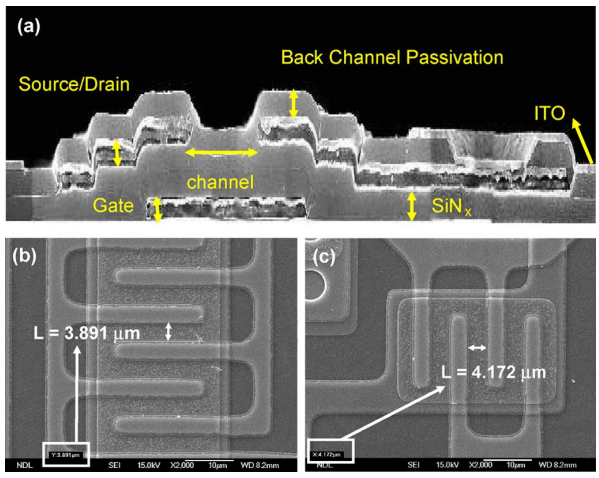


Fig. 6. (a) Cross section view of SEM picture of fabricated TFT sample and the process variation of: (b) L5 and (c) L11 of 14-TFTs ASG driver circuit.

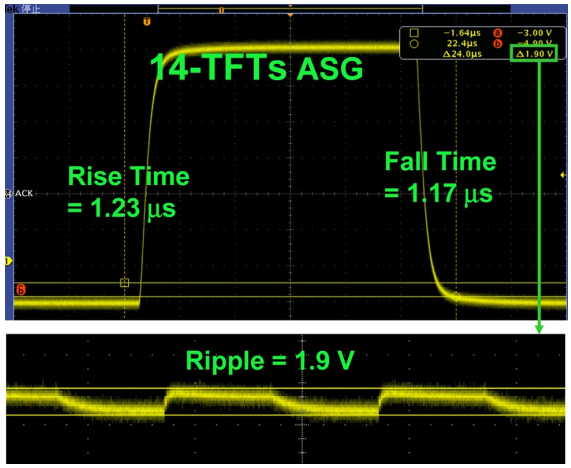
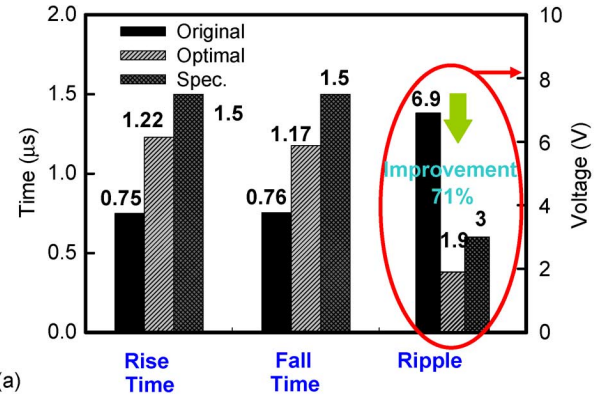


Fig. 7. Experimental results of rise time, fall time, and ripple voltage for 14-TFTs ASG driver circuit measured by using a Tektronix DP04054 oscilloscope.

region is etched off by dry etching method and then overetched until the undoped a-Si:H layer. The back channel passivation layer (Si_3N_4) of 200-nm-thick is deposited by chemical vapor deposition method and patterned. Finally, the contact hole is deposited with 50-nm ITO layer by physical vapor deposition method, as a pixel electrode (connected with source or drain). A cross-section view of scanning electron microscope (SEM) picture of fabricated TFT sample is shown in Fig. 6(a). In addition, the process variation of lengths of ASG driver circuits which makes agreement to assumptions of sensitivity analysis is shown in Fig. 6(b) and (c). Test chips of the optimized 14-TFTs ASG driver circuit are fabricated in the standard 4-μm a-Si:H TFT technology.

We examine the tested layout which consists of six stages gate driver circuit and occupies the area of 1.386 mm^2. A Chroma 58162-E signal generator and a Tektronix DP04054 oscilloscope were used to carry out the aforementioned input signal. As for the measurements more precisely, the input signal, STV (SP), CLK, CLKb, and VSS are set as same as the simulation. Then the measured dynamic characteristics of the chip are illustrated in Fig. 7 where the rise time, fall time, and ripple voltage is 1.23 μs, 1.17 μs, and 1.9 V, respectively.



(a)

(b)

14-TFTs ASG Driver Circuit			
	Fabrication	Simulation	Error (%)
Rise Time (μs)	1.229	1.234	0.41
Fall Time (μs)	1.177	1.188	0.93
Ripple Voltage (V)	1.9	1.904	0.21

Fig. 8. (a) Comprehensive comparison among the fabrication data of the original/optimized setting and the specifications. (b) Comparison of simulation and fabrication results of 14-TFTs ASG driver circuit.

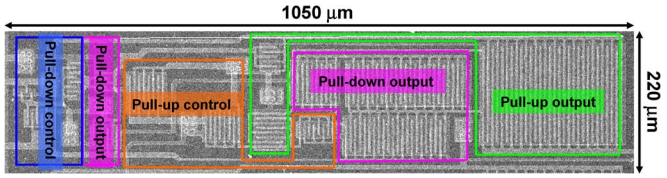


Fig. 9. Optical image of the fabricated 14-TFTs ASG driver circuit occupied area of 0.231 mm^2.

Comprehensive comparison among the fabrication data of the ASG driver circuit with original/optimized design and the specifications are disclosed in Fig. 8(a). The improvement of ripple voltage is 71% for the 14-TFTs ASG driver circuit while we also successfully maintain the rise time and the fall time within the required specifications. In additional, the experimental characterization results are close to the simulation results or even better than the theoretically estimated data, as listed in Fig. 8(b). Fig. 9 shows the optical image of our optimized one stage ASG driver circuit with 14-TFTs by using SEM and occupied the area of 0.231 mm^2 $(1050\ \mu m \times 220\ \mu m)$.

IV. Conclusion

In this study, we have demonstrated an optimized ASG driver circuit for manufacturing using the simulation-based evolutionary approach. The approach combines GA with circuit simulator on the unified optimization framework to execute the optimization flow automatically. It successfully extracts the designed parameters in ASG driver circuit. The ripple voltage of 14-TFTs ASG driver circuit is significantly decreased from 5.419 to 1.904 V while we simultaneously maintain its dynamic characteristics within the required specifications. Sensitivity analysis has further shown promising and stable electrical characteristics of optimized parameters. The optimized ASG driver circuit was fabricated using standard process of 4-μm a-Si TFTs technology. The experimental results of 14-TFTs ASG driver circuit are close to simulation results and the improvement of ripple voltage is 71% as compared with original design. Consequently, this approach is highly extensible to design different functional block of display panel circuits. In additional, the reliabilities, such as temperature and bias-stress, and power consumption in ASG driver circuit are currently examined. Notably, layout technique could be improved empirically for approaching to the theoretical estimation of 35% reduction of total layout.

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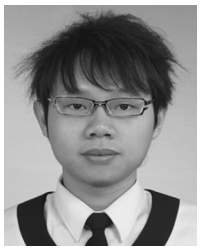

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