Low-Temperature Characteristics of Well-Type Guard Rings in Epitaxial CMOS

Chih-Yao Huang, *Member, IEEE,* Ming-Jer Chen, *Member, IEEE,* Jeng-Kuo Jeng, and Ching-Yuan Wu, *Member, IEEE*

***Abstract*—Characterization and simulation of minority-carrier well-type guard rings in epitaxial substrate at 77 K were performed and compared with those at RT. The escape probability in a narrow guard-ring structure under the same amount of minority carrier injection increases by about one order of magnitude when temperature decreases to 77 K. This degradation in the guard-ring efficiency can be attributed to the enhanced drift mechanism in the conductivity-modulated layer between the well bottom junction and the epitaxial high/low junction at 77 K. In contrast, this mechanism enhances the width dependence of the escape probability at 77 K. The higher minority-carrier recombination velocity of the epitaxial high-low junction contributes to the stronger width dependence secondarily. When the epitaxial layer thickness becomes thinner, the simulation also demonstrates a stronger width dependence of the escape current as well as a reduction in its magnitude. A lightly-doped epitaxial layer on a heavily-doped substrate exhibits even more importance in the guard ring efficiency for low temperature operation, and its thickness should be kept as thin as possible.**

I. Introduction

LOW-TEMPERATURE CMOS has been extensively studied as a result of more excellent performance and reliability than RT operation at device, circuit, and system levels [1]–[4]. Its advantages include higher carrier mobility, higher switching speed, sharper subthreshold slope, decreased noise and junction leakage current, reduced parasitic resistance and interconnection resistance, and better latch up immunity.

On the other hand, minority-carrier well-type guard rings at RT have been studied recently [7]–[12]. Minority-carrier well-type guard rings, which are regarded as one of the most effective methods for latch up elimination, have been widely used for collecting minority carrier injection from parasitic emitter structures around I/O area in CMOS technology. The efficiency of such guard ring can be greatly improved by using epitaxial layer substrate [8]. The mechanism responsible for this enhancement has been reported to be Auger recombination in the heavily-doped substrate [9]. An analytic design formulation has been proposed to quantitatively describe guard ring efficiency and applied to the establishment of design guideline for minimum area consumption [10]–[12]. In view of the excellent features of low-temperature CMOS, the low-temperature operation of the guard ring is clearly worth more investigation. In this work we present both measured characteristics and numerical simulations of guard rings with different guard-ring width at 77 K as compared with those at RT. The physical mechanisms contributing to the behavior of the guard ring are discussed in detail by means of two-dimensional numerical analysis. Finally design considerations for improved low-temperature performance will be addressed based on the experiments and simulations.

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C.-Y. Huang is with Mosel Vitelic Inc., Hsinchu 300, Taiwan, R.O.C.

M. J. Chen and C.-Y. Wu are with the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

J.-K. Jeng is with Vanguard International Corporate, Hsinchu 300, Taiwan, R.O.C.

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II. Experimental Results

The schematic top view and cross section along the line AA' of the test structure investigated is shown in Fig. 1. The inner/outer n-well collectors surround an emitter region on an epitaxial heavily-doped substrate fabricated by 1.0 μm n-well polysilicon CMOS technology. The inner square collector is a guard ring and the outer collector acts as internal circuitry. The emitter region represents drain/source diffusion in a MOS device. The four different guard ring widths W_g are 6, 20, 40, 60 μm and the epitaxial-layer thickness is about 10.0 μm. The emitter junction depth and n-well junction depth are 0.3 and 3.0 μm, respectively. The peak doping concentrations in the n^+ emitter, n-well, p-type epitaxial layer, and p^+ substrate are 2×10^{19}, 6×10^{16}, 2×10^{15}, and 4×10^{18} cm^{-3}, respectively. The devices were mounted on 18-pin ceramic dual-in-line packages. The package was put into a RMC–Cryosystems LTS-22 closed-cycle cold head for low-temperature measurement. Good thermal contact has been made for effective cooling. Besides being measured by a silicon diode temperature sensor, the device temperature was also extracted and checked by PN-junction diffusion equation $I_o \exp(qV/nKT)$. The I–V characteristics were measured with both wells biased at 5.0 V, the emitter grounded, and the base-emitter bias V_{be} swept from 0.0 to 2.0 V for both the RT and 77 K cases.

Fig. 2(a) shows the Gummel plot of the emitter current I_e, collection current I_{c1}, base current I_b, and escape current I_{c2} for a 6 μm wide guard ring at both RT and 77 K. The turn-on voltage in Fig. 2(a) obviously increases by about 0.4 V at 77 K compared with the RT case. This is due to the weak increase of the PN junction built-in potential at low temperature [15]. Low-temperature operation of a guard ring seems to improve its performance in ideal diffusion region. However, 0.4 V increase will not always be sufficient for latch up elimination. This is only a rather limited improvement

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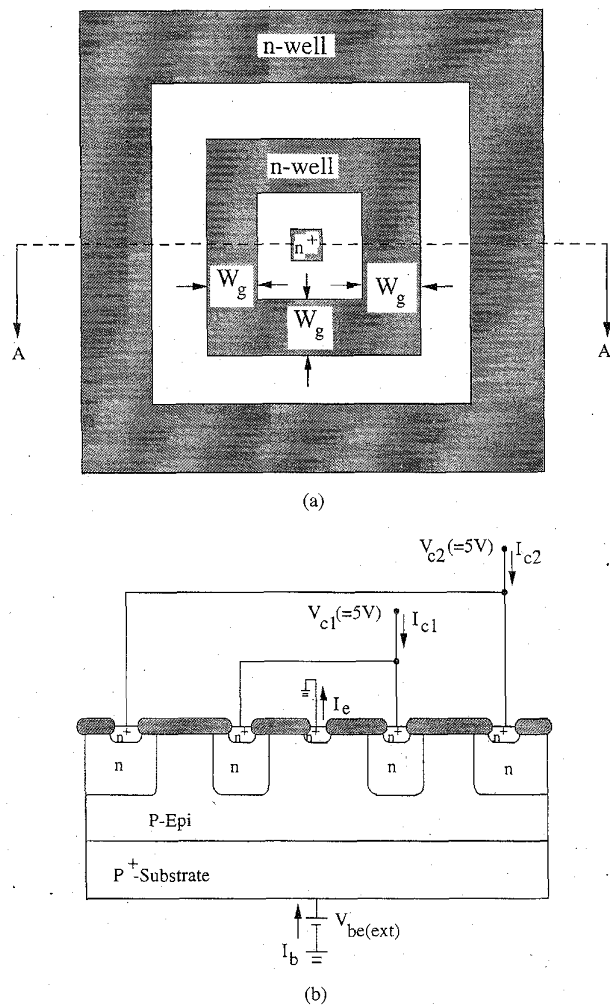

Fig. 1. Schematic top view and cross section along the line AA' of n-well guard ring structure on p-epi/p$^+$-substrate where n$^+$ emitter, inner, and outer n-well collectors are also shown.

as a consequence of high-level injection during latch up state. In various circumstances the place most sensitive to latch up in an IC is the I/O region. Large current flow and large parasitics may be present in such regions. Abnormal circuit voltages, which are immense especially in electrostatic discharge (ESD) event, may be encountered [6]. Devices suffering from outer noise in these regions may be triggered into on state and inject minority carriers into either the substrate or the well, potentially triggering other pnpn paths nearby. Thus the quantity of minority carriers injected instead of the applied outer voltage represents a key factor in effective evaluation of latch up susceptibility around the I/O areas [7]. Hence the intuitively applied bias point of view should be improved, and more insights can be obtained by means of the comparison under the same amount of the injected minority-carrier density from the parasitic emitter, namely the equal I_e. In Fig. 2(a), some typical V_{be} biases at RT for comparison may arbitrarily be selected: for instance, 0.7, 1.0, and 1.2 V. The corresponding emitter currents are directly obtained from the RT Gummel plot. Then three bias values are obtained with the same emitter current values in the 77 K Gummel plot: 1.1, 1.4, and 1.8 V, respectively. That is, the emitter currents of 1.1, 1.4, and 1.8 V at 77 K are identical to those of 0.7, 1.0, and 1.2 V at RT, respectively. Both 0.7 V at RT and 1.1 V at 77 K represent the onset of the high-level injection of the Gummel plot in this structure.

Based on the above method, the escape probability was calculated from Fig. 2(a) by the ratio of the escape current divided by the emitter current, I_{c2}/I_e, which is the transport factor from the emitter to the outer n-well when the guard ring is also collecting carriers [8]. This quantity expresses the amount of injected minority carriers that escape from the guard ring collection and into the substrate. In addition, I_{c1}/I_e, which is the transport factor from the emitter to the guard ring n-well, was also calculated and compared. Either $(1 - I_{c2}/I_e)$ or I_{c1}/I_e can be understandable as a measure of guard-ring efficiency. However, the best indication is the escape probability itself since a very small change in the $(1 - I_{c2}/I_e)$ or I_{c1}/I_e may produce a change of several orders of magnitude in the I_{c2}/I_e. As the I_{c2}/I_e becomes larger the guard-ring efficiency reduces more. On the contrary, as the I_{c2}/I_e becomes smaller the guard-ring efficiency improves more. The escape probability for a 6 μm wide guard ring at 77 K was found to be about ten times higher than that at RT, as illustrated in Fig. 2(b), yet I_{c1}/I_e remains almost the same for both cases. This result demonstrates the reduced efficiency of the narrow guard ring at 77 K. Fig. 2(c) shows the plot of the escape probability as a function of W_g at both RT and 77 K. In Fig. 2(c) the applied V_{be} biases for the characteristics at RT and 77 K are separately 0.9 V and 1.3 V for the first pair of comparison, and 1.2 V and 1.9 V for the second pair. The measured results at these different biases corresponding to the same amount of the injected emitter currents at the two specified temperatures. The width dependence of both the I_{c2} and I_{c2}/I_e becomes stronger as the temperature is lowered. In addition, the amount of the I_{c2} at 77 K with W_g around 6 μm becomes at least one order of magnitude larger than that at RT. The curves at 77 K show a rise in the I_{c2} and I_{c2}/I_e with narrow W_g and a reduction with large W_g as compared with those at RT. The cross points of the RT and 77 K lines are located at W_g ranging from 20 to 35 μm, depending on the amount of the applied biases. To sum up, these results indicate that the narrow guard ring has reduced collection efficiency whereas the wide guard ring has improved efficiency for low temperature operation. Moreover, the width dependence becomes gradual as the V_{be} increases.

III. Reduced Collection Efficiency in Narrow Guard Rings

Because of the wide spreading of minority carriers over the whole substrate and the complicated nature in many physical models at low temperature, it is necessary to employ 2-D numerical simulation for detailed analysis. Two-dimensional numerical simulation utilizing a device simulator MEDICI [16] was performed for both the RT and 77 K cases. Because the test structure and its current flow pattern are symmetrical, only the right half of the device in Fig. 1 was

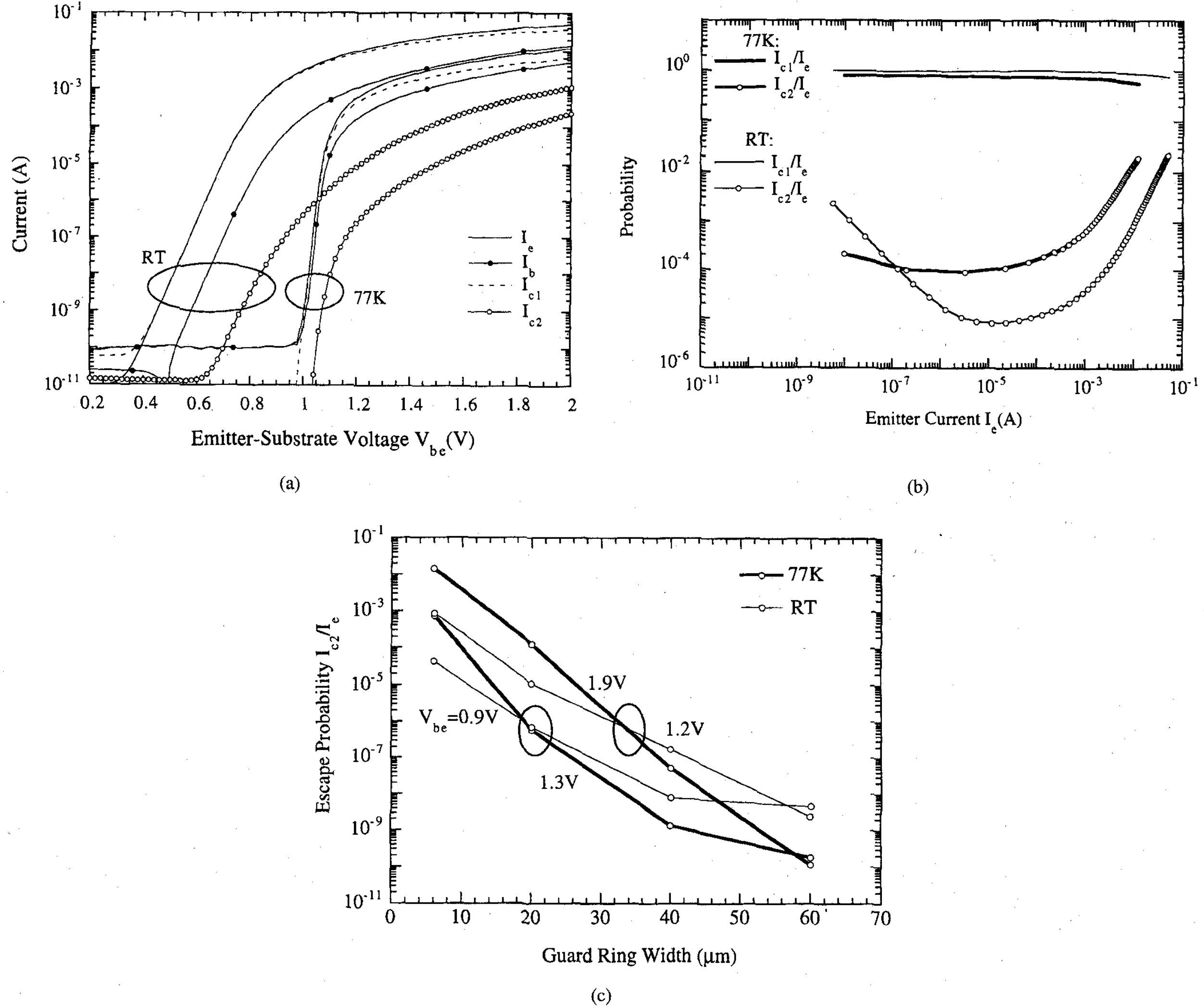

Fig. 2. (a) Measured characteristics of the emitter current I_e, collection current I_{c1}, base current I_b, and escape current I_{c2} for a 6 μm wide guard ring at RT and 77 K with both wells biased at 5 V, emitter grounded, and emitter-substrate bias swept from 0.0 to 2.0 V. (b) Comparison of calculated ratio of collection current divided by emitter current I_{c1}/I_e and escape probability (defined by the ratio of the escape current divided by the emitter current I_{c2}/I_e) versus emitter current I_e at RT and 77 K. (c) The measured escape probabilities I_{c2}/I_e as a function of W_g at RT and 77 K. The V_{be} biases of the first comparison pair are 0.9 and 1.3 V, and the second pair are 1.2 and 1.9 V at RT and 77 K, respectively.

simulated. The simulator in this work, however, is only used for qualitative analysis of low-temperature applications. This is due to simplicity of the low-temperature models and their coefficients, and the nonuniform current distribution along the perimeter of the square layout in the test pattern. For the low-temperature simulation the default models built in the simulator could not completely satisfy the requirements [17], [18]. Among the models utilized in this work, carrier freezeout with Fermi–Dirac statistics is the basic phenomenon at low temperature [14]. Because of the difficulty in introducing the temperature-dependent freezeout ionization energies in the incomplete ionization [18] into the simulator, the two energy values were estimated from the experimental data in [14]. For temperature-dependent energy gap, the default model in the simulator was still adopted in this work. Although the built-in model was used, it was reported that the effect of different model is not significant in qualitative analysis [18]. For SRH recombination, a fully justified model is still unavailable [17], [18]. Hence, the model equation and parameter values at RT were still used here for the 77 K study [19]. Other models include Fermi–Dirac statistics, density of states for conduction and valence band [17], temperature-dependent bandgap narrowing effect [21], Auger recombination [22], carrier mobility with concentration, temperature and field dependence [23] and [24] as well as temperature-dependent carrier saturation velocity [14]. The coefficients in some of these models were modified to meet the requirements at low temperature. Moreover, the nonuniform current distribution along the square test-pattern perimeter is actually beyond the capability of a 2-D simulator. The high applied bias and low temperature further lead to a more complex situation in the current distribution. Under such circumstances, the simulator is only feasible for investigating qualitative behaviors and giving more physical insights for experiment phenomena.

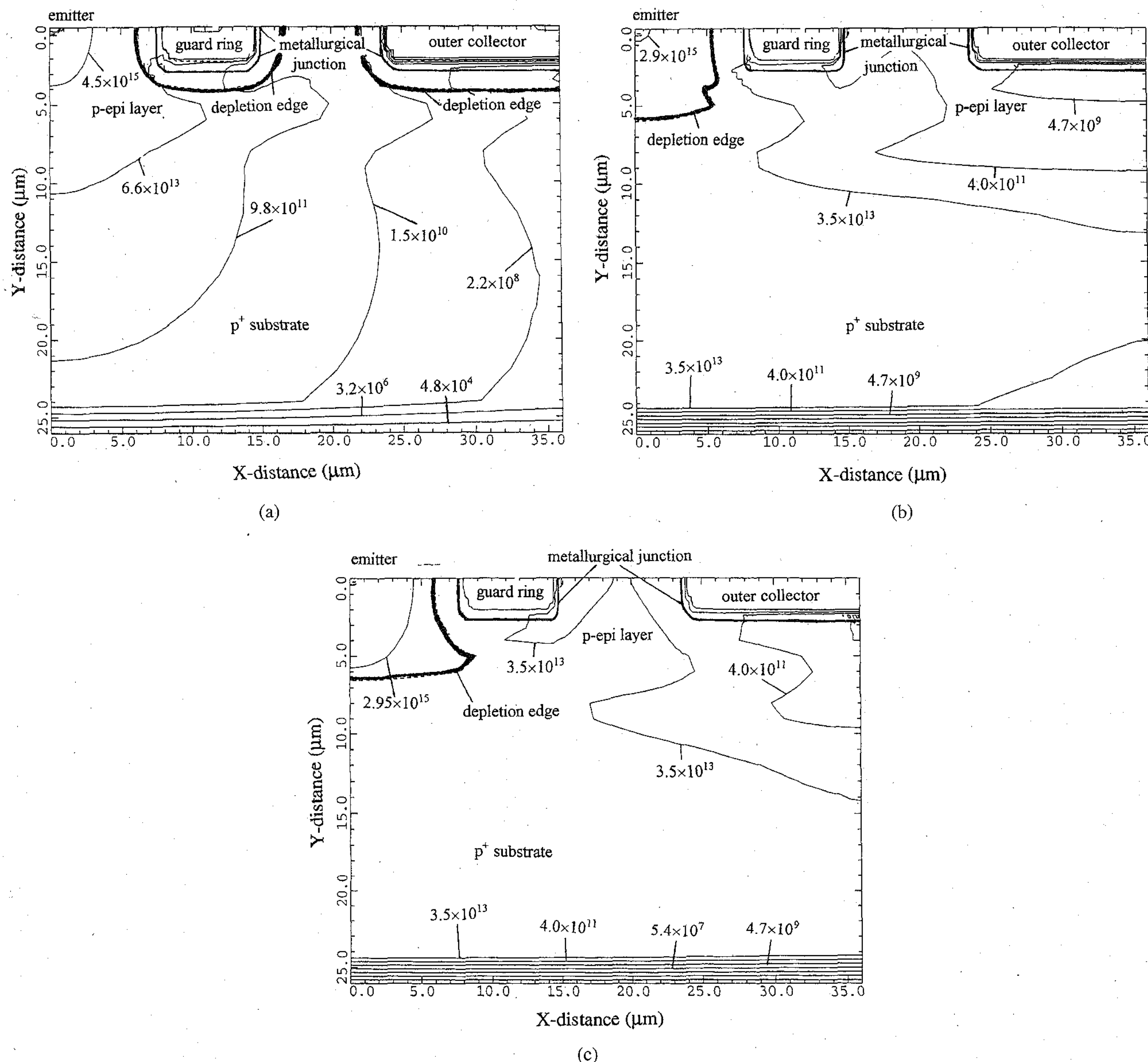

Fig. 3. 2-D minority carrier concentration contour: (a) at $V_{be} = 0.7$ V for RT, (b) at $V_{be} = 1.1$ V for 77 K, and (c) at $V_{be} = 1.4$ V for 77 K. The two bold lines in (a) around the two wells represent the depletion region edges. The bold lines in (b) and (c) have merged into a single line and shifted to the intrinsic region around the parasitic emitter.

Fig. 3(a) shows the 2-D minority-carrier concentration contour for $V_{be} = 0.7$ V at RT, while Fig. 3(b) and (c) for $V_{be} =$ 1.1 V and 1.4 V at 77 K, respectively. The depletion region edges at RT around both wells are smoothly parallel to the metallurgical junctions with the same shape, whereas at 77 K they are merged together in the area between the two n-wells and spread over the whole substrate, as indicated by the bold line in Fig. 3(b) and (c). Hence, the electric field is apparently distributed more widely at 77 K than RT. That is, low-temperature operation can be expected to cause more severe conductivity modulation after high-level injection, or equivalently high injection condition will be easily obtained by a smaller amount of minority carrier injection as a result of majority carrier freezeout, as reported in [5], [18], and [20]. At low temperatures the depletion region of a PN junction generally extends slightly, in this specific circumstance the number of mobile holes are not easy to increase near the emitter region due to freezeout, and hence holes which come from the very far n-well depletion edge increase the depletion region rapidly to form an almost fully depleted lightly-doped layer. More minority carrier contour lines gather near the bottom of the substrate and spread more deeply into the substrate, implying that more minority carriers have penetrated into the heavily-doped substrate and that the current in the heavily-doped substrate has become larger accordingly.

According to the recent studies [10], [11], the escape current I_{c2} is composed of two major components: the first component is due to the minority carriers injected into the sandwich layer between the well bottom junction and the epitaxial high/low junction, namely the sandwich current I_{san}; and the second is due to the minority carriers penetrating the high/low junction and spreading out in the large, heavily-doped substrate, namely the substrate current I_{sub}. Ordinarily the first component dominates the second especially for narrow guard

ring cases. At RT the I_{c2} equals I_{san} for narrow W_g while it becomes nearly the I_{sub} for wide W_g [12]. In contrast, at low temperature the I_{c2} totally equals the I_{san} for thicker epitaxial layer whereas it becomes the I_{sub} component flowing in the high/low junction transition region as in Fig. 5(b) for thinner epitaxial layer [12]. The I_{sub} deep into the substrate corresponds to the I_b in most cases at low temperature. These results will be discussed in the following sections. At high-level injection regime of the parasitic bipolar devices, the concentration of the minority carriers becomes comparable to that of the majority carriers, and both the diffusion and drift mechanisms should be considered for the I_{san}. In the respect of the diffusion mechanism, its temperature dependence can be expressed as [13]

$$J_{diff} = KT^3 \exp\left(-\frac{E_g}{KT}\right)\left[\exp\left(\frac{qV}{KT}\right)-1\right].$$

This temperature dependence is more than merely exponential change, in fact, diffusion current decreases by half for every 6°K decrease in temperature. Therefore, diffusion current at 77 K should decrease by a rather substantial amount. On the other hand, the drift component may increase due to enhanced mobility in moderately-doped semiconductors and/or expansion of electric field from 300 to 77 K. As for carrier mobility, it is well known that the temperature dependence of lattice scattering is generally proportional to $T^{-3/2}$. When temperature is lowered to 77 K, lattice scattering weakens and therefore carrier mobility increases. In our test structure the doping of the sandwich layer where most of the escape current flows is 2×10^{15} cm^{-3}. Mobility enhancement plays an important role undoubtedly. In addition to the mobility factor, the depletion region of the well bottom junction covers most of the sandwich layer as revealed by the numerical simulation. The electric field extends over nearly all of this district where most of the escape current flows. This field factor also contributes to a larger drift component. As regards the second escape current component in the heavily-doped substrate, the electric field also penetrates into this region. Hence the drift current at 77 K can still be expected to be larger than that at RT. Almost all the substrate current flows downward to the substrate contact as shown in Fig. 3(b) and (c) as well as the 2-D current-flow vector plot. As a result, the increased escape current should result from the enhanced drift component along the conductivity-modulated sandwich layer.

The drift current of minority carriers can be calculated by $qn\mu E$ with the electric field and the minority carrier concentration data along a specific line in the test structure from the simulated solutions. Minority carrier mobility μ is calculated by utilizing the same model used in the simulations. The calculated results for comparison between 0.7 V at RT and 1.1 V at 77 K are shown in Fig. 4(a)–(d). Fig. 4(a) and (b) illustrate the electric field distribution and electron drift current density, respectively, in the X-direction along a horizontal line at $Y = 4.5$ μm within the sandwich layer. The X-direction electric field at 77 K is very similar to that at RT except in the range from 13.5–25 μm, which is located between the two n-wells. In this district, the electric field at 77 K is much larger than that at RT. This confirms the wide distribution of the electric field over the sandwich layer at 77 K. In Fig. 4(b) the X-direction minority-carrier drift current density at low-temperature is larger than at RT along the entire line. The drift current density between the two n-wells, most of which flows directly into the outer n-well, is about 500 times greater at 77 K than that at RT. It is still about one order of magnitude greater under the outer n-well. Note that although the electric field under the outer n-well is nearly identical for both temperatures, the low-temperature current density is still greater than that at RT. The 2-D simulation results also indicate almost the same minority-carrier concentration for both cases, which verifies that mobility is enhanced at low temperature. Fig. 4(c) and (d) again, represent the electric field and electron drift current density, respectively, in the Y-direction along the same line. Once more the electric field is quite similar along the whole range except that between the two wells. In this case the electric field at 77 K is indeed smaller than that at RT. Nevertheless, at a distance farther than 25 μm, which is the region beneath the outer n-well, the drift current density in the Y-direction at 77 K is still greater. This fact again verifies the argument that mobility is enhanced.

The comparison addressed is further changed to a vertical line at $X = 20$ μm along the outer n-well sidewall. The results are shown in Fig. 4(e)–(h). The electric field and electron drift current in the X-direction are plotted in Fig. 4(e) and (f), respectively. The electric field at 77 K exhibits a more uniform distribution and is higher than that at RT along the whole depth of the substrate. Similar to the electric field, the electron drift current in the X-direction at 77 K is more uniform and over 500 times higher than that at RT. Here a larger portion of the current spreads into the heavily-doped substrate, where it becomes comparable in quantity to that in the sandwich layer. The current level at 77 K with depth less than 6.0 μm is clearly larger. Fig. 4(g) and (h) compare the electric field and electron drift current in the Y-direction along the same line. Once more the electric field at 77 K is distributed more uniformly into the heavily doped substrate and is weaker than that at RT in the depth range between 5.0 and 12.0 μm. This is due to the decrease of the built-in field across the p/p$^+$ transition junction, which will be discussed later. Nevertheless, the Y-direction electron drift current at RT is smaller than that at 77 K along the entire line. Not only the quantity of the current density below the high/low junction but also its uniform distribution throughout the substrate at 77 K are clearly observed. Therefore, the escape current I_{c2} at 77 K is larger than at RT due to drift component enhancement in the conductivity-modulated layer. The above discussions compare 0.7 V at RT and 1.1 V at 77 K, both of which represent the onset of high-level injection at two temperature. Conductivity modulation is obviously more significant and escape current can also be expected to be larger at low temperature for higher V_{be} bias. This can be observed in Fig. 3(c) that the minority carrier contours spread more deeply into the large substrate.

IV. Width-Dependent Characteristics

The simulation analysis now concentrates on the width-dependent behaviors of the guard ring. The simulated minority-

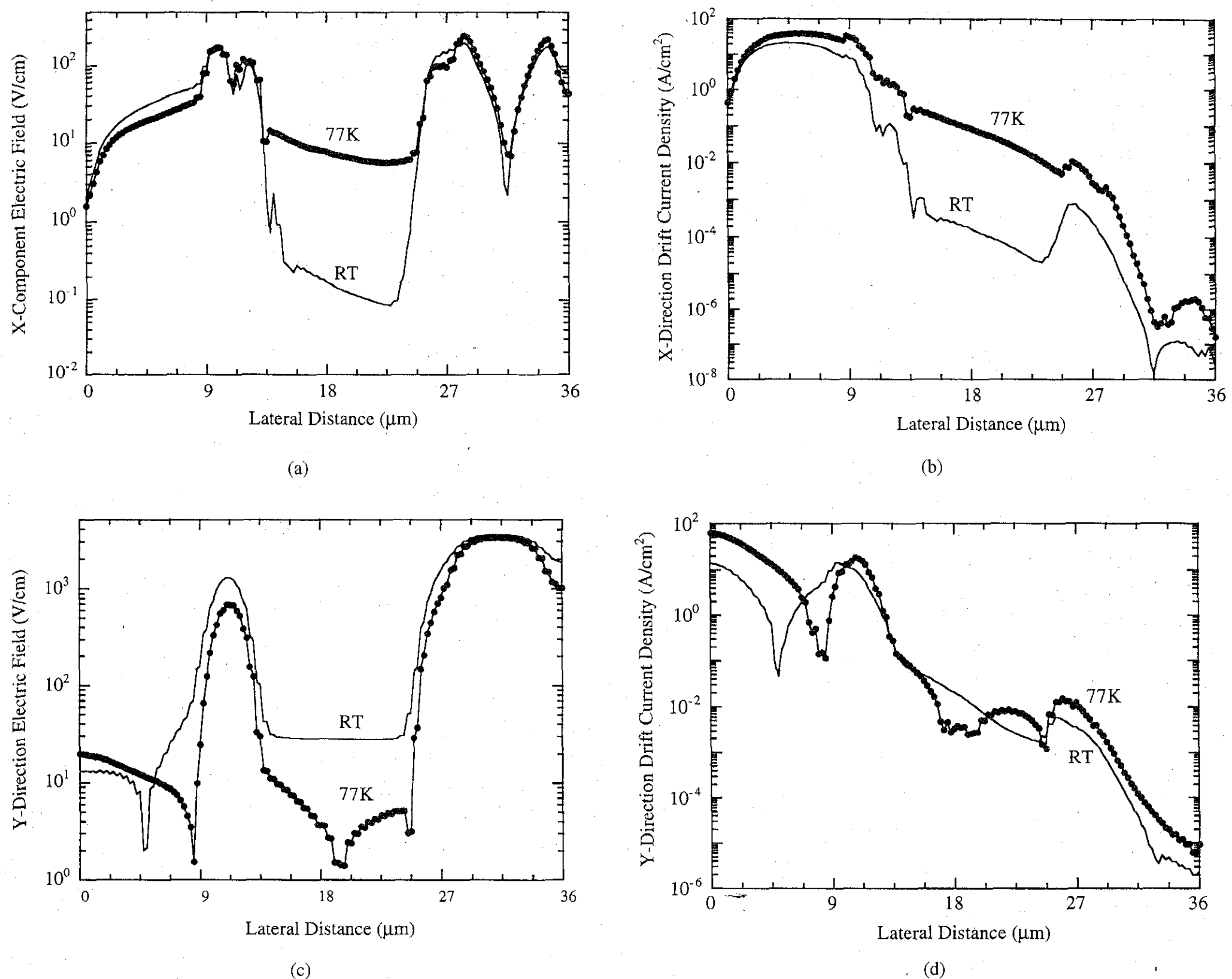

Fig. 4. Comparison of electric field distribution: (a) in the X-direction and (c) in the Y-direction between $V_{be} = 0.7$ V at RT and $V_{be} = 1.1$ V at 77 K along a horizontal line at $Y = 4.5\,\mu$m deep in the sandwich layer of the test structure. Comparison of calculated electron drift current density between $V_{be} = 0.7$ V at RT and $V_{be} = 1.1$ V at 77 K along this line (b) in the X-direction and (d) in the Y-direction.

carrier concentration contours and their current-flow vectors with $W_g = 40\,\mu$m at RT and 77 K are shown in Fig. 5(a)–(d). The depletion region spreads out over the whole epitaxial sandwich layer the same as the narrow guard ring case, while the depletion regions at RT retain the shapes of the n-wells. The depletion region extends the influence of the reverse-biased electric field deeply into the sandwich layer. The electric field can sweep the minority carriers of the I_{san} into the guard ring bottom, thus improving the collection capability of the guard ring, i.e., stronger width dependence of the I_{c2}. It is important to note that the depletion region all over the sandwich layer also contributes to the enhancement of the drift component flowing toward the outer n-well. Therefore, the two competitive tendencies combine into the present result, for a narrow guard ring its bottom junction is not long enough to collect most of the minority carriers in the sandwich layer. The I_{c2} at 77 K is dominated by the enhanced drift component and thus larger than that at RT. In contrast, for wide guard ring its bottom junction is long enough to capture most part of the minority carriers and few carriers can reach the distant outer well, i.e., the I_{c2} at 77 K is smaller than that at RT. As illustrated in Fig. 5(b), the I_{c2} is actually composed of only the minority carriers flowing along the high/low junction transition region and the I_{san} is completely absorbed by the n-well guard ring. The current vectors in the heavily-doped substrate also point toward the substrate contact completely. On the other hand, the current vectors of I_{c2} at RT all come from the heavily-doped substrate as shown in Fig. 5(d) and only a portion of the current vectors in the substrate flow toward the bottom contact. Fig. 5(a) and (c) also reveal such deeper penetration of the minority-carrier contours at 77 K than that at RT. Thus the I_{c2} at 77 K exhibits strong width dependence because they flow along the high/low transition region which is still strongly controlled by the guard ring as in [12]. In contrast, the I_{c2} at RT all come from the substrate, so the controllability of the guard ring becomes weak.

Normally, an epitaxial layer on a highly-doped substrate is the most effective structure for enhanced guard ring per-

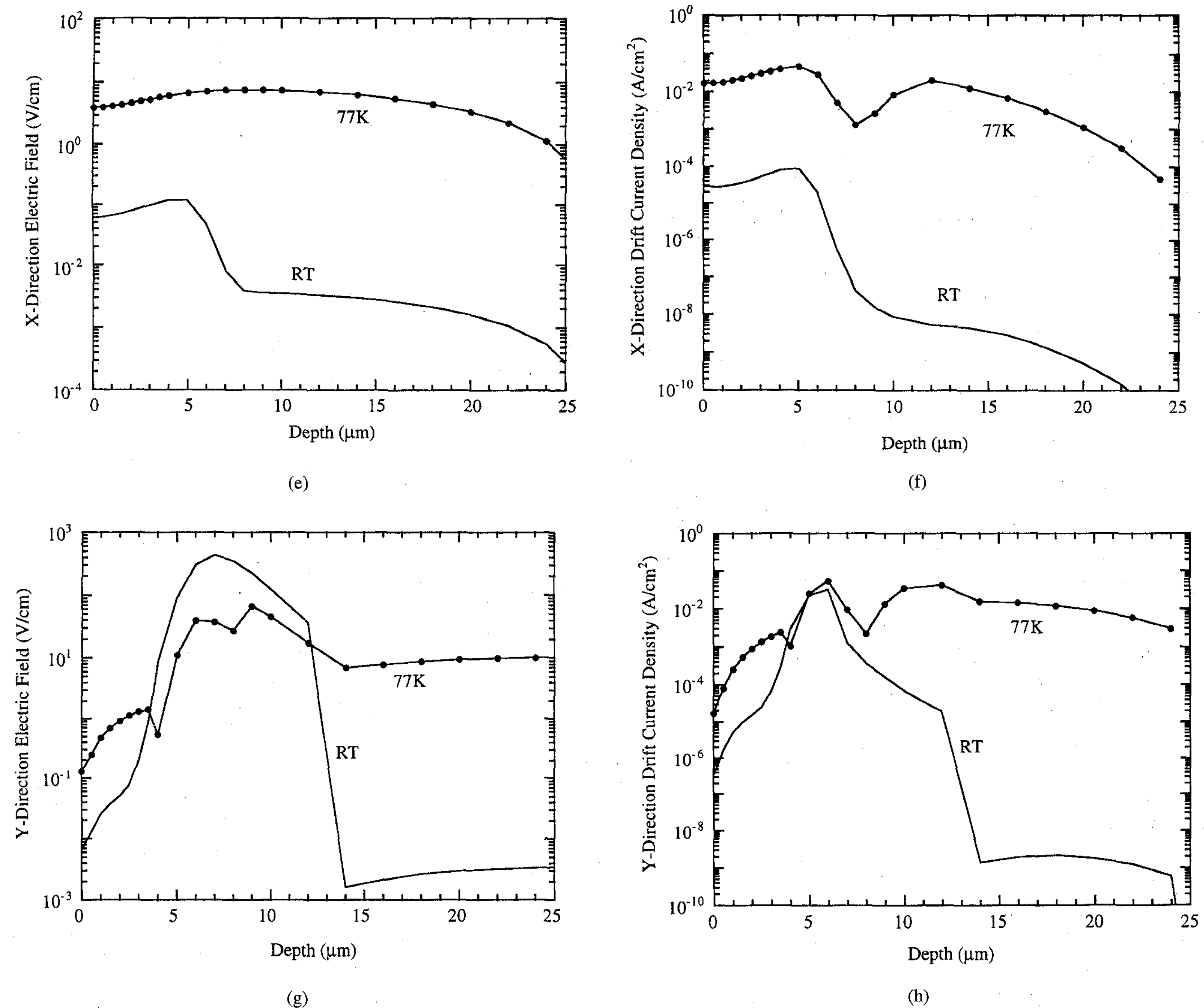

Fig. 4. (*Continued*). Comparison of electric field distribution. (e) in the X-direction and (g) in the Y-direction between V_{be} = 0.7 V at RT and V_{be} = 1.1 V at 77 K along a vertical line at $X = 20\,\mu$m beside the outer n-well sidewall of the test structure. Comparison of calculated electron drift current density between V_{be} = 0.7 V at RT and V_{be} = 1.1 V at 77 K along this line (f) in the X-direction and (h) in the Y-direction.

formance. A thinner epitaxial-layer thickness will lead to a stronger width dependence of the I_{c2} with a decrease in its magnitude [9]. In order to further understand the effect of the epitaxial-layer thickness on the I_{c2} characteristics between low temperature and RT, we consider different guard ring structures with several epitaxial-layer thicknesses by the numerical simulation. Fig. 6(a) shows the three types of ideal doping profiles along the depth direction beneath the guard-ring well. The epitaxial-layer thicknesses are about 2.5, 5, and 10 μm. The ideal 5 and 10 μm cases have the high/low junction transition regions from 5 to 6 μm, and from 9 to 11 μm, respectively. The two structures are identical except the epitaxial-layer thickness. The structure of the ideal 2.5 μm case with an ideal high/low junction, in which transition ranges only 0.5 μm wide, is based on a sub-half micron technology as cited in [25]. Fig. 6(b) shows the I_{c2} versus W_g characteristics for the ideal 10 μm case. The biases at which the I_{c2} is measured for the RT and 77 K cases are chosen to correspond to the same amount of the I_e. The I_{c2} at 77 K is greater than that at RT. Moreover, the slope of the I_{c2} at 77 K with low bias is about the same as that at RT and becomes more gradual than that at RT when the V_{be} bias becomes larger. Fig. 6(c) shows the $I_{c2} - W_g$ characteristics for the ideal 5 μm case. For low V_{be} bias the I_{c2} exhibits a similar tendency with the experimental results whereas for high V_{be} bias the behavior resembles that of the ideal 10 μm case. Fig. 6(d) illustrates the $I_{c2} - W_g$ characteristics for the ideal 2.5 μm case. A similar tendency with the experiments appears for all V_{be} biases. The I_{c2} also exhibits a saturation phenomenon due to the dominance of the I_{sub} [11], [12]. Fig. 6(d) indicates that the saturation property is improved by several orders of magnitude when operated at low temperature. This can be attributed to the better minority-carrier collection capability of the heavily-doped substrate at 77 K and the positive temperature dependence of the well-junction leakage current as well.

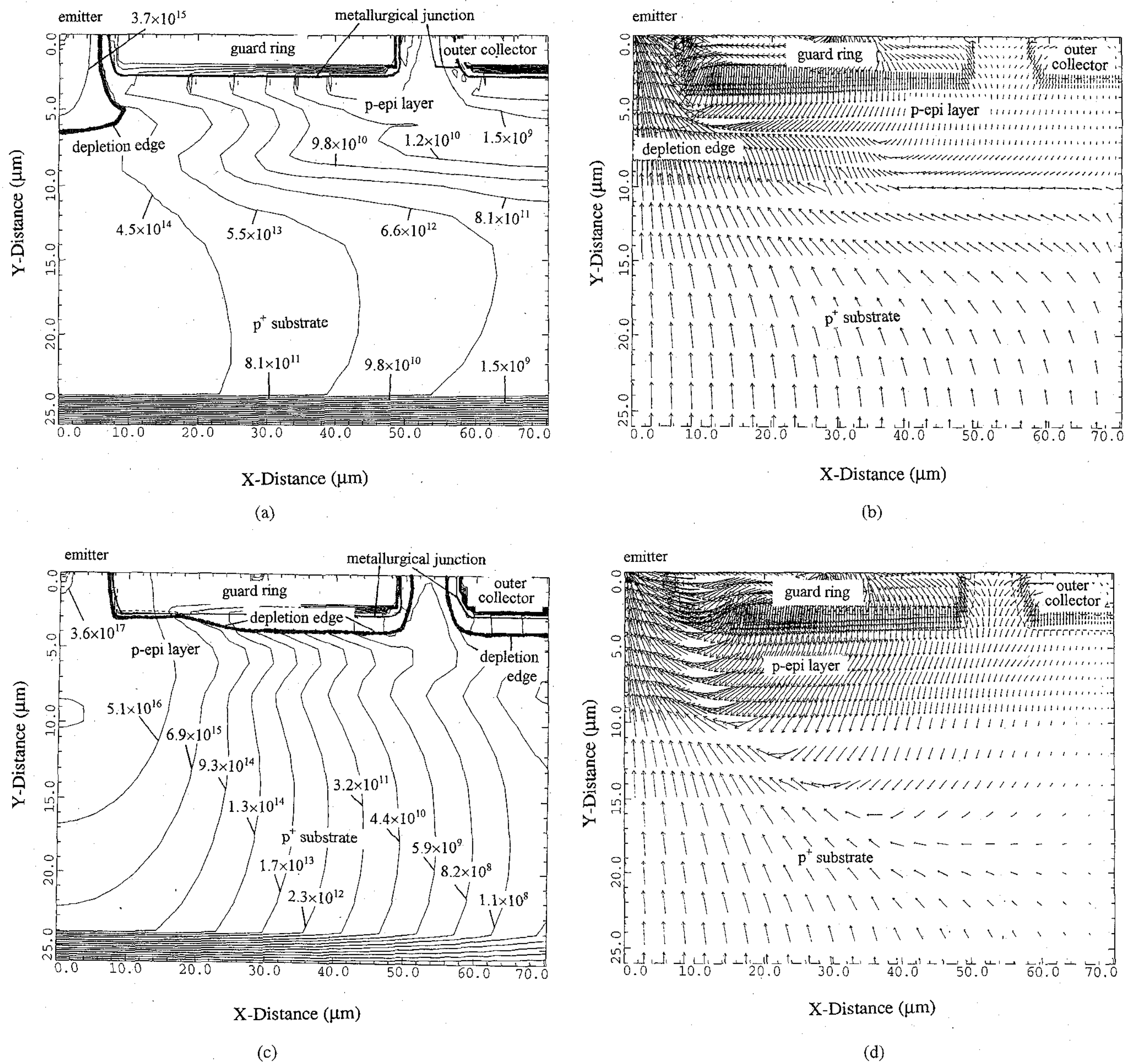

Fig. 5. The 2-D minority-carrier concentration contours with $W_g = 40$ μm (a) at $V_{be} = 1.5$ V for the 77 K case, (c) at $V_{be} = 1.0$ V for the RT case. The plot of 2-D minority-carrier current vectors with $W_g = 40$ μm (b) at $V_{be} = 1.5$ V for the 77 K case, and (d) at $V_{be} = 1.0$ V for the RT case.

Fig. 7(a)–(d) show the 2-D minority carrier contours and their current flow vectors, respectively, with ideal epitaxial-layer thickness of 10 μm and with W_g of 20 and 40 μm at 77 K. The depletion regions of the two n-wells in the 20 μm case are separated and the sandwich layer under the guard ring bottom becomes quasi-neutral because of the thicker epitaxial layer. In the 40 μm case the depletion region under the guard-ring well also shrinks partially. This clearly explains the degraded collection capability of the guard-ring well bottom. In addition, high-level injection in the lightly-doped epitaxial layer at 77 K is severer than that at RT and the high/low junction transition is also sharper than the test key profile. Hence the I_{c2} for this ideal 10 μm case exhibits a weaker width dependence and a greater magnitude than that at RT. Fig. 7(b) and (d) both shows that the lower portion of the current vectors flow horizontally along the sandwich layer, further confirming the uncontrollableness of the guard-ring well. The I_{c2} of the ideal 5μm case at low bias show a similar tendency to the experimental results owing to the certain similarities of the two structures, i.e., the experimental structure has an effective epitaxial layer of 6 μm. When V_{be} bias is close to 2.0 V, although the low-doped epitaxial layer is quite thin, the 2-D minority-carrier contours still reveal the separation of the depletion regions of the two n-wells. Such evidence explains the likeness between the ideal 5 μm case with large applied bias and the ideal 10 μm case at 77 K. As for the ideal 2.5 μm case, its behavior can also be interpreted by the same arguments. In conclusion, these all imply that the structure with a thinner epitaxial layer exhibits more significant width dependence and less magnitude of the I_{c2} for low temperature operation.

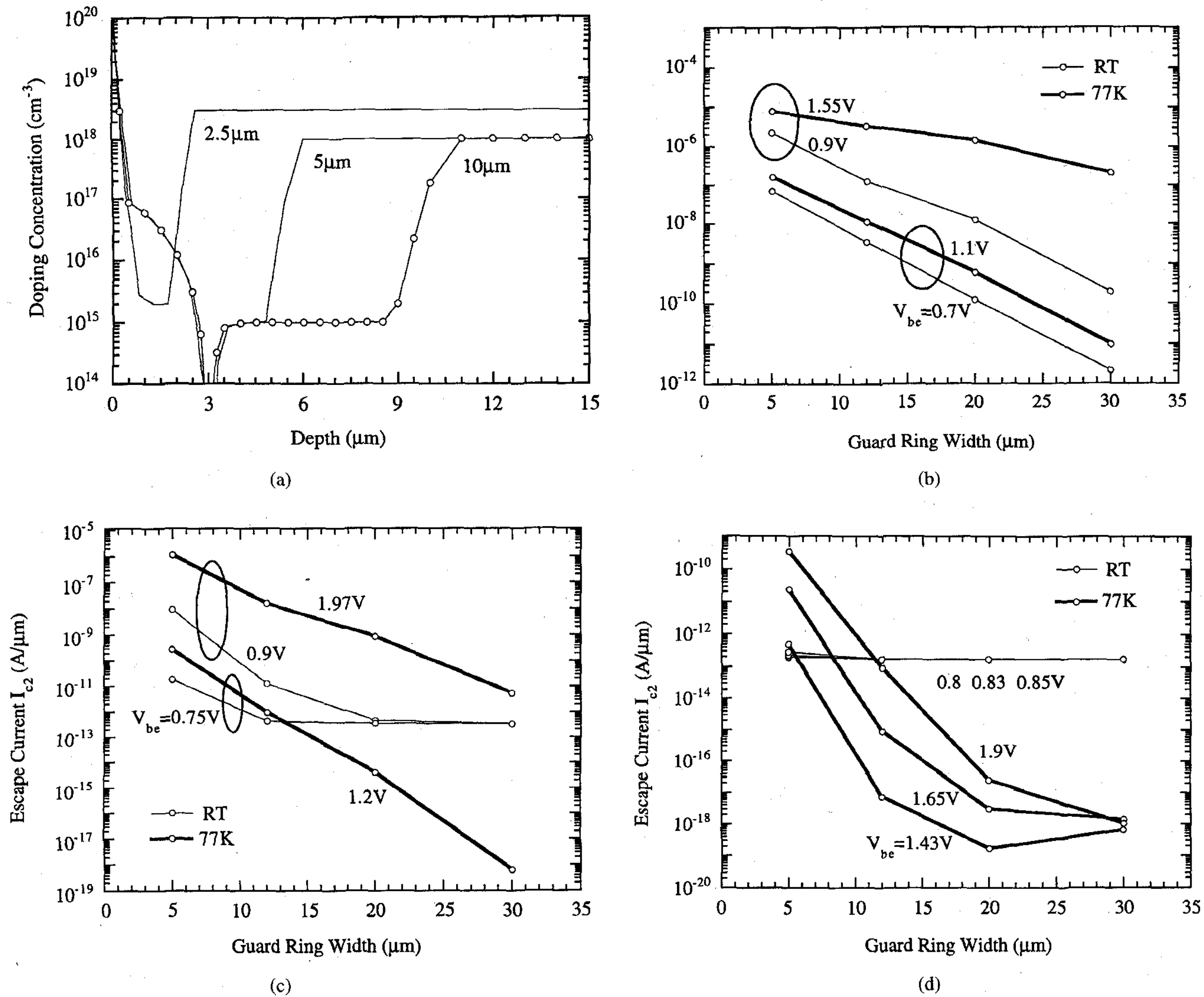

Fig. 6. (a) The ideal doping profile with the epitaxial layer thicknesses of 2.5, 5 and 10 μm along the depth direction under the guard ring. (b) The simulated characteristics of the I_{c2} as a function of W_g at RT and 77 K for the ideal 10 μm case. The V_{be} biases of the first comparison pair are 0.7 and 1.1 V, the second pair are 0.9 V and 1.55 V at RT and 77 K, respectively. (c) The simulated characteristics of the I_{c2} as a function of W_g at RT and 77 K for the ideal 5 μm case. The V_{be} biases of the first comparison pair are 0.75 and 1.2 V, the second pair are 0.9 and 1.9 V at RT and 77 K, respectively. (d) The simulated characteristics of the I_{c2} as a function of W_g at RT and 77 K for the ideal 2.5 μm case. The V_{be} biases of the first comparison pair are 0.8 and 1.43 V, the second pair are 0.83 and 1.65 V, and the third pair are 0.85 and 1.9 V at RT and 77 K, respectively.

V. Discussion

Carrier recombination in the base region requires some discussion. SRH recombination is a strong function of temperature [18], but because of the lack of a fully justified model the equation utilized at RT is used here for low-temperature simulation. The effect of SRH recombination indeed cannot be evaluated quantitatively. Nevertheless, carrier recombination plays an important role only at low-level injection. SRH recombination can be expected to be irrelevant to the increase in the escape current for the narrow W_g case. Furthermore, Auger recombination, which is dominant in heavily-doped semiconductors, exhibits rather weak dependence on temperature and its coefficient, which decreases slightly from RT to 77 K, leads to a low recombination rate. This may be one of the factors that contribute to the larger amount of the minority carriers and the current density in the substrate. However, most of the substrate current flows toward the substrate contact. Hence, Auger recombination doesn't contribute to the increased escape current.

Base resistance R_b typically plays an important role in high-level injection characteristics. The R_b in this test structure is mainly determined by the intrinsic lightly doped epitaxial region between the emitter and the n-well guard ring, and the resistance of the substrate may be neglected because of the highly-doped concentration. The R_b of an ordinary vertical BJT at 77 K actually increases in the ideal diffusion region, but decreases in the high injection owing to more severe conductivity modulation at 77 K in the base region [5]. In general the R_b is influenced by the following factors: conductivity modulation, emitter crowding effect, and base pushout effect. Our specific structure is entirely free from emitter crowding effect as well as base pushout effect [18]. The R_b can be controlled only by conductivity modulation in the intrinsic base region. The R_b was extracted from solutions of simulation by means of dividing the potential difference

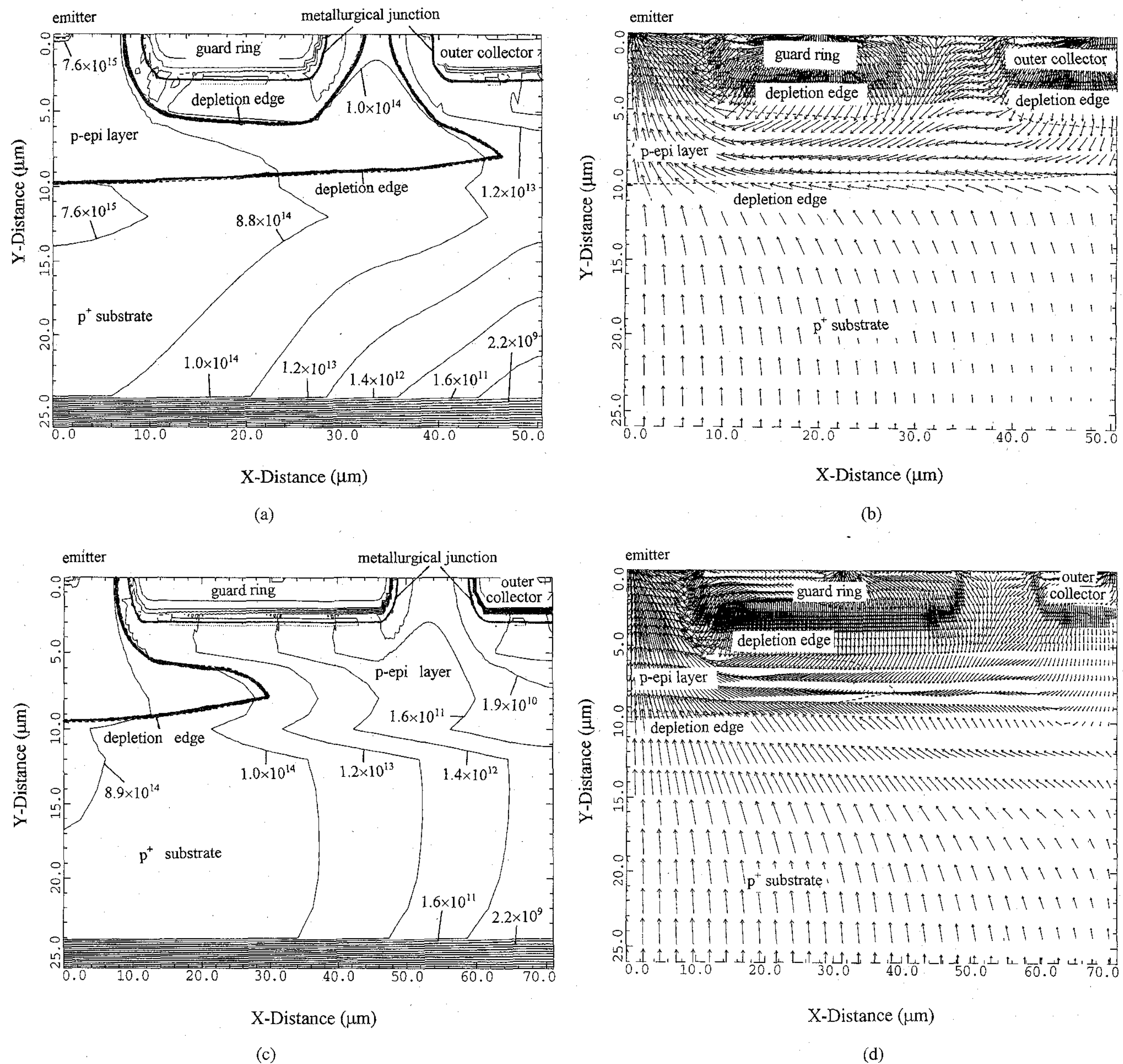

Fig. 7. The 2-D minority-carrier concentration contour of the ideal 10 μm case with W_g = (a) 20 and (c) 40 μm at V_{be} = 1.6 V for 77 K. The plot of 2-D minority-carrier current vector of the ideal 10 μm case with W_g = (b) 20 and (d) 40 μm at V_{be} = 1.9 V for 77 K.

in the base region by the base current. It was calculated to have a value which decreases with decreasing temperature in agreement with [5]. In fact, both the reduced R_b and the enhanced drift current can be traced back to conductivity modulation in high-level injection.

Epitaxial p/p$^+$ high/low junction at low temperature also exhibits behavior far different from PN junction, as shown in Fig. 8. At low temperature semiconductors are well known to become more degenerate, that is, both ϕ_{fp} and ϕ_{fn} become larger. Thus built-in potential $\phi_{fp} + \phi_{fn}$ of a PN junction increases as temperature decreases [15]. In contrast, built-in potential of a p/p$^+$ high/low junction at thermal equilibrium exhibits an opposite tendency, as demonstrated in Fig. 8. The Fermi level on the lightly-doped side approaches the valence band as the temperature decreases while on the heavily-doped side the doping is above the Mott transition [18], it is not subject to freezeout and hence no shift in the Fermi level occurs. As a result ϕ_{fp} increases, causing more degenerate on the lightly-doped side. The built-in potential of the high/low junctions, which is equal to $E_g/2q - \phi_{fp}$, is reduced along with the decreased temperature. Therefore, at low temperature minority-carrier reflection ability of the high/low junction diminishes as a consequence of the reduced built-in field. In other words, the substrate absorbs minority carriers more effectively at low temperature. This phenomenon can clearly be seen from the minority-carrier contour lines in Fig. 3(a) and (b), which spread more widely into the heavily-doped substrate. This is also shown in Fig. 4(f) and (h), in which a greater amount of the minority-carrier current at low temperature is observed. Hence the lowering of the built-in potential is also a contributing factor for the strong width dependence of the I_{c2}.

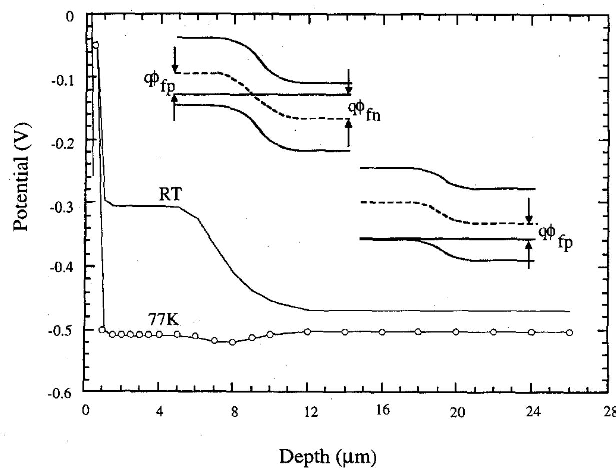

Fig. 8. Comparison of potential distribution at thermal equilibrium between RT and 77 K along the depth direction at $X = 0.0$ μm. The inserted graphs illustrate the energy band diagrams of the PN junction and p^+/p high/low junction.

Finally, several design considerations of the guard ring for better low-temperature operation may be drawn from the above experimental and simulated results. In spite of a special latch up-free case reported in [4], latch up still exists generally in CMOS operated around 77 K [26], i.e., reducing temperature is just one of the possible parameters for latch up elimination design. Therefore, the design issues addressed below may provide further information for total latch up suppression or at least other leakage prevention at low temperature. First of all, the lightly-doped epitaxial layer on a heavily-doped substrate becomes more essential at low temperature than at RT. The epitaxial-layer thickness should be as thin as possible to eliminate the I_{san}, which is usually the dominant component of the I_{c2}. From the above results the epitaxial-layer thickness should be kept at least below 10 μm. The limiting epitaxial-layer thickness is equal to the n-well depth such that the I_{san} vanishes totally. In view of the better sinking capability of the heavily-doped substrate, minority-carrier guard rings may be accompanied by majority-carrier guard rings connected with the substrate [27]. In such circumstance the majority-carrier guard rings can collect not only majority carriers but also minority carriers the same as the heavily-doped substrate does. Next, if the epitaxial layer thickness is around 10 μm, the W_g should be kept larger, for example, about 20 μm for better low-temperature performance. As the epitaxial-layer thickness decreases the minimum W_g for better performance can be reduced. To sum up, these considerations for enhanced low-temperature performance have a similar trend as those at RT. This similar tendency is beneficial and convenient for both temperature operations by using only one design structure.

VI. Conclusion

The experiments and simulations concerning the performance of the minority-carrier well-type guard ring have been compared between RT and 77 K. The comparisons under the same amount of the minority carrier density give a more deep insight. The escape probability of a narrow guard ring is about one order of magnitude higher at 77 K and its width dependence becomes more significant than that at RT. This property has been investigated in detail by the numerical simulations. Design considerations have also been drawn from these experiments and simulations. A lightly-doped epitaxial layer on a heavily-doped substrate exhibits more significance in the guard ring efficiency at low temperature, and its thickness should be kept as thin as possible.

Acknowledgment

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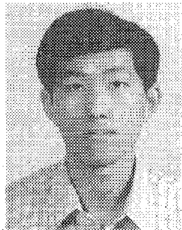
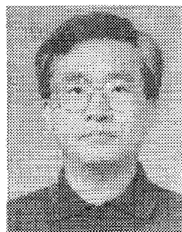


Chih-Yao Huang (S'87–M'95) was born in Hsinchu, Taiwan, R.O.C., on May 31, 1963. He received the B.S. degree in electrical engineering from the National Tsing-Hua University, Hsinchu, in 1985, and the M.S. and Ph.D. degrees in electronics engineering from the National Chiao-Tung University, Hsinchu, in 1987 and 1994, respectively.

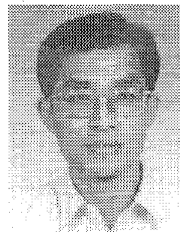
From 1987 to 1989, he served in the Chinese Air Force, and from 1991 to 1993, he was a part-time lecturer in the Institute of Electronics, National Chiao-Tung University. In 1995, he joined Mosel/Vitelic Inc., Hsinchu, working on the analysis and design of submicron semiconductor devices.



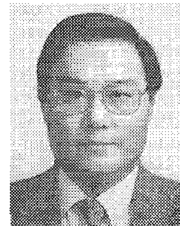
Ming-Jer Chen (S'77–M'86) was born in Taiwan, R.O.C., on April 1, 1954. He received the B.S. degree with highest honors from the National Cheng-Kung University in 1977, and the M.S. and Ph.D. degrees in electrical engineering from the National Chiao-Tung University (NCTU), Hsinchu, in 1979 and 1985, respectively. His doctoral work involved the modeling and prediction of CMOS latch-up.

From 1979 to 1980, he worked at the Telecommunication Laboratories establishing a multiproceesor distributed system. From 1985 to 1986, he conducted post-doctoral research on CMOS latch-up at NCTU. From 1986 to 1992, he was an associate professor and in 1993 became a professor, Department of Electronics Engineering, NCTU. From 1987 to 1992, he set up a series of design rules for the Taiwan Semiconductor Manufacturing Company. His current research interests include deep submicron reliability, low power integrated circuits, and subthreshold CMOS and BiCMOS technologies for new applications. He holds five Taiwan patents and two U.S. patents in the above fields.

Dr. Chen has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, *Solid-State Electronics*, and the *Journal of the Chinese Institute of Engineers*. He is a member of Phi Tau Phi.



Jeng-Kuo Jeng received the B.S. degree in electrophysics in 1982, and the M.S. degree in electronics engineering in 1990, from the National Chiao-Tung University, Hsinchu, Taiwan. He joined the ERSO/ITRI, Hsinchu, in 1984, where he was an integrated circuits reliability and failure analysis engineer in the QRA group. He joined Vanguard Co., Hsinchu, in 1994, and is currently a senior failure analysis engineer for memory products. His technical interests include reliability physics in DRAM and ESD in particular.



Ching-Yuan Wu (M'72) was born in Taiwan, R.O.C., on March 18, 1946. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University in 1968, and the M.S. and Ph.D. degrees from the State University of New York (SUNY) at Stony Brook, in 1970 and 1972, respectively.

During the 1972–1973 academic year, he was appointed as a Lecturer, Department of Electrical Sciences, SUNY-Stony Brook. During the 1973–1975 academic years, he was a Visiting Associate Professor, National Chiso-Tung University (NCTU), Hsinchu, Taiwan, R.O.C. In 1976, he became a Full Professor in the Department of Electronics and the Institute of Electronics, NCTU. At NCTU, he was the Director of Engineering Laboratories and Semiconductor Research Center from 1974 to 1980; the Director of the Institute of Electronics from 1978 to 1984; and the Dean, College of Engineering, from 1984 to 1990. He was a principal investigator of the National Electronics Mass Plan-Semiconductor Devices and Integrated-Circuit Technologies from 1976 to 1979. His research activities have been in semiconductor device physics and modelings, Integrated circuit designs and technologies. His present research areas focus on the development of efficient 2-D and 3-D simulators for deep-submicrometer semiconductor devices, design rules and optimization techniques for deep-submicrometer CMOS devices, and key technologies for deep-submicrometer CMOS devices. He has published more than 180 papers in the semiconductor field and has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, *Solid-State Electronics*, etc.

Dr. Wu is a member of the Honorary Editorial Advisory Board of Solid-State Electronics and is a board member of the Chinese Engineering Society. He received the Academic Research Award in Engineering from the Ministry of Education (MOE), in 1979, the outstanding Scholar award from the Chinese Educational and Cultural Foundation, in 1985. From 1982 to 1995, he has received the outstanding research Professor fellowship from the Ministry of Education and the National Science Council (NSC), ROC. In 1992, he received the Distinguished Engineering Professor Medal Award from the Chinese Engineering Society. From 1982 to 1988, he was a Coordinator of the National Microelectronics Researches and High-Level Man-Power Education Committee, National Science Council, R.O.C. He has been the Research Consultant of the Electronics Research and Service Organization (ERSO), ITRI; a member of the Academic Review Committee, the Ministry of Education; and the chairman of the Technical Review Committee on information and Microelectronics Technologies, the Ministry of Economic Affairs.