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Dual gate indium-gallium-zinc-oxide thin film transistor with an unisolated floating metal gate for threshold voltage modulation and mobility enhancement

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In this study, we propose a floating dual gate (FDG) indium-gallium-zinc-oxide (IGZO) thin film transistor (TFT) with a floating metal back gate that is directly contact with IGZO without a dielectric layer. The floating back gate effect is investigated by changing the work function (ϕ) of the back gate. The FDG IGZO TFT exhibits an improved field-effect mobility (μ), unchanged subthreshold swing (SS), high on/off current ratio, and a tunable threshold voltage ranged (V_{th}) from −5.0 to +7.9 V without an additional back gate power supply. © *2011 American Institute of Physics*. [doi:10.1063/1.3578403]

Amorphous metal-oxide such as amorphous indium-gallium-zinc-oxide (*a*-IGZO) based transistors has attracted much attention for their excellent characteristics, like high mobility[1] and uniform amorphous structure.[2] However, the lack of feasible p-type semiconductor[3,4] limits its application on logic circuit. To realize a basic inverter unit with metal oxide transistors, two n-channel transistors with different threshold voltages are required. In previous reports, Lee *et al.*[5] have proposed a means of threshold voltage adjusting by varying thickness. However, the depletion-mode thin film transistor (TFT) using thick body increases the subthreshold swing (SS) and the leakage current. Double gate TFT is another feasible approach that uses one gate with a constant voltage (control gate) to change the threshold voltage position during the main gate scanning.[6,7] Double gate TFT can adjust the threshold voltage position in both positive and negative direction. However, the additional power supply to the control gate makes the circuit design complicated. The fabrication of the top dielectric layer also increases the process cost.

In this study, we proposed a modified double gate a-IGZO TFT that can adjust the threshold voltage in both positive and negative directions without the additional dielectric layer and power supply. The control gate metal is formed directly on the back interface of the IGZO active layer. There is no dielectric layer between the IGZO body and the control gate, indicating a metal-semiconductor (MS) back gate. During device operation, the back gate is floated, and therefore the power supply for the back gate is not necessary. The back gate bias (V_{BG}) is provided from the intrinsic built-in voltage across the IGZO body and the back gate. Because there is no dielectric layer beside the back gate, the control ability of the floating back gate is better than that of the conventional back gate formed by a metal-oxide-semiconductor (MOS) diode. By choosing a floating back gate that processes work function higher or lower than that of IGZO (ϕ_{IGZO}), we can significantly move the threshold voltage (from −5.0 to 7.9 V). An inverter comprised of one enhancement-mode TFT [using gold (Au) as floating gate] and one depletion-mode TFT [using calcium (Ca) as floating gate] is demonstrate. Besides, as compared with the standard single gate devices (STD devices), the a-IGZO TFT with a floating back gate has an enlarged field-effect mobility and an almost unchanged SS.

A 100-nm-thick layer of thermal silicon nitride (SiN_x) was grown on Si wafers to serve as the dielectric. A 35-nm-thick active layer of *a*-IGZO was deposited by radio-frequency sputtering onto SiN_x through a shadow mask. The annealing process at 350 °C was conducted in a nitrogen furnace for 1 h. A single gate a-IGZO TFT (STD) was completed after a 50-nm-thick layer of aluminum (Al) was deposited through a shadow mask to form the source and drain. The channel width and length are 1000 μm and 300 μm, respectively. Then, the 150-μm-long metallic back gate was deposited on the IGZO top surface of some STD devices to form the double gate devices as shown in the inset of Fig. 1(a). The capping layer is located between the source and drain contacts. Various metal materials with different work functions include calcium (Ca, ϕ_{Ca}=2.78 eV), titanium (Ti, ϕ_{Ti}=4.33 eV), copper (Cu, ϕ_{Cu}=4.65 eV), and gold (Au, ϕ_{Au}=5.10 eV) were used as the floating back gate. Except Ca, the thickness of these capped layers is fixed as 60 nm. For Ca, to avoid oxidation, 100-nm-thick Al is passivated onto the 35-nm-thick Ca. The threshold voltage and mobility are extracted from the slope and the x-axis intercept of the $\sqrt{I_D}$-V_{GS} curve measured under saturation condition (V_{DS} =20 V, V_{GS} is scanned from −15 to 20 V).

Figure 1(a) presents the transfer characteristics of the uncapped (STD), Ti-capped, Ca-capped, and Au-capped a-IGZO TFTs. As compared with the STD device, there are significant V_{th} shifts of −7.4 V and 5.5 V of the Ca-capped and Au-capped devices, respectively; a small V_{th} shift of −1.7 V of Ti-capped device is probed. Capping a metal layer (a control gate without insulator) on the IGZO back surface does not form a current leakage path to increase SS and leakage current. In Fig. 1(b), the slopes of $\sqrt{I_D}$-V_G curves are raised by metallic capping layers, indicating a significantly

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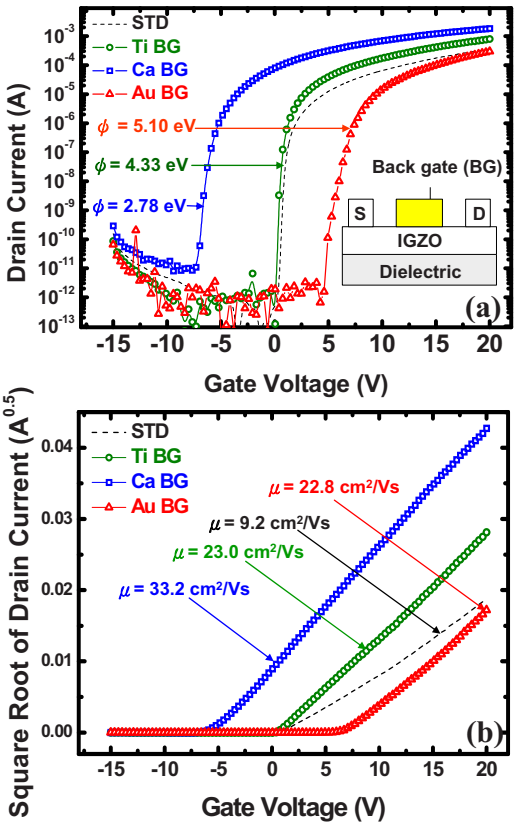

FIG. 1. (Color online) (a) The transfer characteristics and (b) the square root of drain currents plotted as a function of gate voltage of uncapped, Ca-capped, Ti-capped, and Au-capped a-IGZO TFTs.

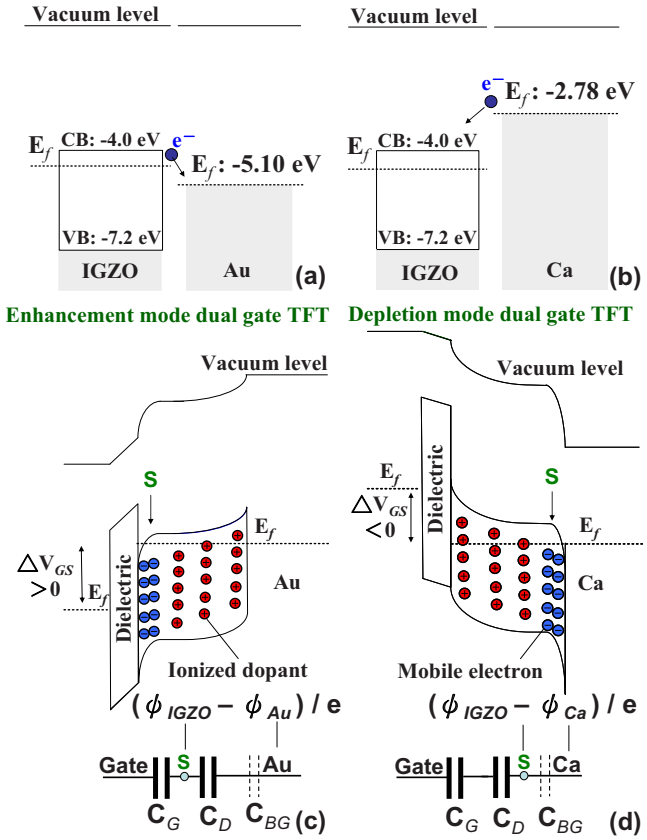

FIG. 2. (Color online) The energy band diagrams of IGZO, (a) Au, and (b) Ca before contacting. The energy diagram and equivalent circuit of (a) the enhancement mode dual gate IGZO TFT and (b) the depletion mode dual gate IGZO TFT.

improved field effective mobility. Table I lists the extracted typical parameters of a-IGZO TFTs with various metallic capping layers. A tunable V_{th} ranges from −5.0 to 7.9 V is demonstrated. Where the threshold voltage shift (ΔV_{th}) is the threshold voltage difference between STD device and the floating dual gate (FDG) device. Besides, all these FDG devices possess an improved field-effect mobility, a comparable SS (0.16–0.33 V/dec) and a high on/off current ratio ($>2.6\times10^8$).

The back gate bias (V_{BG}) is contributed from the intrinsic built-in voltage between IGZO body and the floating back gate. As shown in Figs. 2(a) and 2(b), before contact, the Fermi-level in Au and Ca are lower and higher than that of IGZO, respectively. After IGZO contacts with Au, the thermal equilibrium is attained with a constant Fermi-level. The electrons in IGZO flow into Au to form a built-in voltage and a depleted IGZO body as shown in Fig. 2(c). The system can be regarded as a conventional dual gate TFT that has a control gate with a negative gate-to-source voltage (always off).

TABLE I. The extracted parameters of a-IGZO TFTs with various metallic capping layers.

	ϕ (eV)	ΔV_{th} (V)	V_{th} (V)	μ (cm^2/V s)	SS (dec/V)	On/off
Ca	2.78	−7.4	−5.0	33.2	0.33	2.6×10^8
Ti	4.33	−1.7	0.7	23.0	0.16	5.7×10^8
Cu	4.65	0.6	3.0	17.3	0.23	4.1×10^9
Au	5.10	5.5	7.9	22.8	0.27	4.5×10^8
STD	⋯	⋯	2.4	9.2	0.27	3.5×10^8

The voltage is contributed from the work function difference, $(\phi_{IGZO}-\phi_{Au})/e$, where e is the electron charge. Because Au depletes the IGZO body, the channel formation on the dielectric will be suppressed and the V_{th} is increased (enhancement mode TFT). On the contrary, as shown in Fig. 2(d), Ca injects electrons into IGZO body. The injected electrons accumulate near the interface between IGZO and Ca to form a channel. The system can be regarded as a conventional dual gate TFT that has a control gate with a positive gate-to-source voltage (always on). The voltage is contributed from the work function difference, $(\phi_{IGZO}-\phi_{Ca})/e$. Because Ca generates a channel on the IGZO back surface, the V_{th} becomes more negative to suppress the initially existed channel to turn-off the device (depletion mode TFT). Due to the thin active layer (e.g., 35 nm), the devices are operated with a fully-depleted IGZO body.[6,7] The proposed double gate transistor can be regarded as a composition of three capacitors. They are the capacitor of the bottom main gate (C_G, which is formed by the gate dielectric), the depletion capacitor (C_D, which is formed by the depleted IGZO body) and the capacitor of the back gate (C_{BG}, which is formed by the MS back-gate contact).[7] In the case of the enhancement mode operation, the channel forms on the dielectric surface and the body is depleted by the back gate. Therefore, the channel is located between C_G and C_D as shown in the bottom of Fig. 2(c). On the contrary, in the case of the depletion mode operation, the channel forms on the interface between IGZO and the back gate and the IGZO body is depleted by the bottom gate. Therefore, the channel is located between C_D and C_{BG} as shown in the bottom of Fig. 2(d). Under enhance-

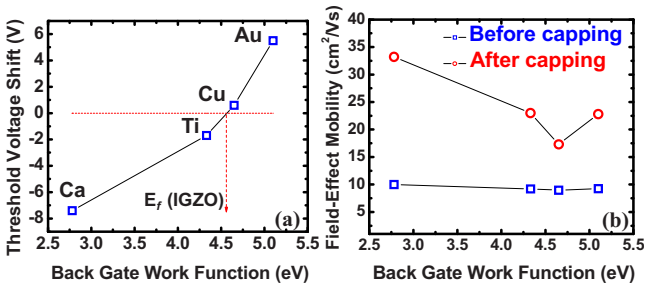

FIG. 3. (Color online) (a) The threshold voltage shift and (b) the field-effect mobility plotted as a function of the work function of the back gate.

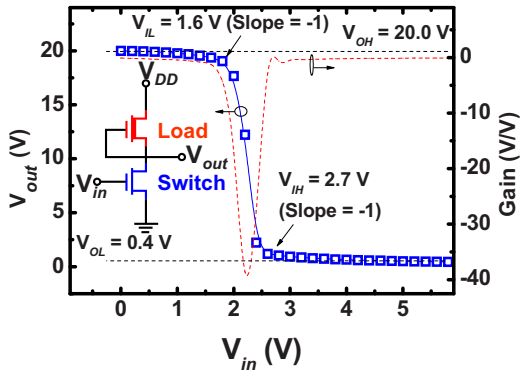

FIG. 4. (Color online) The voltage transfer curve and the voltage gain of the inverter comprised of one Ti-capped device (switch) and one Ca/Al-capped device (load). The inverter circuit is shown in the inset.

ment mode operations, the back-gate-voltage dependent threshold voltage shift (dV_{th}) can be estimated by the formulas as: $dV_{th}C_G = -dV_{BG}[C_D C_{BG}/C_D + C_{BG}]$. Under depletion mode operation, dV_{th} can be given as $dV_{th}[C_G C_D/C_G + C_D] = -dV_{BG}C_{BG}$.[7] Compared to the conventional dual gate TFT that uses a MOS diode as the back gate, the MS back gate contact in this study leads to a high capacitor (C_{BG}). As a result, a small back gate voltage (V_{BG}) can shift the V_{th} significantly. The derivation of V_{th} to back gate voltage, dV_{th}/dV_{BG}, is as high as 5 for the proposed dual gate TFT.

Figure 3(a) presents the threshold voltage shifts plotted as a function of work function of the floating back gate. The V_{th} shift ranging from −7.4 to 5.5 V is approximately linearly dependent with the work function of floating gate. A point that corresponds to zero V_{th} shift can estimate the work function of a-IGZO. Figure 3(b) shows the field effective mobility of a-IGZO TFT plotted as a function of work function of the floating back gate. All kinds of back gate metals raise the mobility. The field-effect mobility is improved two to three times. The improved mobility in dual gate TFT was also reported in Ref. 6. The mechanism is still not clear but could be related to the change in the field distribution in the channel by adding the back gate. The hysteresis behavior of metal-capped devices was also investigated. No noticeable hysteresis effect was observed, indicating that the metal capping does not generate additional defect states.[8]

An inverter comprised of an enhancement-mode a-IGZO TFT (Ti back gate) to serve as a switch and a depletion-mode a-IGZO TFT (Ca back gate) to serve as the load is demonstrated as shown in the inset of Fig. 4. The voltage transfer curve and the voltage gain of the inverter is shown in Fig. 4. With a supply voltage (V_{DD}) of 20 V, a signal inversion behavior with a maximum voltage gain of −39 V/V is obtained. The maximum input voltage that will be recognized as a low input logic level (V_{IL}) is 1.6 V. The minimum input voltage that will be recognized as a high input logic level (V_{IH}) is 2.7 V. The output high voltage (V_{OH}) is 20 V and the output low voltage (V_{OL}) is 0.4 V. The transfer width, defined as $V_{IH} - V_{IL}$, is only 1.2 V.

In this study, a dual gate IGZO TFT with a floating MS back contact is proposed to modulate the threshold voltage and to increase the field-effect mobility. The floating back gate has a back-gate bias (V_{BG}) contributed from the built-in voltage between the IGZO and the capping metal. By using various floating metals, a depletion mode or an enhancement mode dual gate TFT can be achieved. An improved mobility is also obtained in the proposed FDG TFT. An inverter comprised of the proposed dual gate a-IGZO TFTs has a maximum voltage gain of −39 V/V with a supply voltage of 20 V.

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