行政院國家科學委員會專題研究計畫　成果報告

新式非揮發性記憶體元件之研究(I)

計畫類別：個別型計畫
計畫編號：NSC94-2215-E-009-086-
執行期間：94 年 08 月 01 日至 95 年 07 月 31 日
執行單位：國立交通大學電子工程學系及電子研究所

計畫主持人：荊鳳德

報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 95 年 8 月 4 日

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中 華 民 國 95 年8 月2 日

行政院國家科學委員會補助專題研究計畫

■成果報告□期中進度報告

新式非揮發性記憶體元件之研究(I)

計畫類別：■ 個別型計畫　□整合型計畫

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計畫主持人：荊鳳德

共同主持人：

計畫參與人員：

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

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執行單位：交通大學電子所

中 華 民 國 九十五 年 七 月 二十七 日

行政院國家科學委員會研究計畫成果報告

新式非揮發性記憶體元件之研究(I)

計畫編號: NSC 94-2215-E-009-086-
執行期限：94年8月1日至 95年7月31日

主持人：荊鳳德 教授 執行單位：交通大學電子工程系

中文摘要

使用具有高捕陷能力的新穎材料 AlN (k=10), 利用在高介電值層有較低壓降以及使用高功函數的 IrO_2 來降低漏電流, SiO_2/AlN/HfAlO(k=17)/IrO_2 元件, 在 85°C 時展現了良好的記憶體特性，以及 100us 的 erase 速度, 在 13V 的 program/erase 低操作電壓下, ΔV_{th} 可達 3V, 利用外插的方式, 經過十年的保持, 記憶體的 window 仍可維持 1.9V, 若將 erase 的速度降低為 1ms, 則 ΔV_{th} 可達到 5.5V, 在 85°C 十年的保持情況下, 記憶體的 window 將增加為 3.4V。

一、簡介

Fundamental challenges for advanced non-volatile memory are the continuous down-scaling program/erase (P/E) time and operation voltage, while still maintaining good 10 years data retention. Although the MONOS memory provides a potential solution for down-scaling the gate oxide beyond conventional floating gate memory, further performance improvements with larger ΔVth of charge-tapping in nitride and faster erase time at low voltage are required [1]-[4]. Of the known high-κ dielectrics, AlN has a better charge-trapping capability than Si_3N_4 and Al_2O_3 as well as unique P/E memory characteristics [5]. In this paper, we report the memory performance of novel IrO_2-HfAlO-AlN-SiO_2-Si MONOS device. At ±13V and fast 100us P/E, we found a large ΔVth of 3.7V that extrapolated to 1.9V for 10-year retention at 85°C. The 85°C initial ΔVth and 10-year retention window further increase to 5.5V and 3.4V for 1ms erase. Such fast P/E also gives large 10^5-cycled ΔVth window due to small stress on tunnel SiO_2. The good retention is due to the strong Al-N ionic bond related higher trapping capability. The very fast 100us erase is owing to the high electric field (E) over tunnel SiO_2 from D ($\varepsilon_0 \kappa E$) continuity of high-κ HfAlO (κ=17) barrier and AlN (κ=10) trapping layer. The low P/E voltage is from the efficient charge-trapping AlN, very high 3.5fF/um^2 capacitance density for charge storage, large E field in SiO_2 and high workfunction IrO_2 metal gate [6] for low gate carrier injection during erase. These results are among the best reported data [1]-[4] summarized in Table 1.

二、實驗步驟

The IrO_2-HfAlO-AlN-SiO_2-Si devices were formed by first growing a 2.8 nm thermal SiO_2, depositing 12 or 16 nm AlN by PVD [5], 13 nm HfAlO by ALCVD, 50nm IrO_2 metal-gate [6], followed by gate definition, self-aligned ion-implantation and 85°C RTA. The fabricated devices were characterized by P/E, cycling and retention tests at 85°C.

三、結果與討論

A. P/E Characteristics:

Fig. 1 shows the schematic band diagram of SiO_2/AlN/HfAlO/IrO_2 devices. The strong trapping AlN can reduce the P/E voltage even for thin AlN. The 5.1eV high workfunction [6] is important to scale down the HfAlO thickness and erase voltage. This is evidenced from the 1 order of magnitude lower Jg in Fig. 2 than a previous report of a similar structure [3] also under -10 to -15V erase. This is consistent with the >10X lower Jg in IrO_2/high-κ pMOS than mid-gap metal-gate device [6]. The C-V hysteresis curves, in Fig.3, show very large ΔVth shifts of 7-10V. The capacitance further increases to 3.5 fF/um^2 for 12nm AlN MONOS to give large charge storage at low voltage. The detailed P/E characteristics from Id-Vg are shown in Figs. 4-5 for thicker 16nm AlN MONOS. A fast P/E time of 100us-1ms are measured at ±13V, with a large ΔVth shift. The ΔVth and P/E speed are improved using the thinner 12nm AlN MONOS. As shown in Figs. 6-7, the 13V 100us program gives 3.3V ΔVth change and the -13V 100us erase has -3.7V ΔVth. Even a ΔVth shift of 2.1V and -1.8V is obtained at 10us and ±13V P/E. Such very fast erase is ~10X better than published data [1]-[4] with larger ΔVth. It arises from the higher electric field in thin 2.8nm SiO_2 due to a smaller voltage drop in small EOT high-κ HfAlO (κ=17) barrier and trapping AlN (κ=10) from $\varepsilon_0\kappa E$ continuity. The high work-function IrO_2 gate [6] also helps the erase by largely reducing charge injection from gate with thin HfAlO.

B. Retention & Cycling:

Figs. 8-10 show the retention data. The 10-year retention ΔVth is larger for 12nm than and 16nm AlN devices with only slightly faster decay rate. The extrapolated 10-year memory window at 25^{o}C for 12nm AlN device, increases from 2.4 to 4.1V with increasing erase time from 0.1 to 1ms. Still a large 10-year window at 85^{o}C of 1.9 or 3.4V was obtained for 100us or 1ms erase and 100us program at ±13V. This is above the best reported data [1]-[4] in Table 1. Besides, the 85^{o}C highand low-level retention decay rate of 120 and only 64mV/dec are comparable with published data [1]-[4], with added merit of the largest initial ΔVth of 5.5V (3.7V) at 1ms (0.1ms) -13V erase. This large memory window arises form the strong Al-N ionic bond to give better trapping capability than Al_2O_3 and Si_3N_4. Good endurance is also obtained in Figs. 11-12. At 85^{o}C and ±13V, big 10^5-cycled memory window of 2.9 or 4.6V and 10k-cycled 10-year retention window of 1.6 or 2.7V are obtained at 0.1ms or 1ms erase. Such excellent endurance is due to the fast P/E time with less stress to tunnel SiO_2. Table 1 summarizes the important memory data. At 85^{o}C and ±13V P/E, good memory integrity of fast 100 to 1000us erase time, large ΔVth of 3.7 or 5.5V, big 10^5-cycled ΔVth of 2.9 or 4.6V, and good retention of large 10-year memory window of 1.9 or 3.4V are obtained at the same time in this MONOS device.

四、結論

Fast erase, large ΔVth, good retention and cycling are simultaneously obtained in SiO_2/AlN/HfAlO/IrO_2 devices.

五、參考文獻

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[3] C. H. Lee *et al, IEDM Tech. Dig.* (2003), p. 613.

[4] T. Sugizaki *et al*, *Symp.On VLSI Tech. Dig.* (2003), p.27.

[5] C. H. Lai *et al, 62th Device Research Conf. Dig.* (2004), p.77.

[6] D. S. Yu *et al, IEDM Tech. Dig.* (2004) p. 181

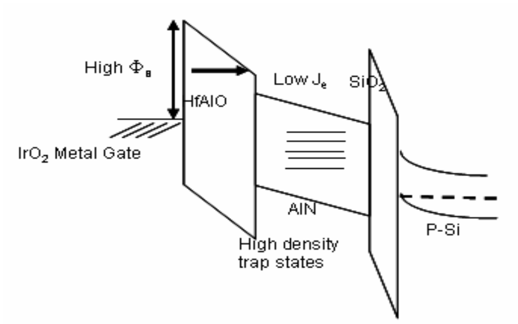


Fig.1. Band diagram of IrO_2-HfAlO-AlN-SiO_2-Si MONOS memory in erase state. The higher work-function IrO_2 allows thinner HfAlO w/o large electron injection into AlN.

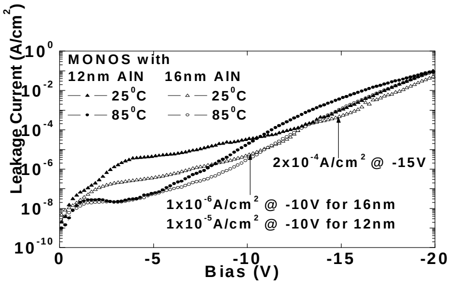


Fig.2. J_g-V_g curves of MONOS memory with 12nm and 16nm AlN at 25 and 85℃ The J_g is 1 order of magnitude lower than the data from [3] due to higher Φ_B of IrO_2.

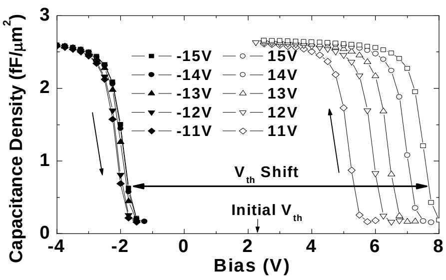


Fig.3. C-V hysteresis curves of MONOS capacitor with 16nm AlN for various V_g. The capacitance density increases to 3.5fF/μm^2 for 12nm AlN device.

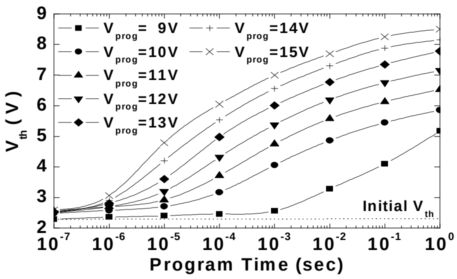


Fig.4. The measured program characteristics from I_d-V_g for 16nm AlN MONOS devices. The L_g is 10μm.

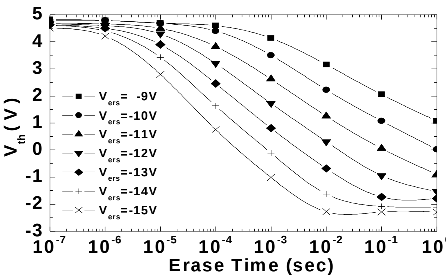


Fig.5. Erase characteristics of MONOS memory with 16nm AlN. The device was initially programmed at 13V for 100μs.

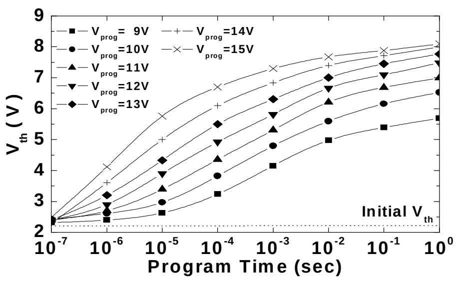


Fig.6. The measured program characteristics of MONOS with 12nm AlN.

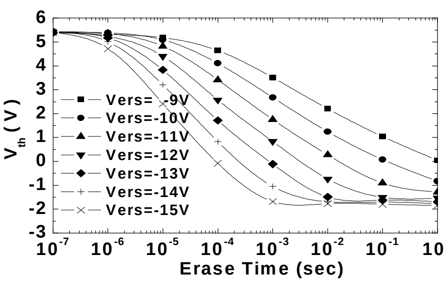


Fig.7. Erase characteristics of MONOS memory with 12nm AlN. The device was initially programmed at 13V for 100μs.

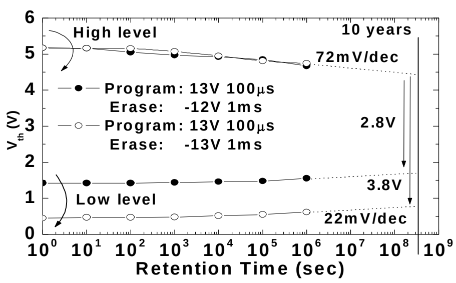
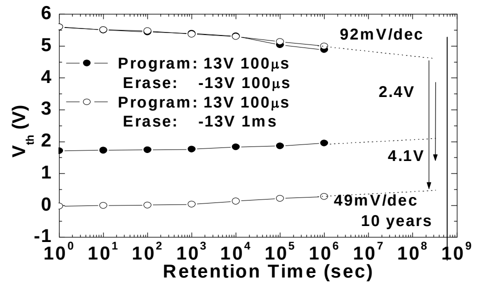


Fig.8. Retention of MONOS devices with 16nm AlN at 25℃. The P/E decay rates are only 72/22 mV/dec.



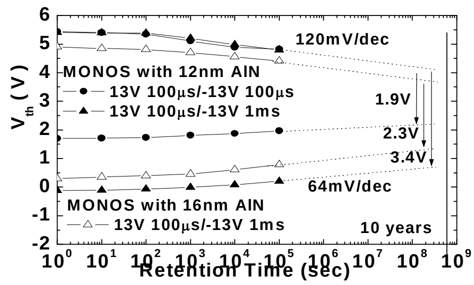
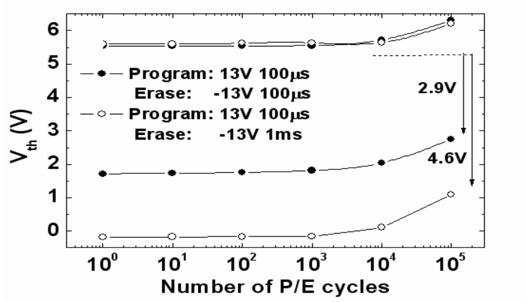


Fig.9. Retention of MONOS devices with 12nm AlN at 25℃ The P/E decay rates are 92/49 mV/dec.

Fig.10. Retention of MONOS devices with 12nm and 16nm AlN at 85℃. The P/E decay rates are 120/64 mV/dec.



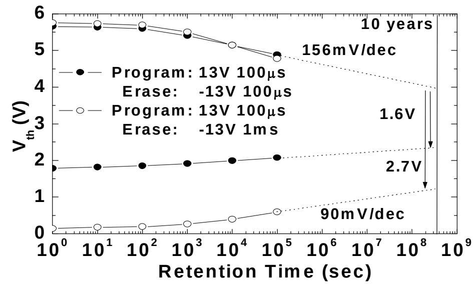


Fig.11. Endurance of MONOS memory with 12nm AlN at 85℃. High ΔVth can be maintain up to 10^5 P/E.

Fig.12. Retention of 10k P/E-cycled MONOS devices with 12nm AlN at 85℃. Large ΔVth of 1.6 and 2.7V are still obtained.

	P/E condition for retention & cycling	Initial ΔVth (V) @85℃	ΔVth (V) for 10-year retention @85℃	85℃-P/E decay rate (mV/dec)	ΔVth @Cycles & 85℃	ΔVth (V) for 10-year after 10k cycles @ 85℃
This Work	**13V 100μs/ -13V 100μs**	**3.7**	**1.9**	**120 / 52**	**2.9 @ 10^5**	**1.6**
	13V 100μs/ -13V 1ms	**5.5**	**3.4**	**120 / 64**	**4.6 @ 10^5**	**2.7**
Tri-gate [1] $SiO_2/Si_3N_4/SiO_2$/poly	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25℃ only)	12.5 /12.5 (@25℃ only)	1.5 @ 10^4 (@25℃)	No data
FinFET [2] $SiO_2/Si_3N_4/SiO_2$	13V 10μs/ -12V 1ms	5	2.9	60 / 150	4.2 @ 10^4	No data
SiO_2/Si_3N_4/ Al_2O_3/TaN [3]	13.5V 100μs/ -13V 10ms	4.4	2.07	140 / 75	4 @ 10^5	1.36
SiO_2/Al_2O/ SiO_2/poly [4]	9V >1ms/ no data	0.9	0.9	No charge loss	No data	No data

Table.1. Comparisons of P/E speed, ΔVth window (extrapolated for 85℃ 10-years retention), retention decay rate and endurance.