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次100奈米SOI CMOS的RF/Analog特性分析與模式建立(II)

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次 100 奈米 SOI CMOS 的 RF/Analog 特性分析與模式建立 (II)
RF/Analog Modeling and Characterization of Scaled SOI CMOS (II)

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一、中文摘要

在本計畫中我們對次 100 奈米 SOI CMOS 的 RF/analog 特性作深入研究與模式建立。利用我們早先完成的統整 SOI 低頻元件模型為基礎，我們在本計畫中所發展的 RF SOI 元件模型將有益於 RF 電路模擬以及 SOI CMOS 在 SOC 的應用。在本計畫中我們對於前瞻 SOI 元件在高頻時的閘極漏電流、閘極電阻、基極電阻以及浮動基體等效應的實驗分析與探討，也有助於使用數位 SOI CMOS 技術的 RF/analog 元件設計的最佳化。

關鍵詞：
RF/analog ； SOI CMOS ； SOC ； 元件設計；電路模擬；實驗分析與模式

Abstract

In this project we investigate sub-100-nm SOI CMOS with emphasis on RF/analog characteristics. Using our previously established unified SOI model as the low frequency core, our developed RF SOI SPICE model will enable RF circuit design and facilitate SOI CMOS for SOC applications. Our physical characterization and modeling including gate tunneling, gate input resistance, substrate resistance and floating body effects for scaled SOI CMOS operated at high frequency will also enhance the device design of digital SOI CMOS technology for RF/analog applications.

Keywords :
RF/analog, SOI CMOS, SOC, device design, circuit simulation, characterization and modeling

二、計畫緣由及目的

The growing demand of mobility and the rapid progress in the wireless industry make the ubiquitous connection possible in today's world. In the past, the Radio Frequency (RF) market was dominated by GaAs or silicon bipolar technology due to their high speed. However, the continual scaling of CMOS technology has raised the cutoff frequency of the deep-submicron MOSFET significantly and made this technology sufficient to build GHz RF circuit blocks. The main advantage of CMOS technology for wireless communication is the integration of RF and analog functionality into the advanced digital CMOS technology to yield the cost-effective System-On-Chip (SOC) solution.

With the scaling of CMOS, SOI (Silicon-On-Insulator) CMOS is emerging as an important IC technology due to the following four technological trends: (1) *High performance*. SOI provides a performance gain of 20 to 35 percent over bulk CMOS [1] due to the reduction of junction capacitance and the absence of the body-bias effect in series connected devices, e.g. in NAND and NOR gates. (2) *Low power*. With the same performance SOI can operate at a lower voltage and therefore lower power. Notice that the primary measures of analog performance such as G_m/I_d, f_T and f_{max} also improve at a low supply voltage. (3) *Process simplicity.* SOI may reduce some future bulk-technology's manufacturing difficulties such

as isolation, shallow junction, and latchup sensitivity. (4) *Mixed Technologies.* SOI devices have good immunity to substrate noise due to the isolation provided by the buried oxide layer and to the high-resistivity substrate, which also improves the performance of passive elements such as high-Q inductors and transmission lines commonly used in analog and RF circuits. It may also be useful to embedded DRAM because of good signal isolation from the logic circuit blocks.

Therefore, besides the high performance microprocessor and low power logic, SOI offers advantages over the bulk silicon to realize an SOC by integrating high-performance digital and analog/RF circuits. As a matter of fact, the SOI CMOS technology with f_{max} up to 100 GHz has penetrated into the RF SOC applications [2-3].

However, the main barrier to full exploitation of SOI CMOS performance is that the design of an SOI chip is a relatively risky process because a relative lacking of design experience makes it difficult to achieve fast turnaround and high probability of first-pass success. To surmount this barrier, a robust and physically accurate SPICE (compact) model is needed. SPICE modeling is the standard approach for precise design of standard cell libraries and critical-path sub-circuits in all large systems, as well as the basis for computing the look-up tables used in higher-level timing simulators. IP blocks are in turn designed using the speedier simulations. The existing SOI SPICE models [4-6] are inadequate for GHz frequency operation since they were initially developed for low-frequency applications and mainly focused on DC and transient behavior. The parasitic components ignored at low frequency become very important for predicting device performance at high frequency.

Therefore, we propose to conduct research on RF/analog characterization and modeling for scaled SOI CMOS. In this project, state-of-the-art SOI MOSFETs will be characterized by DC, AC and S-parameter measurements. A new model which considers gate tunneling, gate input resistance, body/substrate resistance and floating body effects for scaled SOI CMOS operated at high frequency will be developed. Our investigation will further enhance the device design of digital SOI CMOS technology for RF/analog applications. The developed SPICE model will also facilitate RF/analog circuit simulation/design using advanced SOI CMOS.

三、研究方法

Since the device behavior is continuous as the frequency goes from low to high, a physically accurate SOI SPICE model at low frequency is crucial to compact RF SOI modeling. For sub-100-nm SOI CMOS [7], the modeling challenge at low frequency lies in the fact that an SOI model continuously spanning PD (Partial-Depletion) and FD (Full-Depletion) is required due to the following considerations. (1) The need for multiple V_T/T_{OX} transistors for low active/standby power requirement in a single chip may result in the coexistence of both PD and FD devices in the same circuit by design. (2) The laterally non-uniform channel doping (halo/pocket implant) may lead to PD nominal devices and FD long-channel devices with continuous variations in between. (3) The influence of the gate field may encroach from the isolation edges and result in FD narrow-width devices. (4) The coexistence of PD and FD behaviors in a single device, depending on bias conditions.

In our previous NSC project [8], we have used the concept of body-source built-in potential lowering (ΔV_{bi}) [10] to solve the problem of the coexistence of PD/FD devices in a single chip as well as the coexistence of PD/FD behavior in a single device for scaled SOI CMOS [22-23]. In this project, we will use this unified model as our low frequency

core and further extend this model in the AC and high frequency regime.

Since the self-biasing of SOI floating body may impact the transistor current gain (h_{21}), unilateral gain (U) and the cutoff frequency, it is crucial to investigate/solve the following floating-body related issues for the RF/analog modeling of sub-100-nm SOI CMOS. (1) The measurement of ΔV_{bi} [10] becomes difficult with the SOI-thickness scaling because of the reduction of the efficiency of body contacts. To extract ΔV_{bi} for floating-body SOI devices without body contacts, we have proposed a methodology based on the correlation between ΔV_{bi} and threshold voltage (V_T) [21]. (2) The gate-body-tunneling induced floating-body effect [24] becomes significant with the oxide-thickness scaling and is responsible for the second peak present in the G_m-V_{GS} characteristics [9] as well as the frequency dependence of G_m [9]. Moreover, it induces excess shot noise in the low-frequency noise spectrum [9], which is an important figure of merit for analog circuits because it may impact the jitter of VCOs and the charge pump of PLLs [11].

For extremely scaled SOI CMOS, multiple-gate device has been widely proposed [12-13]. The sizes of state-of-the-art multiple-gate devices can be well below 50nm in all of the three dimensions. For devices with geometries so small, mesoscopic effects may be present. Reference 14-18 demonstrated that conductance oscillations can occur in small devices with novel test structures or at very low temperature. For advanced CMOS transistors under room temperature, however, this phenomenon has rarely been investigated. In this project, we have investigated the phenomenon of transconductance (G_m) oscillations in advanced multiple-gate FinFET SOI transistors with 1.6nm gate oxide near room temperature. The results of our investigation have been published in [19,36].

Gate input capacitance is one important figure of merit for high-frequency analog transistor performance. As the gate dielectric thickness is reduced and gate tunneling current increases, the measurement of gate capacitance becomes difficult due to the attenuated capacitance caused by the coexistence of inductance, series resistance and gate tunneling current in MOS test structures [20]. Although several models have been proposed to capture the measured C-V characteristics, they are not physically accurate enough to provide satisfactory scalability. In this project, we have investigated the anomalous C-V behavior for MOSFETs with ultra-thin gate oxide and proposed an intrinsic input resistance approach [37] to reconstruct the inversion C-V characteristics. The results of our investigation will be detailed in this report.

The substrate network is important for RF application because the substrate resistance will degrade output resistance as the impedance of the drain junction capacitance drops at high frequency. A wide range of topologies of substrate network has been proposed in the RF CMOS modeling. For scaled SOI CMOS with quasi-neutral body (i.e., PD), the body resistance together with the junction capacitance provides a shunt branch from the output to ground. In this project, we have developed an analytical small signal model for RF SOI MOSFETs by considering the neutral-body network and the body trans-conductance. This model predicts the occurrence of abnormal behaviors in output characteristics, which has been verified by our s-parameter measurements. We have demonstrated that an adequate consideration for the coupling path between the source and drain terminals through the quasi-neutral body region, as well as the modulation of body-to-source potential through this additional current path are crucial to RF SOI modeling. The results of our investigation will be detailed in this report.

四、結果與討論

1. Modeling the Anomalous S-Parameter Characteristics in RF SOI MOSFETs

The RF SOI MOSFETs used in this study were fabricated using state-of-the-art SOI technology. The thicknesses for gate oxide, SOI layer and buried oxide are 1.4nm, 40nm and 200nm, respectively. The presence of kinks in Fig. 1 shows that the devices under study are partially depleted (PD).

On-wafer 2-port *S* parameters up to 6 GHz were measured, and then de-embedded with open dummy. Afterwards, the source/drain series resistances can be extracted using the method described in [29] and then be de-embedded to get the intrinsic *Y* parameters of the device under test [28].

Fig. 2 shows the cross-sectional view of a PD SOI MOSFET. The corresponding intrinsic small signal equivalent circuit is depicted in Fig. 3(a), where the neutral-body parasitic is represented by a series combination of two junction capacitances, $C_{j,bs}$ and $C_{j,bd}$, and a body resistance R_b along with the body trans-conductance g_{mb}. In the conventional model (Fig. 3(b)) used for bulk MOSFETs, the body is usually out-connected to the signal ground, and hence the neutral-body effect is eliminated. For PD SOI MOSFETs with floating body, however, these neutral-body related components have to be considered.

Comparing Fig. 3(a) with Fig. 3(b), we can find that the major impact of the neutral-body effect is the output admittance Y_{ds}. The expressions of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ for these two models have been derived and shown in Eq. (2), (3), (6) and (7). It can be seen that Eq. (2) and (3) will be identical to Eq. (6) and (7), respectively, as R_b approaches infinity (i.e., full depletion). For PD SOI, however, $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ become frequency dependent due to the neutral-body effect. Table 1 lists their low and high frequency limits. One can find that if we neglect the significant low frequency dependence caused by the neutral-body effect, the output conductance extracted from $Re(Y_{ds})$ at high frequency will no longer be $1/R_{ds}$. This also explains the abnormal phenomenon observed in [33].

Figure 4 shows the expressions of the first derivative of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ with respect to the angular frequency (Eq. (4) and (5)). They represent the slopes of the curves for $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ versus frequency. Based on these expressions, we can find that the sign of these slopes is governed by the criteria summarized in Table 2.

The modeling results of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ for two different bias condition **A** (V_{DS} = 1.2V and V_{GS} = 0.4V) and **B** (V_{DS} = 1.2V and V_{GS} = 1.2V) are shown in Fig. 5. The slopes of these curves in condition **A** and **B** meet the criterion **I** and **II** defined in Table 2, respectively, and both can be modeled by our derived Eq. (2) and (3).

Figures 6 and 7 show the modeling results of *S* parameters with and without considering the neutral-body effect. Both S_{22} and S_{21} show abnormal low frequency behaviors and only the proposed model can capture these phenomena. It is worth noting that the criterion **I** and **II** can explain the abnormal inductance-like and kink behaviors in S_{22}, respectively.

The extracted body trans-conductance, junction capacitances and body resistance versus gate bias are shown in Fig. 8, 9 and 10, respectively. All these components show significant influence compared to the intrinsic ones and will play an important role in the characterization, analysis and modeling of RF SOI MOSFETs.

2. Inversion C-V Reconstruction for MOSFETs with Leaky Dielectrics using Intrinsic Input Resistance Approach [37]

As the gate dielectric thickness is reduced (below 20 Å), the inversion C-V characteristic is distorted due to direct tunneling current. Although Goo *et al*. [25] demonstrated that the conventional two-element parallel model (Fig. 11(a)) can provide valid C-V characteristics for short-channel devices (e.g., below 0.2 μm [25]), using these devices in C-V measurement has several drawbacks such as small intrinsic capacitance, large parasitic components (Fig. 12) and uncertainty in the physical gate length. In other words, the variation of measured C-V increases as channel length decreases (Fig. 13). Therefore, the C-V reconstruction for long-channel MOSFETs is still a crucial issue.

Several studies have constructed the C-V characteristic for long-channel devices using distributed circuit approaches [20,26-27]. For example, Barlage *et al*. [26] proposed using a transmission line concept to extract the inversion MOS capacitance. In [20] we employed segmented SPICE simulation (Fig. 14(a)) with each sub-transistor modeled by the BSIM4 MOSFET model to simulate the anomalous C-V characteristics due to gate direct tunneling (Fig. 14(b) and (c)). Although these methods may provide well-restored characteristics, the implementation is too complicated to be routinely used in a technology development.

To develop a simple method for the inversion C-V reconstruction, the challenge lies in capturing the distributed nature of the gate capacitance and the channel resistance in a compact way. This is analogous to the gate input impedance modeling in the compact model development for RF CMOS, where an intrinsic input resistance has been introduced [30] as a major part of the gate input resistance. Here we present an inversion C-V reconstruction method for long-channel MOSFETs using the concept of intrinsic input resistance.

Fig. 15(a) shows BSIM4/SPICE-simulated C-V characteristics for devices with leaky dielectric. Segmented SPICE simulation that divides the transistor along the length direction with 10 sub-transistors in series (Fig. 15(b)) was utilized and the BSIM4 device model parameters were well calibrated as described in [20]. As shown in Fig. 15(a), a substantial attenuation in the inversion capacitance for long-channel MOSFETs can be seen. The attenuation results mainly from the gate tunneling induced de-biasing effect. Also shown in Fig. 15(a) is that a single transistor simulation with an intrinsic input resistance, R_{ii}, added to the gate terminal in addition to gate electrode resistance (Fig. 15(c)) yields nearly identical results as those of segmented simulation.

R_{ii} represents a channel-reflected gate resistance and can be thought of as an equivalent resistance accounting for the first-order non-quasi-static effect in the channel [30-31]. R_{ii} is proportional to the total channel resistance with a proportional constant α, which accounts for the distributed effect of the complex RC network constructed by the gate capacitance and the channel resistance. Since this RC network has a short termination at both source and drain nodes in the C-V measurement, α can be approximated as 1/12 because the location at which the gate current equals zero occurs at L/2 [31]. The channel resistance has been modeled in BSIM4 [30-31] and may be extracted from the measured I-V (i.e., $(dI_{ds}/dV_{ds})^{-1}$). Fig. 16 shows that R_{ii} dominates the total gate resistance for the device with long channel length (L = 10 μm) and therefore is crucial in the C-V reconstruction of long-channel MOSFETs.

As indicated in Fig. 15(a), the concept of intrinsic input resistance can be used to develop a simple method for the inversion capacitance extraction. As the conventional three-element model (Fig. 11(b)) is used to

represent the small-signal equivalent model of a leaky MOS capacitor, the total series resistance, R_s, can be calculated by $R_{ii} + R_{ge} + R_{sd}/2$. The inversion C-V can then be reconstructed by [27,32]:

$$C_{OX} = C_m / ((1 - G_m R_s)^2 + \omega^2 C_m^2 R_s^2)$$

where C_m and G_m represent the measured capacitance and conductance, respectively, using the parallel circuit model of the LCR meter (Fig. 11(a)).

Standard MOSFETs with doped poly-Si gate electrode were fabricated and tested in this study. The EOT is about 11 Å. The impedance analyzer HP4294A was used in the C-V measurement. The measurement frequency is 1 MHz. Fig. 17(a) and Fig. 17(b) show the measured inversion capacitance and our reconstructed C-V characteristics for NMOS and PMOS, respectively. The impact of R_{ii} on the reconstructed results can be seen. Moreover, the correction for PMOS is larger because the lower PMOS channel mobility may result in a higher channel resistance and R_{ii}. Besides, the reconstructed C-V characteristics show a slight decrease in the high V_{GS} regime. This may be attributed to poly-depletion effects. Also shown in Fig. 17 are the theoretical characteristics provided by the NCSU CVC (C-V analysis software developed by the North Carolina State University) [34-35]. Our reconstructed C-V curves agree with the NCSU-CVC simulation results.

五、計畫成果自評

In this project, we have investigated sub-100-nm SOI CMOS with emphasis on RF/analog characteristics. Our investigation has included critical modeling issues regarding floating body effects [21], single-electron G_m oscillation in multiple-gate SOI [19,36], gate input capacitance extraction for ultra-thin oxide [20,37] and the body/substrate resistance effect for PD SOI MOSFETs operated at high frequency [29,38].

Our investigation will be instrumental in early anticipation of the potentials of digital SOI CMOS technology for RF/analog applications and enhancing the device design so as to effectively utilize the tremendous intrinsic speed resulting from further scaling of sub-100-nm SOI CMOS. The developed SPICE model and model parameter extraction procedure based on our investigation will enable early RF/analog circuit design and facilitate SOI CMOS for SOC applications.

The results of the project have been disseminated through research reports in international journals [21,36,38] and conferences [19-20,29,37] as well as used in education of our graduate students to become leading researchers in the areas of compact modeling, device design and circuit simulation for SOI CMOS.

六、參考文獻

[1] G. G. Shahidi et al., 1999 IEEE International Solid-State Circuits Conference, Feb. 1999, p. 426.
[2] J. Kim et al., IEEE 2004 Custom Integrated Circuits Conference, pp. 541-548.
[3] J.-O. Plouchart, IEEE 2003 SOI Conference.
[4] P. Su et al., IEEE 2000 Custom Integrated Circuits Conference, pp. 197-200.
[5] J. B. Kuo, Digest of HKEDM, June 2000.
[6] P. Su et al., IEEE 2003 Custom Integrated Circuits Conference, pp. 241-244.
[7] F.-L. Yang et al., IEDM Tech. Dig., Dec. 2003.
[8] P. Su, NSC 93-2215-E-009-029 成果報告, Oct. 2004.
[9] P. Su, NSC 93-2215-E-009-042 成果報告, Oct. 2005.
[10] P. Su et al., "On the body-source built-in potential lowering of SOI MOSFETs," IEEE EDL, vol. 24, no.2, pp. 90-92, February 2003.
[11] J. Kim et al., ISLPED, pp. 434-439, August 2003.
[12] Z. Krivokapic et al., SSDM (2003) p. 760.
[13] F.-L. Yang et al., SSDM (2004) p. 772.
[14] Y. Takahashi et al., IEEE TED, vol.43, no.8, 1996.
[15] Y. Omura et al., IEEE EDL, vol.18, no.5, 1997.
[16] M. G. Peters et al., JAP, vol.84, no.9, Nov. 1998.
[17] J. Scott-Thomas et al., Phys. Rev. Lett., vol.62, p.583, 1989.
[18] F.R. Waugh et al., Phys. Rev. Lett., vol.75, p.705, 1995.
[19] W. Lee, P. Su et al., 2005 ISDRS, Washington D.C., Dec. 2005.
[20] W. Lee, P. Su et al., "Inversion MOS capacitance extraction for ultra-thin gate oxide using BSIM4," Proc. 2005 VLSI-TSA, April 2005, p. 62.
[21] P. Su et al., "On the prediction of geometry-dependent floating-body effect in SOI MOSFETs," IEEE TED, vol.52, no.7, p. 1662, July 2005.
[22] P. Su et al., "Modeling geometry-dependent floating-body effect using body-source built-in potential lowering for scaled SOI CMOS," SSDM, Sep. 2004, pp. 510-511.
[23] P. Su et al., "Modeling geometry-dependent floating-body effect using body-source built-in potential lowering for SOI circuit simulation," Jpn. J. Appl. Phys., vol. 44, no. 4B, p. 2366, April 2005.
[24] P. Su et al., "Studying the impact of gate tunneling on dynamic behaviors of partially-depleted SOI CMOS using BSIMPD," Proc. 2002 ISQED, San Jose, CA, March 2002, pp. 487-491.
[25] J.-S. Goo et al., IEEE EDL, 25(12), 2004.
[26] D. W. Barlag et al., IEEE EDL, 21(9), 2000.
[27] C.-H. Choi et al., IEEE TED, 47(10), 2000.
[28] D. Lovelace et al., IEEE MTT-S International Microwave Symp. Digest, pp. 865-866, 1994.
[29] S.-C. Wang, P. Su et al., "RF extrinsic resistance extraction considering neutral-body effect for partially-depleted SOI MOSFETs," Proc. 2006 VLSI-TSA, April 2006, p. 139.
[30] X. Jin et al., IEDM, 1998.
[31] W. Liu, "MOSFET models for SPICE simulation including BSIM3v3 and BSIM4", John Wiley & Sons, 2001.
[32] E. M. Vogel et al., IEEE TED, 47(3), 2000.
[33] C. L. Chen et al., IEEE EDL, vol.21, pp. 497–499, Oct. 2000.
[34] J. R. Hauser et al., Proc. AIP Int. Conf. Characterization Metrology ULSI Technology, Gaithersburg, MD, 1998.
[35] W. K. Henson et al. IEEE EDL, 20(4), 1999.
[36] W. Lee, P. Su et al., "An assessment of single-electron effects in multiple-gate SOI MOSFETs with 1.6-nm gate oxide near room temperature," IEEE EDL, vol.27, no.3, pp. 182-184, March 2006.
[37] W. Lee, P. Su et al., "Investigation of inversion C-V reconstruction for long-channel MOSFETs with leaky dielectrics using intrinsic input resistance approach," 2006 SSDM, Yokohama, Japan, Sep. 2006, p. 416.
[38] S.-C. Wang, P. Su et al., "Neutral-body effect on the output characteristics of RF SOI MOSFETs," submitted to IEEE EDL.

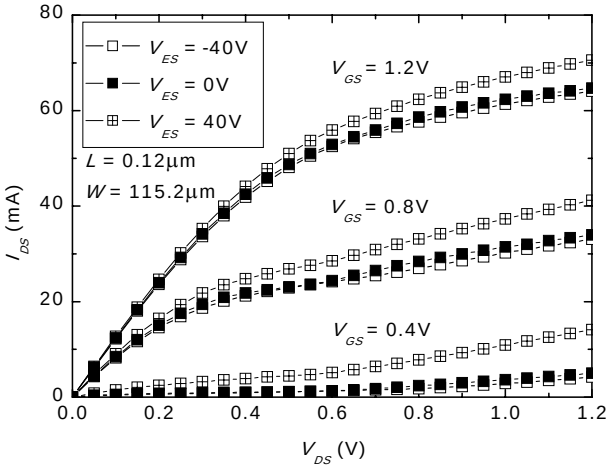


Fig. 1. I_{DS} versus V_{DS} curves for the RF SOI MOSFET used in this study with different V_{GS} and V_{ES} (backgate bias).

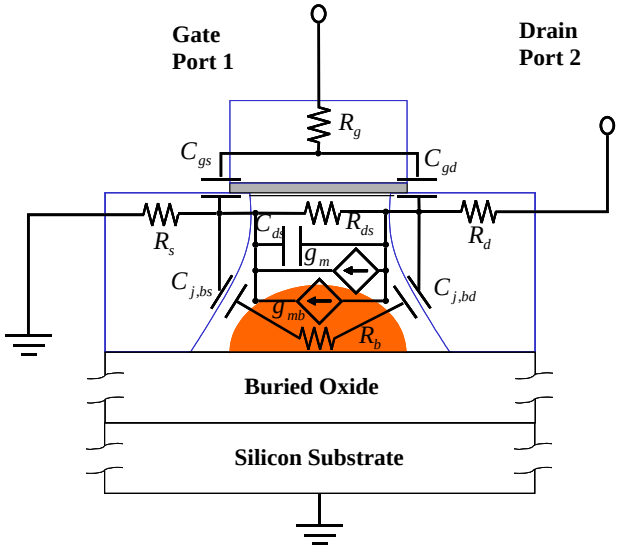


Fig. 2. Cross-sectional view of a PD SOI MOSFET

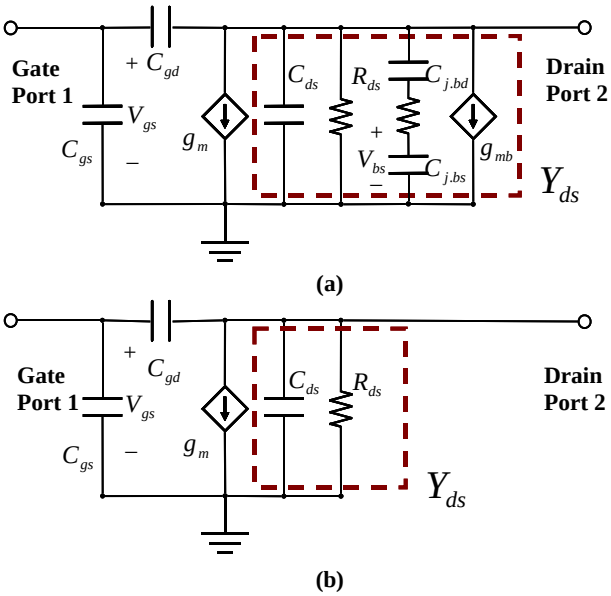


Fig. 3. Equivalent circuits for (a) an SOI MOSFET with the neutral-body effect and (b) a bulk MOSFET without considering this effect. Dotted boxes are used to define the output admittance Y_{ds}.

$$Y_{ds} = Y_{21} - Y_{12} \tag{1}$$

$$\mathrm{Re}(Y_{ds}) = \frac{1}{R_{ds}} \times \left[\left(C_{j,bd} + C_{j,bs}\right)^2 + \omega^2 C_{j,bs}^2 C_{j,bd}^2 R_b \left(R_b + R_{ds}\right) + g_{mb} C_{j,bd} R_{ds} \left(C_{j,bs} + C_{j,bd}\right) \right] \Big/ \left[\left(C_{j,bd} + C_{j,bs}\right)^2 + \omega^2 C_{j,bs}^2 C_{j,bd}^2 R_b^2 \right] \tag{2}$$

$$\frac{\mathrm{Im}(Y_{ds})}{\omega} = \left[C_{ds} \left(C_{j,bd} + C_{j,bs}\right)^2 + C_{j,bs} C_{j,bd} \left(C_{j,bd} + C_{j,bs} - g_{mb} C_{j,bd} R_b + \omega^2 C_{ds} C_{j,bs} C_{j,bd} R_b^2 \right) \right] \Big/ \left[\left(C_{j,bd} + C_{j,bs}\right)^2 + \omega^2 C_{j,bs}^2 C_{j,bd}^2 R_b^2 \right] \tag{3}$$

$$\frac{\partial \mathrm{Re}(Y_{ds})}{\partial \omega} = 2\omega C_{j,bs}^2 C_{j,bd}^2 R_b \left(C_{j,bs} + C_{j,bd}\right) \left(C_{j,bs} + C_{j,bd} - g_{mb} C_{j,bd} R_b\right) \Big/ \left[\left(C_{j,bd} + C_{j,bs}\right)^2 + \omega^2 C_{j,bs}^2 C_{j,bd}^2 R_b^2 \right]^2 \tag{4}$$

$$\frac{\partial \left(\mathrm{Im}(Y_{ds})/\omega\right)}{\partial \omega} = -2\omega C_{j,bs}^3 C_{j,bd}^3 R_b^2 \left(C_{j,bs} + C_{j,bd} - g_{mb} C_{j,bd} R_b\right) \Big/ \left[\left(C_{j,bd} + C_{j,bs}\right)^2 + \omega^2 C_{j,bs}^2 C_{j,bd}^2 R_b^2 \right]^2 \tag{5}$$

$$\mathrm{Re}(Y_{ds}) = \frac{1}{R_{ds}} \text{ (for the conventional model)} \tag{6}$$

$$\frac{\mathrm{Im}(Y_{ds})}{\omega} = C_{ds} \text{ (for the conventional model)} \tag{7}$$

Fig. 4. Expressions of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ and their first derivatives with respect to frequency for the proposed SOI model (Eq. (2)-(5)) and the conventional one (Eq. (6)-(7)).

Table 1. Low and high frequency limits of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ for the proposed SOI model

	Low frequency limit	**High frequency limit**
$\mathrm{Re}(Y_{ds})$	$\frac{1}{R_{ds}} + g_{mb} \frac{C_{j,bd}}{C_{j,bs} + C_{j,bd}}$	$\frac{1}{R_{ds}} + \frac{1}{R_b}$
$\frac{\mathrm{Im}(Y_{ds})}{\omega}$	$C_{ds} + \frac{C_{j,bs} C_{j,bd}}{C_{j,bs} + C_{j,bd}} - g_{mb} R_b \frac{C_{j,bs} C_{j,bd}^2}{\left(C_{j,bs} + C_{j,bd}\right)^2}$	C_{ds}

Table 2. The criteria governing the sign of the first derivatives of $Re(Y_{ds})$ and $Im(Y_{ds})/\omega$ with respect to frequency

	Criterion I $H_{gmb} R_b C_{bd} > C_{bd} + C_{bs}$	**Criterion II** $H_{gmb} R_b C_{bd} < C_{bd} + C_{bs}$
$\frac{\partial \mathrm{Re}(Y_{ds})}{\partial \omega}$	< 0	> 0
$\frac{\partial \left(\mathrm{Im}(Y_{ds})/\omega\right)}{\partial \omega}$	> 0	< 0

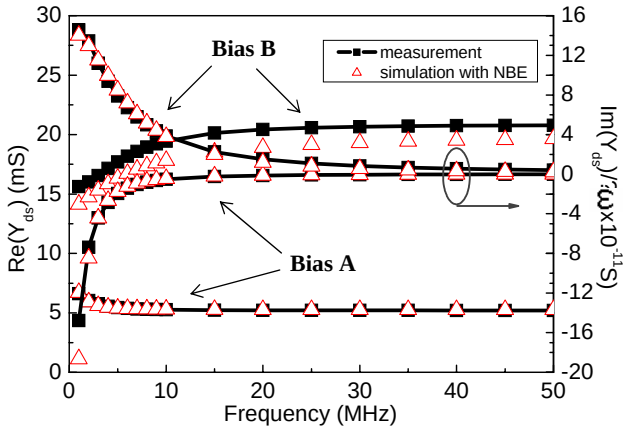


Fig. 5. Modeling results of Y_{ds} with considering the neutral-body effect (NBE) for two different bias condition – Bias **A** (V_{DS} = 1.2V and V_{GS} = 0.4V) and Bias **B** (V_{DS} = 1.2V and V_{GS} = 1.2V)

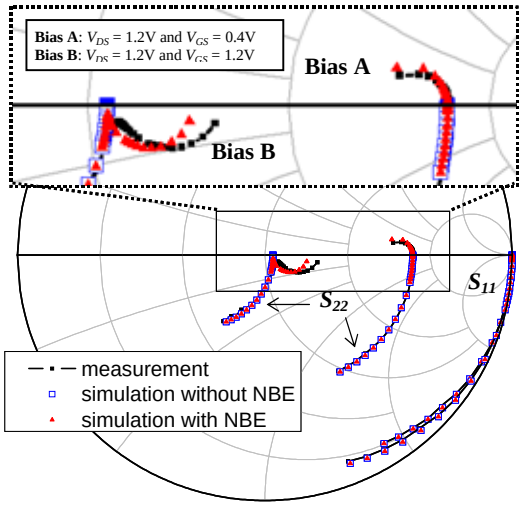


Fig. 6. Modeling results of S_{11} and S_{22} with and without considering the neutral-body effect. Only the proposed model taking NBE into account can capture the abnormal S_{22} behaviors.

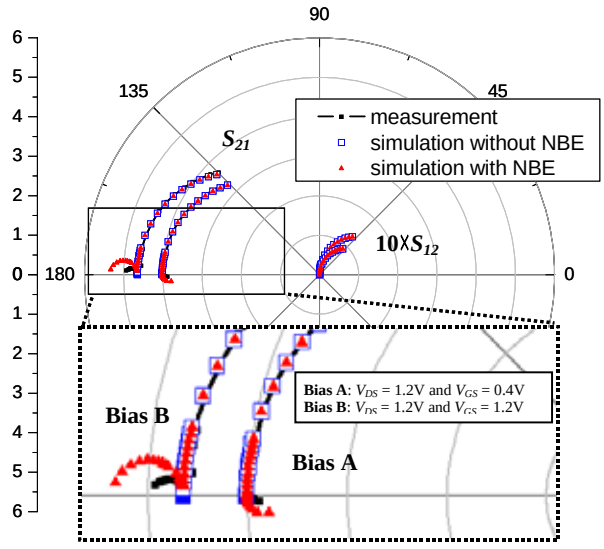


Fig. 7. Modeling results of S_{12} and S_{21} with and without considering the neutral-body effect. Only the proposed model taking NBE into account can capture the abnormal S_{21} behaviors.

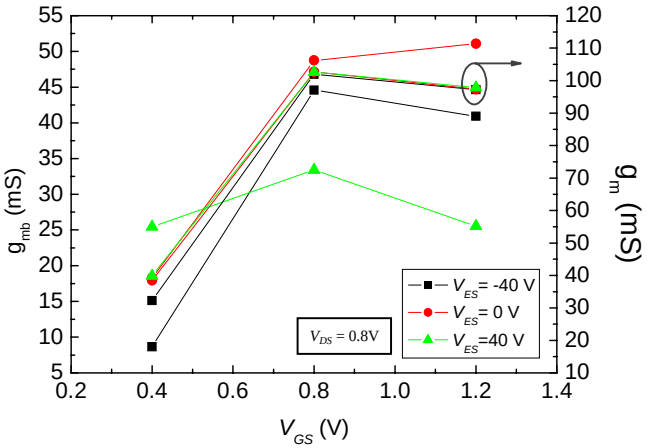


Fig. 8. The extracted values of g_{mb} and g_m for the bias conditions with V_{DS} = 0.8V and different V_{GS} and V_{ES}.

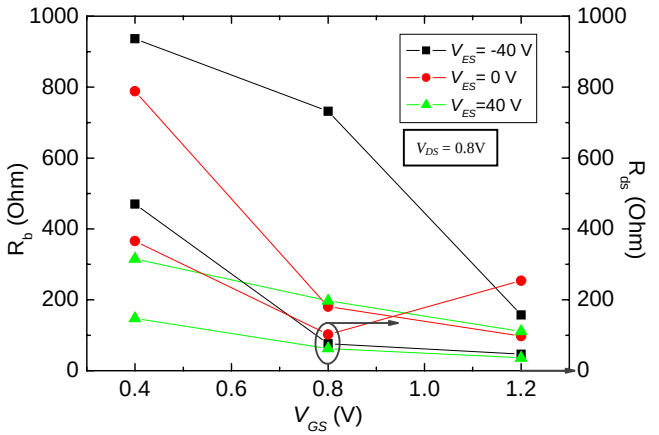


Fig. 9. The extracted values for R_b and R_{ds} for the bias conditions with V_{DS} = 0.8V and different V_{GS} and V_{ES}.

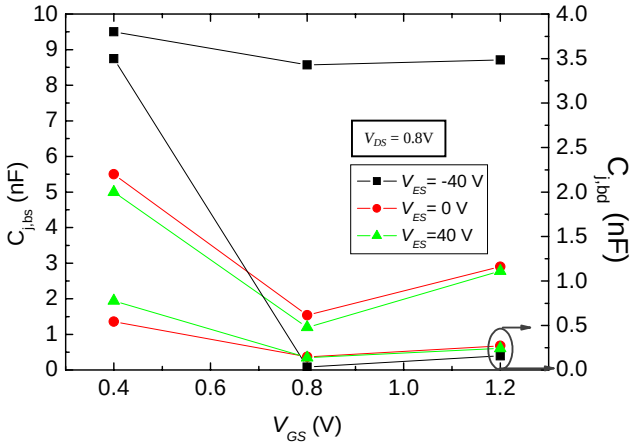


Fig. 10. The extracted values for $C_{j,bs}$ and $C_{j,bd}$ for the bias conditions with V_{DS} = 0.8V and different V_{GS} and V_{ES}.

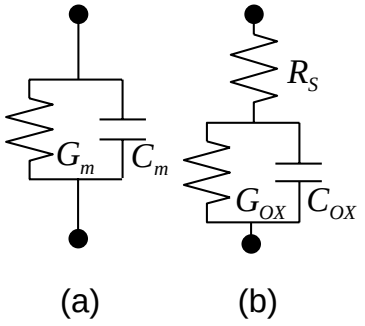


Fig. 11. Small-signal equivalent models for MOS capacitor. (a) Two-element parallel model. (b) Three-element model.

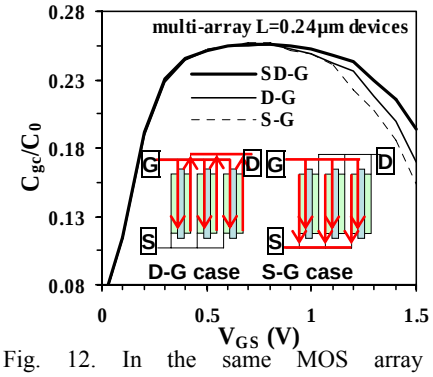


Fig. 12. In the same MOS array of short-channel devices, the impact of on-chip inductance (L_i) depends on the measurement configuration. C_{gc} : inversion capacitance. C_0 : true capacitance for L = 10 μm.

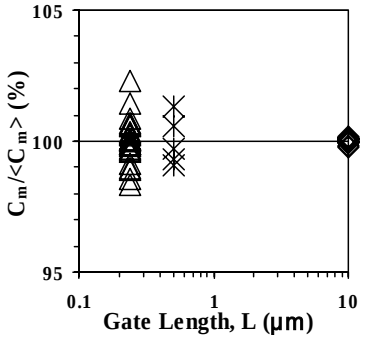
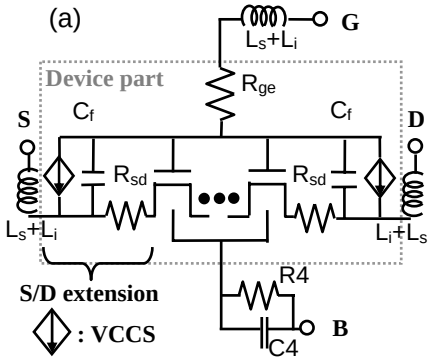
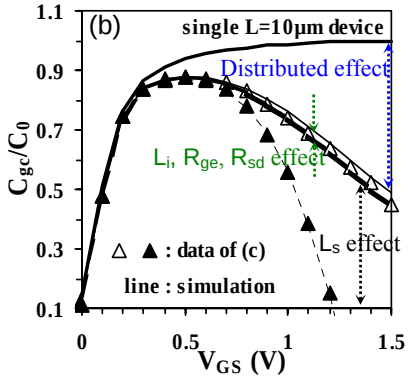


Fig. 13. The variation of C_m increases as L decreases. C_m : measured capacitance.





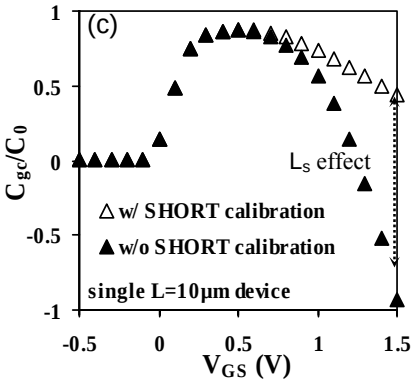
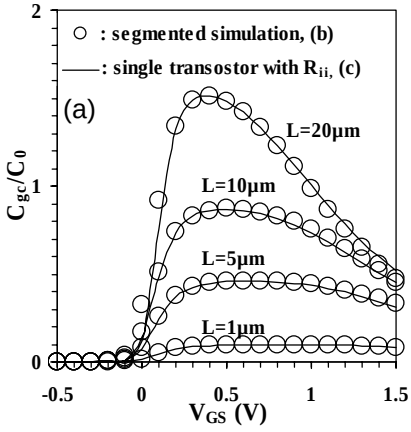


Fig. 14. BSIM4-based macro model to simulate the anomalous C-V characteristics caused by gate direct tunneling. R_{ge} : gate electrode resistance. R_{sd} : source/drain resistance. L_s : cable inductance. C_f : fringing capacitance. R4 = 1e9 Ω, C4 = 1e-9 F.



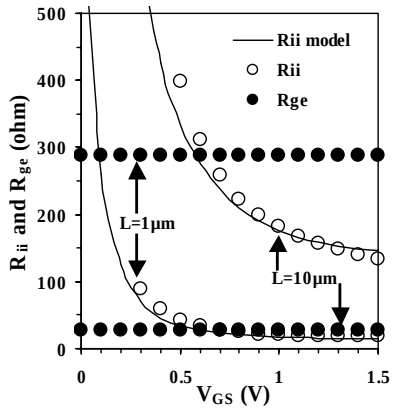


Fig. 16. R_{ii} and R_{ge} versus V_{GS} for devices with L = 1 μm and 10 μm. (Symbols : extracted date. Lines : model)

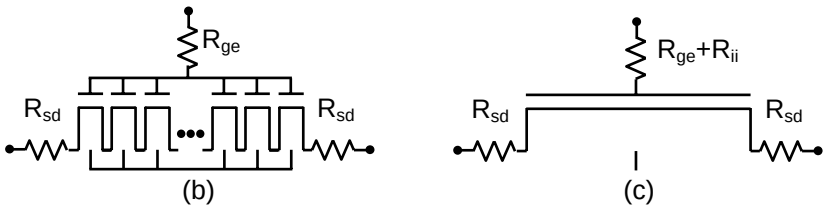
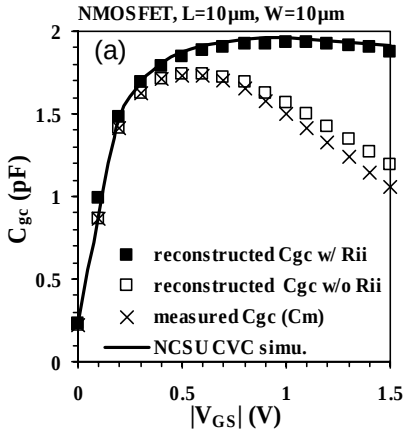


Fig. 15. (a) The gate-tunneling induced C-V attenuation can be simulated by BSIM4/SPICE simulation. (b) Segmented SPICE simulation with each sub-transistor modeled by the BSIM4 MOSFET model. (c) Single transistor SPICE simulation with R_{ii} added to the gate terminal in addition to R_{ge}. R_{ge} : gate electrode resistance.



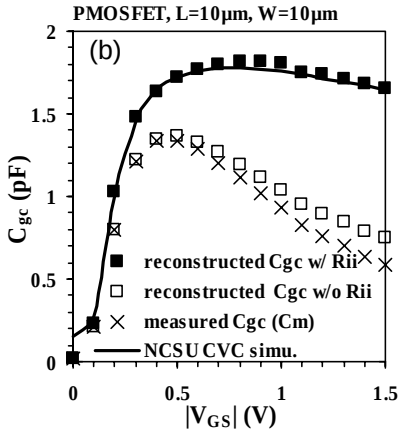


Fig. 17. Reconstructed C-V characteristics for (a) NMOS and (b) PMOS with and without considering R_{ii}. The results agree well with the simulation results of NCSU CVC. (T_{OX} = 1.15 nm. NMOS : N_{Bulk} = 3E17 cm^{-3}, N_{Gate} = 1.8E20 cm^{-3}. PMOS : N_{Bulk} = 2.5E17 cm^{-3}, N_{Gate} = 8.5E19 cm^{-3}.)