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Fabrication of High-Sensitivity Polycrystalline Silicon Nanowire Field-Effect Transistor pH Sensor Using Conventional Complementary Metal–Oxide–Semiconductor Technology

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High-sensitivity polycrystalline silicon (poly-Si) nanowire field-effect transistor (NW FET) pH sensors using top-down and self-aligned fabrication approaches involving the conventional complementary metal–oxide–semiconductor (CMOS) process are reported. For the top-down NW FET, the shrinkage due to reoxidation enables the nanowire width to be scaled to 40 nm without requiring the use of extra lithography equipment, and this improves the electrical uniformity and the performance of the sensors. The surface-ionic coupling operation of this buried-channel field-effect sensor exhibits superior pH sensitivity (threshold voltage shift > 100 mV/pH) as compared to the surface-channel ion-sensitive FET (ISFET). In addition, we report a novel method for fabricating self-aligned, vertical-channel, poly-Si nanowire sensors. The resulting 65-nm self-aligned vertical-channel poly-Si device was found to be feasible for independent-gate bias control, thus enabling its possible integration in very-large-scale integration (VLSI) circuits. Both the abovementioned approaches enable the manufacture of nanowire devices on a large-scale integrated (LSI) circuit using only CMOS manufacturing processes; this provides a high sensitivity, compact and cost-efficient biosensor systems-on-a-chip application. © 2011 The Japan Society of Applied Physics

1. Introduction

Biodetection devices prepared using complementary metal–oxide–semiconductor (CMOS)-compatible manufacturing technologies are likely to be very useful in healthcare applications.[1–3] Research into exploring biosensing functionality using CMOS-compatible devices is evolving, taking advantage of state-of-the-art CMOS technologies, including scaling of the feature sizes of devices, mature fabrication techniques, and precise process control. Among the most promising vehicles for unlabeled, real-time, high-sensitivity electrochemical detection, Si nanowire (SiNW)-based devices are one of the most promising devices because they have widths and heights similar to the dimensions of biomolecular species. The excellent electrical characteristics and biosensing functionalities of these systems were originally demonstrated using single-crystalline SiNWs fabricated using the bottom-up approach.[4] In recent years, SiNW field-effect transistors (FETs) fabricated using CMOS-compatible, top-down approaches on Silicon-On-Insulator (SOI) substrates have been used for high-sensitivity detection of biomolecular species.[5–7] To further reduce the manufacturing cost, a manufacture-friendly nanowire fabrication process, in which polycrystalline silicon (poly-Si) was used as a channel material, was recently developed for the detection of pathogenic avian influenza DNA and avidin/streptavidin.[8–10] Nevertheless, all of the abovementioned NW fabrication methods are difficult to implement in conjunction with commercialized, low-cost Si CMOS processing. In this paper, we report two simple processes for integrating poly-Si NWs into the CMOS process. Using these approaches along with the CMOS production technology, both the number of process steps and the chip size of the integrated sensor system can be reduced significantly; this in turn will provide cost-efficient, highly integrated devices for potential healthcare applications.

2. Experimental Methods

2.1 Fabrication of planar channel poly-Si NW

Figure 1 shows the process flow of the fabrication of poly-Si nanowire (PSNW) FETs on a planar channel. A 35-nm-thick oxide layer was grown at 900 °C by thermal oxidation and a 45-nm-thick SiN layer was deposited at 780 °C by low-pressure chemical vapor deposition (LPCVD) following which an approximately 1.5-nm-thick layer was grown by thermal oxidation at 900 °C on the Si substrate as the bottom dielectric layer of the device. For the semiconductor channel layer, a 50-nm-thick amorphous-Si layer was deposited using LPCVD at 550 °C. Next, annealing was performed at 600 °C in N_2 ambient for 12 h to convert the amorphous-Si into poly-Si as the device material. After carrying out I-line lithography, the wafer underwent photoresistor trimming followed by Si etching in a plasma etcher system to form a slender channel and a source/drain pad region on the bottom dielectric layer. To further trim the dimension of the PSNW, a 20-nm-thick thermal oxidation was carried out at 900 °C followed by oxide removal. An approximate 40 nm PSNW width reduction can be obtained after the reoxidation and oxide stripping process. Figure 2 shows the scanning electron microscopy (SEM) images of the PSNW; the line edge roughness of the PSNW is preserved during the two-step trimming process and the nanowire width can be directly scaled to around 40 nm as determined by the transmission electron microscopy (TEM) analysis. Subsequently, a channel protection photoresistor was used to define the intrinsic poly-Si channel region to increase PSNW sensitivity;[11] in addition, the n+ source/drain (S/D) region was implanted to reduce the resistance of the contact pad. Finally, the channel protection photoresist was removed and the S/D dopant was activated by annealing at 600 °C for 30 min.

2.2 Fabrication of self-aligned vertical-channel poly-Si NW

Another process flow for the fabrication of a vertical-channel PSNW device is presented in Fig. 3. After defining the Si-active region, Si etching was performed and followed by gap filling. After performing oxide chemical-mechanical polishing (CMP) planarization, the SiN hard mask was stripped to form the device active area.

A photoresist hard mask was used to protect the planer MOSFET device areas; the wafer was then subjected to an HF dip to partially remove the Shallow Trench Isolation (STI) oxide regions in the unprotected areas. The approach

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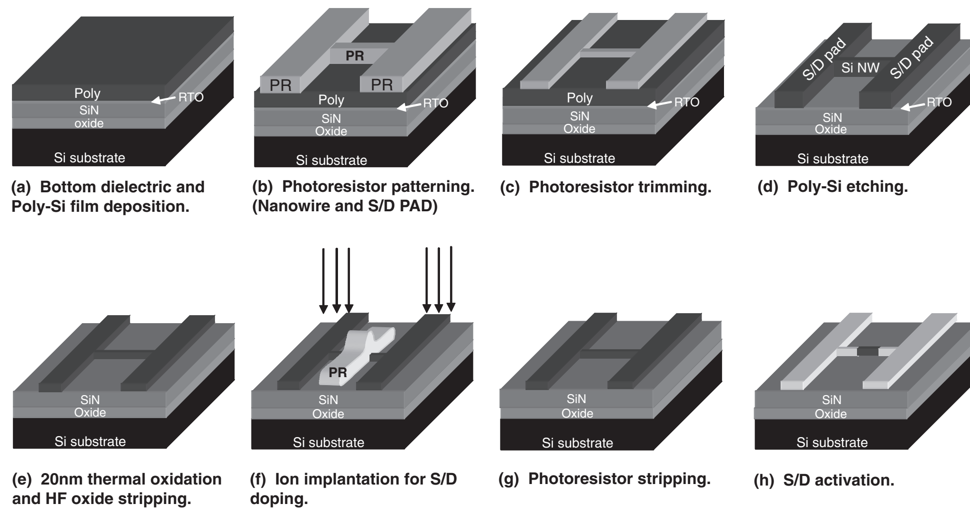

Fig. 1. Process flow for the fabrication of planar channel PSNW. A 10 keV and $5 \times 10^{15}/\mathrm{cm}^2$ phosphorus implantation is used for S/D pad resistance reduction. RTA is carried out at 900 °C for 30 s for dopant activation.

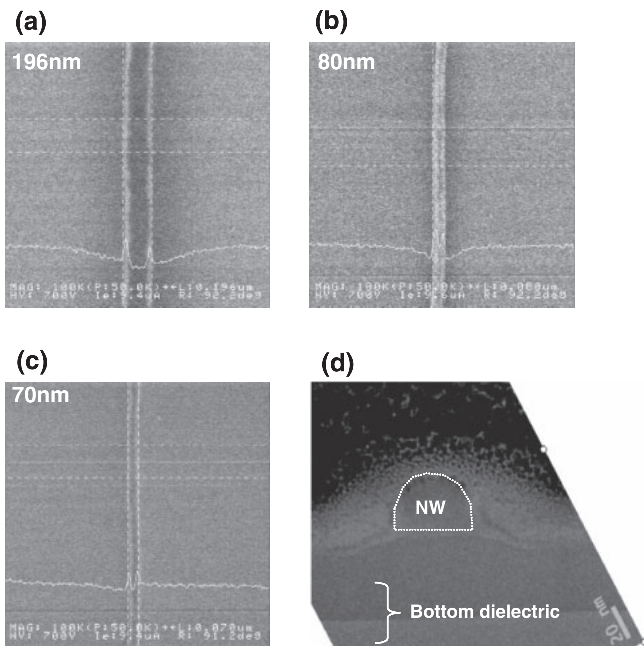

Fig. 2. The top-down SEM images of the PSNW two-step trimming process flow. (a) The nanowire photoresistor pattern after I-line exposure. (b) The photoresistor pattern after first plasma trimming. (c) The nanowire after Si etch and thermal oxidation trimming. (d) The cross-sectional TEM image of two-step trimmed nanowire.

is a simplified bulk Fin field-effect transistor (FinFET) process;[12] the fin-shaped active region acted as the gate electrode for the PSNW device. The photoresist hard mask was stripped and then a 10-nm-thick layer of TEOS was deposited using LPCVD at 750 °C, to function as the gate dielectric layer. A 50-nm-thick layer of poly-Si was deposited and then N^+ doping implantation using arsenic (dose: $1 \times 10^{15}/\mathrm{cm}^2$) was employed to induce PSNW source/drain doping. Patterning of the PSNW source/drain were performed using I-line lithography, followed by a reactive plasma etch for poly etching. This process led to the formation of a self-aligned undoped PSNW as a spacer of the fin-shaped active region. Next, a rapid thermal annealing (RTA; 900 °C, 30 s; N_2 ambient) was used for dopant activation and defect reduction. After annealing, a thin oxide layer was grown on the poly-Si surface that acts as a passivation layer for the PSNW.

3. Results and Discussion

3.1 Characteristics of planar-channel PSNW

Figure 4 shows the scheme used for testing a planar channel PSNW device and it presents comparisons of the electrical characteristics of SOI-made NWs and PSNWs. By using a thinner buried dielectric (58 nm effective oxide thickness of PSNW as compared to 150-nm-thick buried oxide of SOI) and carrying out thermal oxidation annealing, the PSNW exhibits subthreshold swing comparable to that of the SOI NW device and exhibits nearly hysteresis-free characteristics in the drain current drift in comparing forward and reverse gate-voltage sweep directions which indicates that no significant mobile oxide charge is present and the density of slow interface trap is low.[13,14] Figure 5 shows the PSNW FET statistics of the comparisons of the electrical characteristics for various wire widths with and without shrinkage due to the reoxidation process, and these characteristics are collected from 32 dies in each wafer. The driving current measured as the bottom gate bias is 5 V and drain bias is 0.5 V without any liquid solution on the nanowire surface. After the reoxidation process, the scaled PSNW exhibits tighter current distribution and superior performance. The reoxidation process not only increases the surface-to-volume ratio of the nanowire but also improves the PR trimming induced by the surface roughness. Irene *et al.*[15] found that a thin layer of intergranular oxide was formed between the poly grain during the high-temperature oxidation process that reduces the charge state density at the poly grain interface and passivates the grain boundary without introducing a series resistance. Additionally, the tighter distributions imply higher production yield and more accurate detection ability for nanosensor fabrication. To ensure stable device operation in a liquid solution environment, a plasma treatment is employed after S/D activation. NH_3 plasma treatment is carried out for 30 min, which

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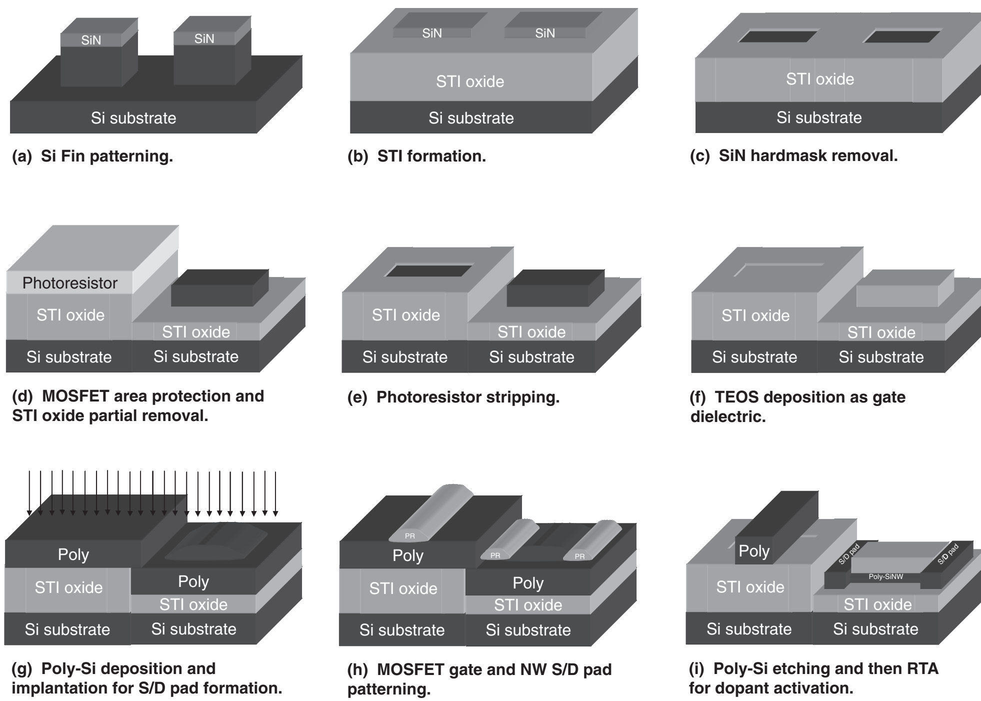

Fig. 3. Process flow for the fabrication of vertical-channel, self-aligned, PSNWs using bulk-Si technology.

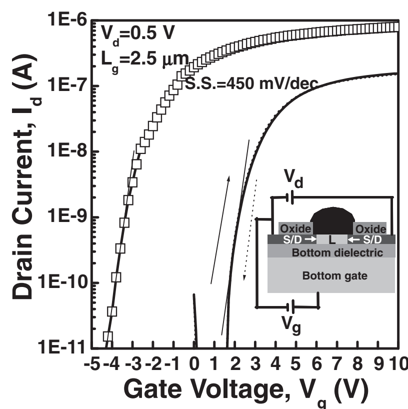

Fig. 4. Comparison of I_d–V_g characteristics of a fabricated PSNW FET device and SOI NW FET. The inset shows a schematic illustration of electrical testing of the nanowire FET configuration.

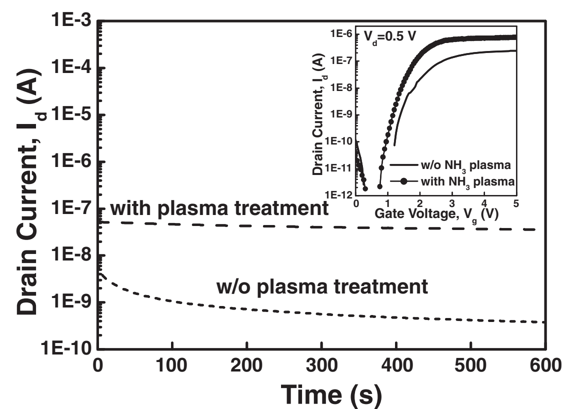

Fig. 6. The NH_3 plasma treatment improves the PSNW FET performance and stability under constant voltage ($V_g = 5$ V; $V_d = 0.5$ V) stress condition in the aqueous environment.

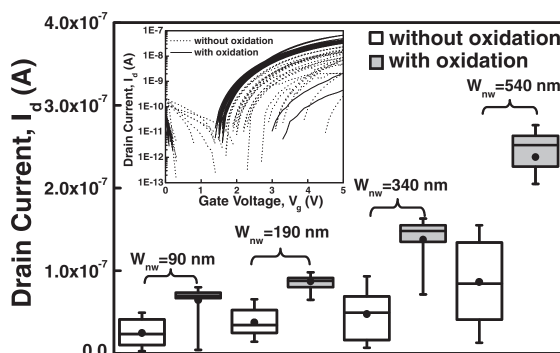

Fig. 5. PSNW FET I_{dsat} distribution within the wafer with various nanowire widths measured by SEM before oxidation. Those devices with second oxidation trimming exhibit superior current uniformity and device performance. Inset shows a comparison of the 32 die I_d–V_g characteristics for different oxidation effects.

passivates the dangling bond of the PSNW buried channel interface and improves the device performance.[16] The device stability measurement under constant voltage stress ($V_d = 0.5$ V and $V_g = 5$ V) in a liquid solution environment is shown in Fig. 6. The plasma passivation reduces the interface trap and avoids threshold voltage (V_{th}) variations due to mobile-ion diffusion. Figure 7 presents the I_d–V_g characteristics of the PSNW FET when the channel was exposed to buffered solutions with various pH values. The increase in the device response when the pH is above 7 can be attributed to silanol (≡SiOH) groups present in the surface oxide layer. Because the acidity (pK_a) of the silanol groups is *ca.* 6.8, deprotonation of the surface oxide layer occurs when the pH of the solution is higher than 7; this leads to the formation of negative charges on the surface.[17] As Fig. 7(b) shows, these changes in the net charge modify the surface potential and generate space charges at the

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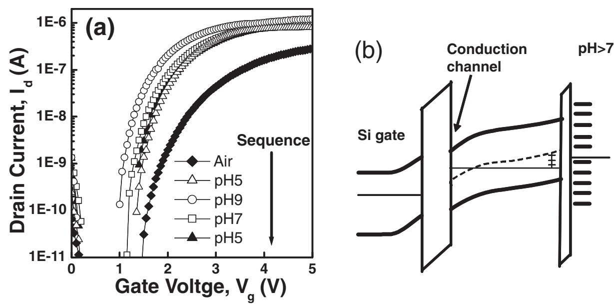

Fig. 7. (a) PSNW FET I_d–V_g measurement in aqueous solutions with varied pH concentration. The testing sequence is indicated by the arrow symbol. Each testing is performed after the solution is injected into the channel for 5 min. (b) The band diagram of this buried channel NW sensor in the pH > 7 solution.

surface silicon–thin oxide interface, in turn modifying the channel conductivity. It is worth noting that when the solution is switched from pH = 5 to 9 and then back to 5 again, the two I_d–V_g curves are not completely overlapping. The hysteresis is believed to be caused by the presence of buried OH sites just below the surface.[18] The buried OH sites are generated due to the water (H_2O) diffuse into SiO_2 and react with the SiO_2 and forms Si–OH sites. Although this number of Si–OH site buried below the surface is small compared to the number of sites on the surface, those slow response buried site will alter the pH_{pzc} of the surface oxide and the response of NW FET is changed as a consequence and lead to the hysteresis.[19,20] As compared to the V_{th} shift of the conventional surface channel ISFET, that of this buried-channel pH sensor (110 mV/pH) is significantly higher than the Nernst limit of 59.5 mV/pH.[21,22] By considering an analytical threshold voltage model and the body potential effect for thin Si SOI devices,[23] the coupling effect of the pH sensitivity can be approximately calculated by

$$\delta V_{gb} \sim -\frac{C_{si}}{C_{box}}\,\delta\varphi_s,$$

where V_{gb} is the threshold voltage of the buried-channel device; φ_s, the surface potential of the exposed device; and C_{si}, the Si-film capacitance ($\approx \varepsilon_s/T_{Si}$). In this experimental device, the coupling factor is 2.2; hence a pH sensitivity of 129.8 mV/pH will be achieved when the surface potential sensitivity reaches the Nernst limit. In addition, the device exhibits excellent reversible electrical characteristics after sequential measurement, indicating its sensitivity and repeatability in response to the variation of the surface charge. Such behavior makes this device suitable for applications to electrochemical detection.

3.2 Characteristics of self-aligned vertical-channel PSNW

Figure 8 shows the SEM and TEM images of the self-aligned vertical-channel PSNW formed around the fin-shaped Si. Using this sidewall NW formation approach, the vertical-channel width and the channel thickness of the PSNW in the device can be readily controlled by varying the topography of the STI oxide, recess region, and poly etch time. In particular, expensive lithography tools are not

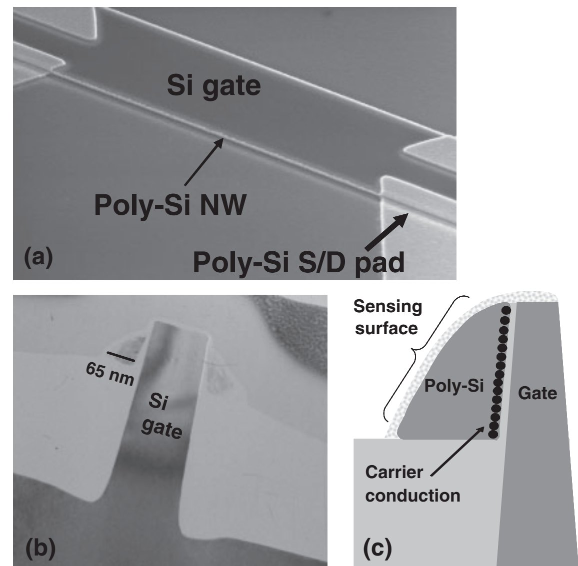

Fig. 8. (a) Tilt-angle SEM image of the vertical channel PSNW. (b) TEM image of a vertical channel, self-aligned, PSNW with a fin-shaped, Si gate electrode. (c) The schematic illustration of this self-aligned PSNW during current conduction.

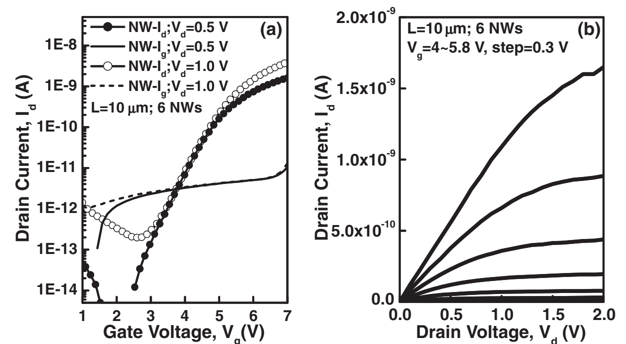

Fig. 9. *I*–*V* characteristics of a fabricated self-aligned PSNW FET device. (a) Subthreshold I_d–V_g characteristics with gate leakage current. (d) I_d–V_d output characteristics.

required to achieve such nanometer-scale NWs; further dimensional shrinkage, which is used to enhance the sensitivity, is achieved merely by increasing the poly etch time. To increase the uniformity of PSNW fabricated in both side of fin-shape wall, an optimal dummy pattern insertion technique[24] as well as the advance CMP process[25] can be included to alleviate the pattern loading effect to obtain the same topographies in both side of STI recess areas. Figure 9 shows the I_d–V_g and I_d–V_d characteristics of PSNW devices. A current flow occurred along the vertical sidewall and, the carrier density was modulated by the bias in the bulk Si. The on/off ratio of the device was *ca.* 10^5 with an applicable current level and a subthreshold swing of 0.65 V/dec. Unlike in the case of previous studies, the gate-bias of each NW could be determined independently—a highly desirable property when such sensors are embedded in a very-large-scale integration (VLSI) circuit. In addition, the value of the V_{th} of this undoped NW could be readily controlled by varying the degree of gate-electrode doping, thereby allowing a reduction in the subthreshold leakage current.

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Because a significant portion of the PSNW channel was exposed to the environment during operation, the device surface could be used as a sensing site by exploiting electrochemical reactions. An electrochemical reaction between the ambient and the device surface would induce charges at the channel surface, thus affecting the value of V_{th} of buried-channel devices. Because the sensitivity of the detection of small variations in conductance depends on the concentration or ionic strength of the undetermined species,[26] an embedded electronic circuit that exhibits different degrees of signal amplification, with corresponding noise reduction, would increase the detection limits. By using this integration approach, involving a CMOS-compatible manufacturing process, the production cost, device uniformity, and chip dimensions can all be reduced significantly.

4. Conclusions

In this study, we demonstrate an inexpensive and high-production yield fabrication process for PSNW FET devices that can be used for applications to electrochemical sensors. The device uniformity is controlled well by using certain manufacturing processes. Additionally, the highly integrated process will help to serve as an interface to connect the sensor and logic-based devices. The proposed process should lead to the development of portable and inexpensive sensor systems-on-a-chip that are mass produced using conventional semiconductor technology for applications to healthcare.

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