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## Dual-Material Gate Approach to Suppression of Random-Dopant-Induced Characteristic Fluctuation in 16 nm Metal–Oxide–Semiconductor Field-Effect-Transistor Devices

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In this work, we explore for the first time dual-material gate (DMG) and inverse DMG devices for suppressing the random-dopant (RD)-induced characteristic fluctuation in 16 nm metal–oxide–semiconductor field-effect-transistor (MOSFET) devices. The physical mechanism of suppressing the characteristic fluctuation of DMG devices is observed and discussed. The achieved improvement in suppressing the RD-induced threshold voltage, on-state current, and off-state current fluctuations are 28, 12.3, and 59%, respectively. To further suppress the fluctuations, an approach that combines the DMG method and channel-doping-profile engineering is also advanced and explored. The results of our study show that among the suppression techniques, the use of the DMG device with an inverse lateral asymmetric channel-doping-profile has good immunity to fluctuation. © 2011 The Japan Society of Applied Physics

### 1. Introduction

The minimum feature size of metal–oxide–semiconductor field-effect transistors (MOSFETs) has been rapidly scaled down, and the variability leading to line edge roughness,<sup>1,2)</sup> the granularity of polysilicon gates,<sup>3–5)</sup> and random discrete dopant<sup>5–30)</sup> effects now substantially affects MOSFET characteristics. Various effects of randomness resulting from the random nature of manufacturing processes, such as ion implantation, diffusion, and thermal annealing,<sup>16)</sup> have induced significant fluctuations in the electrical characteristics of nanoscale MOSFETs. The number of dopants is on the order of tens in the depletion region in a nanoscale MOSFET, whose effect on device characteristics is large enough to be distinct. Various random dopant effects have recently been studied using both experimental and theoretical approaches.<sup>5–30)</sup> The fluctuations in characteristics are caused not only by a variation in average doping density, which is associated with the fluctuation in the number of impurities, but also by a particular random distribution of impurities in the channel region. Recently, fluctuation-related issues in semiconductor devices<sup>5–27)</sup> and circuits<sup>27–30)</sup> indicate that random-dopant (RD)-induced threshold voltage ( $V_{th}$ ) fluctuation has become a crucial problem with today's MOSFET devices. The suppression of RD-induced  $V_{th}$  fluctuation is thus urgent for 16 nm device technologies. The dual-material gate (DMG) has recently been proposed to improve MOSFET performance.<sup>31)</sup> However, the effects of random dopants on MOSFET devices with a DMG structure have not been studied yet.

In this work, we explore the effectiveness of the use of DMG and inverse DMG devices for the suppression of RD-induced characteristic fluctuation in 16 nm MOSFET devices. To explore such fluctuations, a large-scale three-dimensional (3D) “atomistic” device simulation is performed by solving a set of quantum-mechanically corrected drift-diffusion equations by the density gradient method<sup>32–35)</sup> using our parallel computing system.<sup>36–38)</sup> On the basis of the effect of the dopant position inside the channel region, we investigate the fluctuation suppression of DMG and inverse DMG devices; consequently, the physical mechanism of the fluctuation suppression is disclosed and discussed.

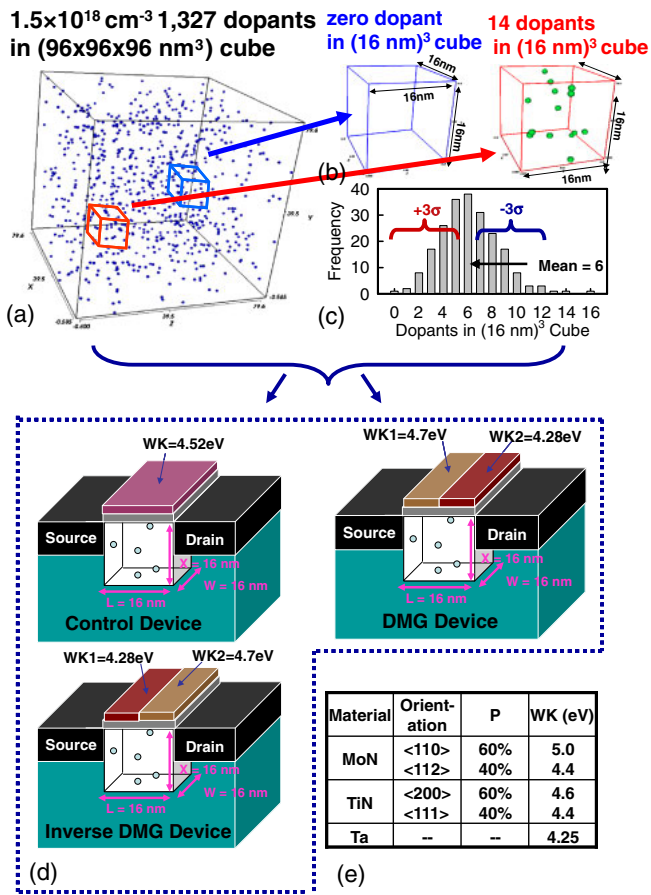
The results of this study show that devices with a DMG structure possess interesting fluctuation suppression. Note that lateral asymmetric channel (LAC) and inverse LAC (inLAC) devices have also been reported in our recent work<sup>39)</sup> for suppressing RD-induced characteristic fluctuation. Therefore, except for the proposed DMG approach in this work, by simultaneously integrating the channel-doping-profile engineering technique<sup>39)</sup> in the device's channel doping profile, techniques for fabricating DMG devices with an LAC and inLAC, which exhibit good effectiveness of fluctuation suppression, are further explored.

This paper is organized as follows. In §2, we introduce the analytical technique used for studying the RD effect in 16 nm MOSFET devices. In §3, we report our result and examine the effectiveness of fluctuation as determined by various approaches. Finally, we draw our conclusions and suggest future works in §4.

### 2. Simulation Technique

The control device here has a titanium nitride/hafnium silicon oxynitride (TiN/HfSiON) gate stack of 0.8 nm effective oxide thickness. The gate length and width are both 16 nm, and the work function (WK) is 4.52 eV. Outside the channel, the doping concentrations of the source/drain and background are  $1.045 \times 10^{20}$  and  $1 \times 10^{15} \text{ cm}^{-3}$ , respectively. In the channel region, to consider the effects of the random fluctuations in the number and location of discrete channel dopants, 1327 dopants are first randomly generated in a  $96 \times 96 \times 96 \text{ nm}^3$  cube, in which the equivalent doping concentration is  $1.5 \times 10^{18} \text{ cm}^{-3}$ , as shown in Fig. 1(a). The  $96 \times 96 \times 96 \text{ nm}^3$  cube is then partitioned into 216 subcubes of  $16 \times 16 \times 16 \text{ nm}^3$ . The number of dopants may vary from 0 to 14, and its average is 6, as shown in Figs. 1(b) and 1(c), respectively. The 216 subcubes are then equivalently mapped in the channel region of the explored device for 3D “atomistic” device simulation with discrete dopants, as shown in Fig. 1(d). The device simulation is performed by solving a set of 3D density-gradient equations coupled with the Poisson equation as well as electron–hole current continuity equations.<sup>17,18,22,34)</sup> The characteristic fluctuation of devices was validated with respect to experimentally measured data to ensure the highest accuracy.<sup>18)</sup>

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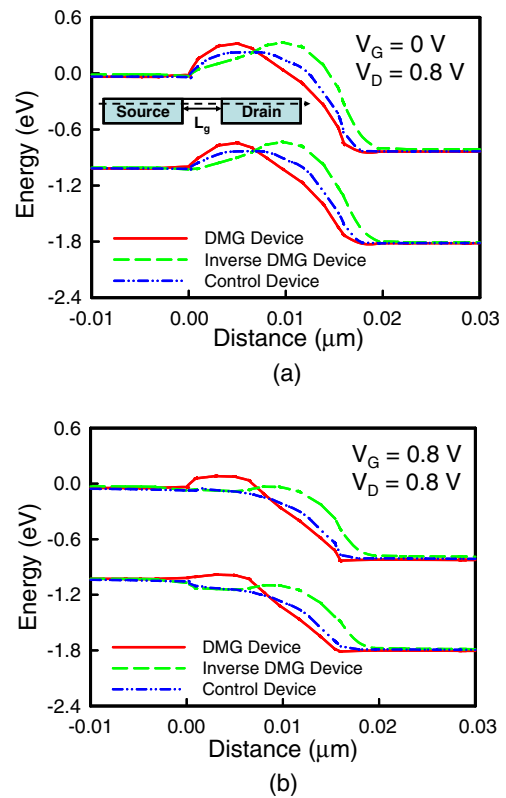


**Fig. 1.** (Color online) (a) 1327 dopants are randomly generated in a large cube of  $96 \times 96 \times 96 \text{ nm}^3$ , in which the equivalent doping concentration is  $1.5 \times 10^{18} \text{ cm}^{-3}$ . The large cube is then partitioned into 216 subcubes of  $16 \times 16 \times 16 \text{ nm}^3$ . The number of dopants in each subcube may vary from 0 to 14, and its average is 6 (b, c). (d) The 216 subcubes are equivalently mapped in the channel region of the control, DMG, and inverse DMG devices. (e) Properties of metal material used in this work.

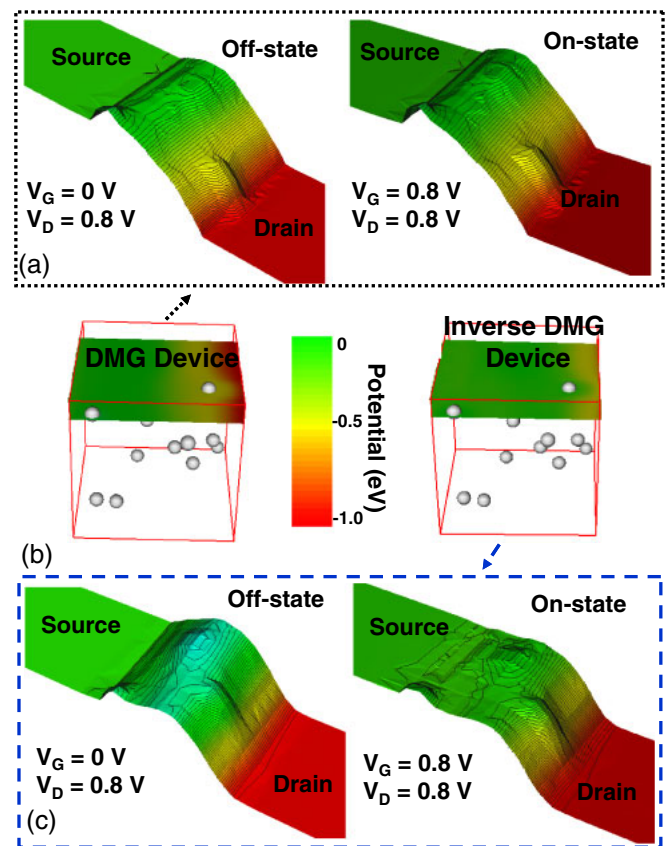
Without loss of generality, the explored DMG and inverse DMG devices, as shown in Fig. 1(d), have a 16 nm gate and a  $1.5 \times 10^{18} \text{ cm}^{-3}$  equivalent channel doping concentration. In the DMG device, the WKs at the source and drain sides are denoted as WK1 and WK2, respectively, and  $WK1 > WK2$ . The inverse DMG device is designed accordingly, and  $WK1 < WK2$ . The gate materials were molybdenum nitride (MoN), titanium nitride (TiN), and tantalum (Ta), whose distributions of grain orientation and WK are summarized in Fig. 1(e).<sup>31)</sup>  $V_{th}$  for each device is calibrated to 250 mV for our following examinations, in accordance with the 2007 ITRS Roadmap for low-operating-power applications.

### 3. Results and Discussion

A device with a high WK near the source or drain side may induce relatively high intrinsic electrostatic potential barriers for both the on- and off-states, as shown in Figs. 2(a) and 2(b), respectively. The RD induces rather different potential profiles owing to the difference in WK, in spite of the same number and position of dopants, as shown in Figs. 3(a)–3(c). Therefore, the RD-induced drain current versus gate voltage ( $I_D - V_G$ ) fluctuations for both the inverse DMG and DMG devices are further shown in Figs. 4(a) and 4(b),



**Fig. 2.** (Color online) Energy band diagrams of the (a) off-state and (b) on-state for the nominal control, DMG and inverse DMG devices.



**Fig. 3.** (Color online) Fourteen-random-dopant-induced potential profiles extracted from the on- and off-state of the (a) DMG and (c) inverse DMG devices. (b) Fourteen random dopants within the channel of DMG and inverse DMG devices.

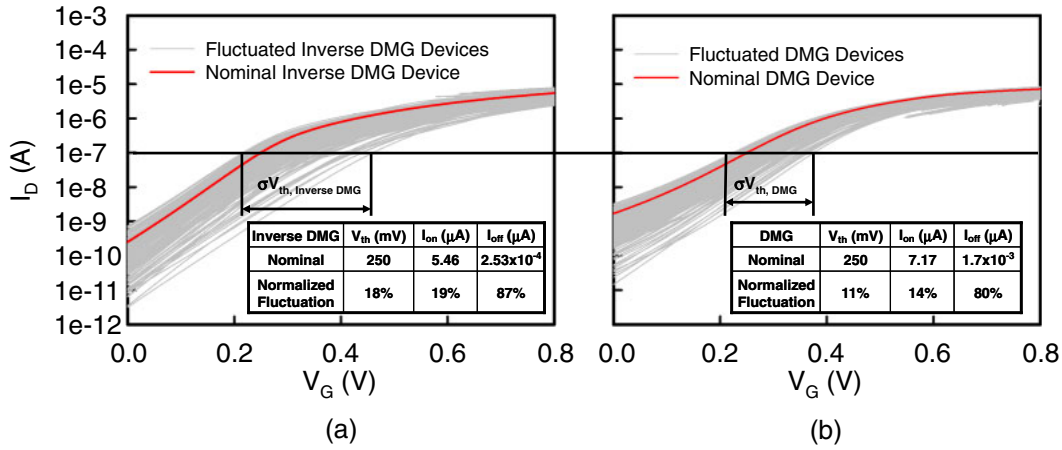


Fig. 4. (Color online)  $I_D$ - $V_G$  curves of the (a) inverse DMG and (b) DMG devices. The nominal values and normalized characteristic variations for the inverse DMG and DMG devices are summarized in the respective insets.

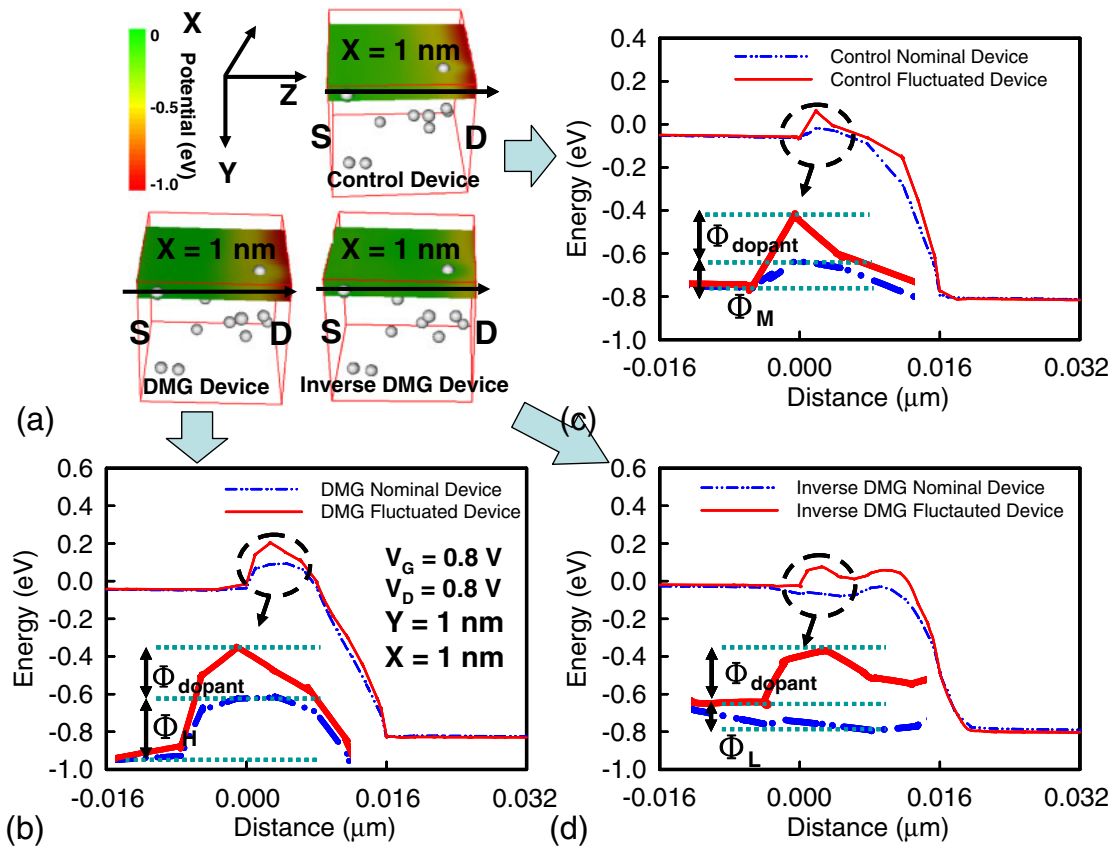
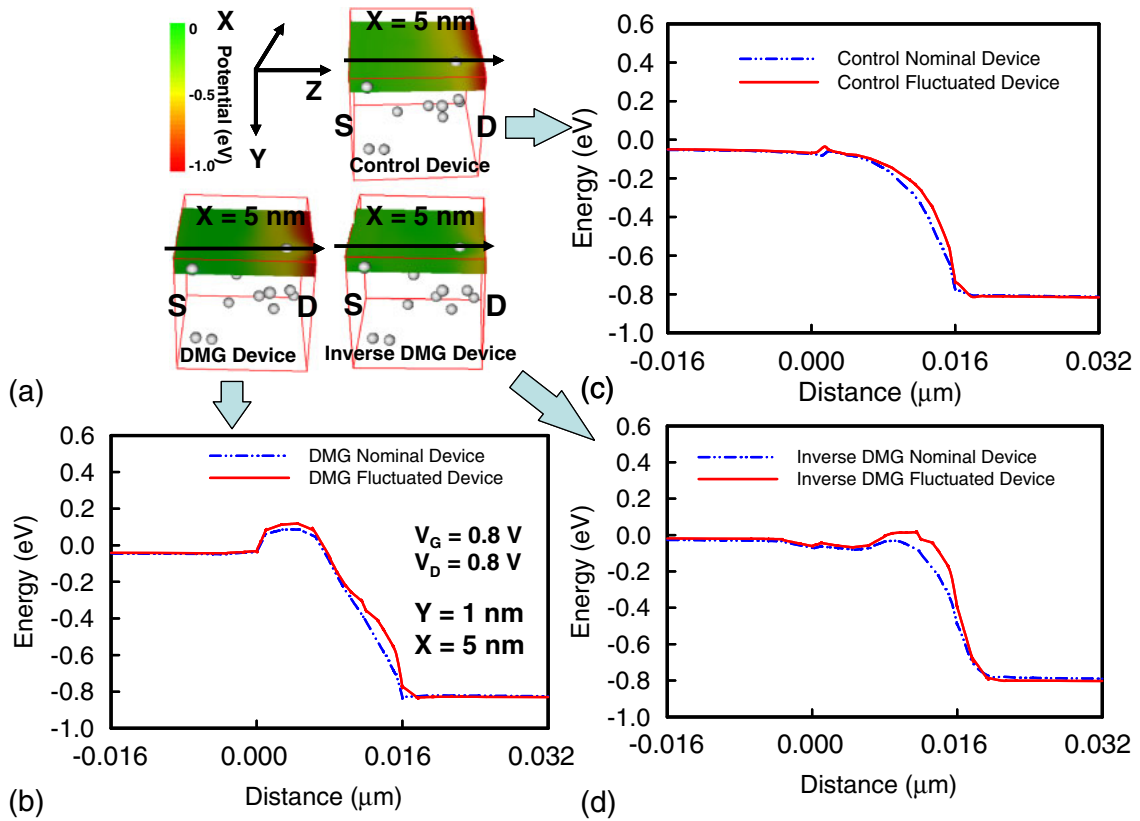


Fig. 5. (Color online) (a) Surface potential energies induced by the 14 random dopants for the control, DMG, and inverse DMG devices. (b)–(d) Slicing plots of the potential energy for the dopants near the source side.

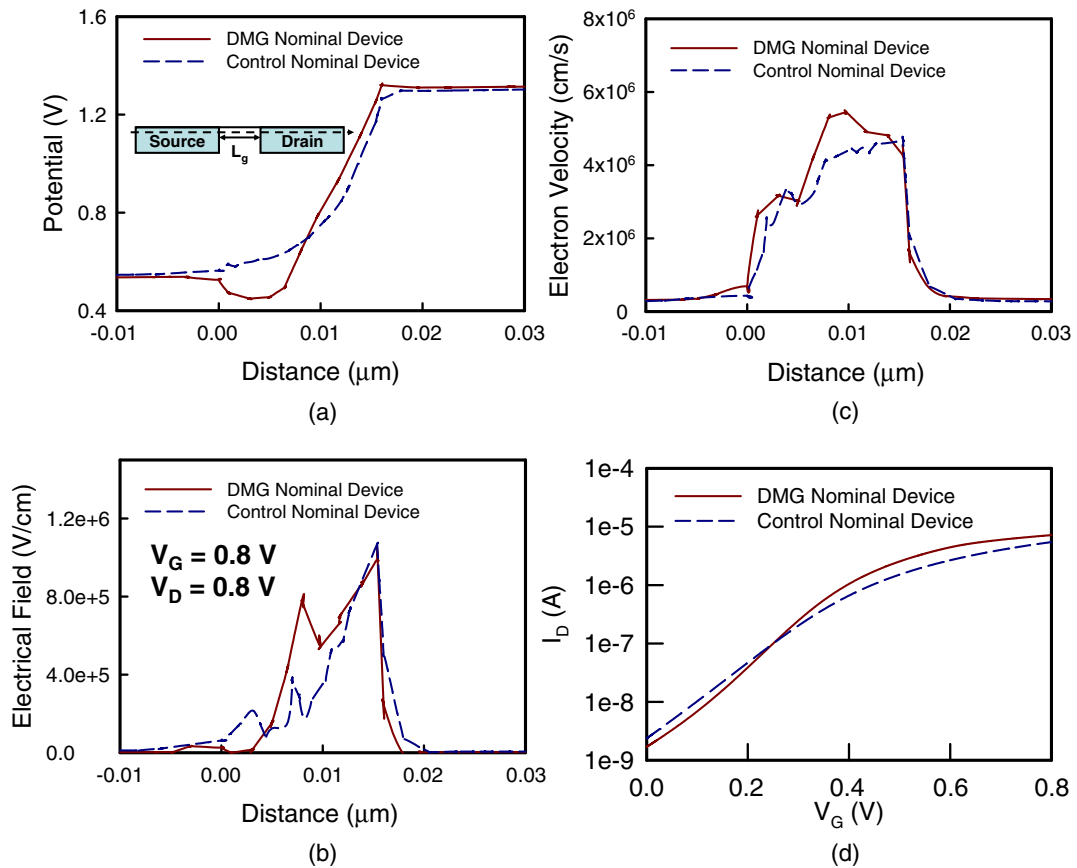
respectively. The inset tables of Figs. 4(a) and 4(b) list the nominal values and normalized fluctuations (the standard deviation divided by the mean value for various DC characteristics). The  $V_{th}$  fluctuations are 51.9 and 30.8 mV for the inverse DMG and DMG devices, respectively, and the DMG devices show small DC characteristic fluctuations. The normalized fluctuations of the on-state current ( $I_{on}$ ) and off-state current ( $I_{off}$ ) of the DMG devices are 14 and 80%, respectively, which are smaller than those of the inverse DMG device (18 and 87%).

To obtain physical insights into  $V_{th}$  fluctuations, the same dopant-number- and dopant-position-induced potential en-

ergies are shown in Fig. 5. The dopants result in sizeable potential deviations, and the high, low, and control WK-induced potential barriers are denoted by  $\Phi_H$ ,  $\Phi_L$ , and  $\Phi_M$ , respectively, as shown in Fig. 5. As shown in Figs. 5(a)–5(d), the dopants induce a relatively small potential deviation in the DMG device due to the existence of a high initial potential barrier ( $\Phi_{dopant}/\Phi_H$ , compared with  $\Phi_{dopant}/\Phi_L$  and  $\Phi_{dopant}/\Phi_M$ ) in the cross-sectional view of potential energies for the dopant near the source side. Therefore, the DC characteristic fluctuations in the DMG device are markedly reduced. However, the same phenomenon for the dopant near the drain side cannot exploit the

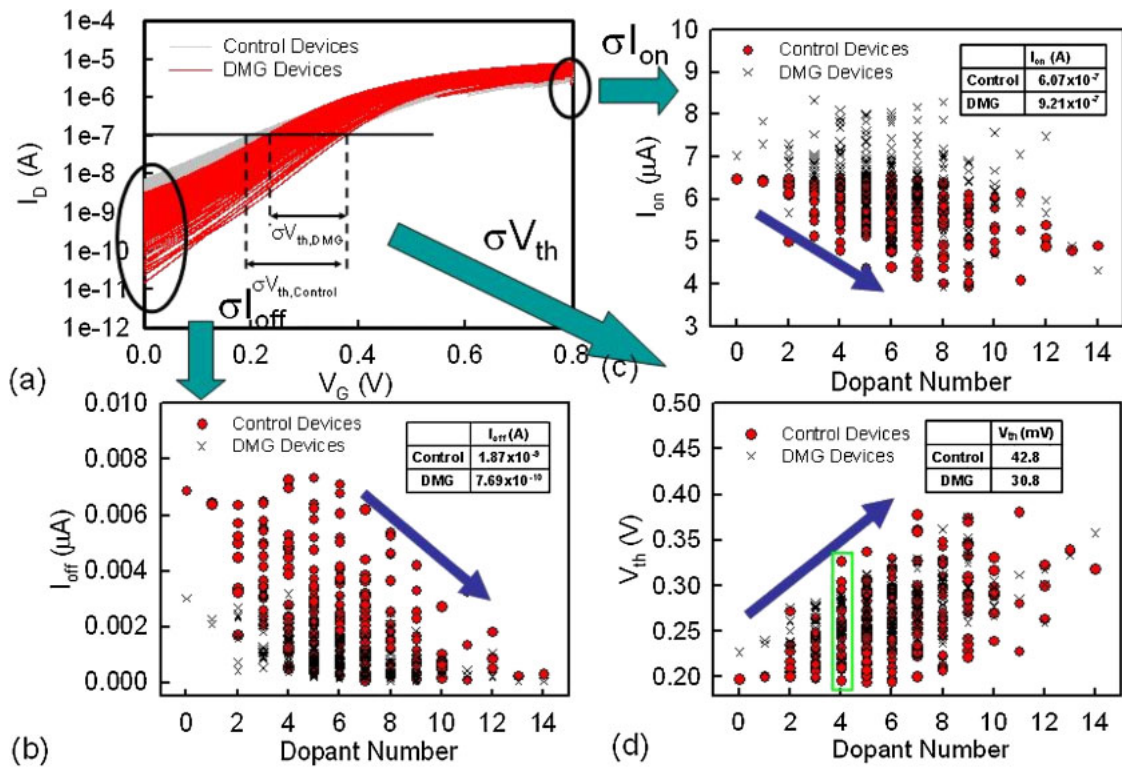


**Fig. 6.** (Color online) (a) Surface potential energies induced by the 14 random dopants for the control, DMG, and inverse DMG devices. (b)–(d) Slicing plots of the potential energy for the dopants near the drain side.



**Fig. 7.** (Color online) Comparison of the nominal (a) surface potentials, (b) lateral electric fields, (c) electron velocities, and (d)  $I_D$ – $V_G$  curves of the DMG and control samples.





**Fig. 8.** (Color online) (a) Comparison of the RD-induced  $I_D$ - $V_G$  curves of the DMG device (red line) and control sample (gray line). (b)  $I_{off}$ , (c)  $I_{on}$ , and (d)  $V_{th}$  fluctuations extracted from (a).

advantage of the inverse DMG structure because carrier controllability is completely decided at the source edge, as shown in Figs. 6(a)–6(d). Comparisons of  $I_D$ - $V_G$ , potential, electron velocity, and lateral electric field between both the DMG and control devices are further conducted, as shown in Fig. 7. As can be seen in the plot in Fig. 7(a), the DMG device shows an abrupt potential step in the middle of the channel. This abrupt potential step mainly comes from the difference in WK between the different gate materials, and the potential profile of the DMG device results in a locally enhanced lateral electric field inside the channel. For the plot in Fig. 7(b), the control device attains its maximum electric field near the drain, similarly to in a classical electric field profile. However, the DMG device studied has the peak electric field inside the channel as well as near the drain. A locally generated electric field inside the channel results in a relatively high carrier velocity, where Fig. 7(c) shows the velocity profiles along the channel direction. Therefore, the DMG device has a larger  $I_{on}$  at a similar  $I_{off}$  than the control device, as shown in Fig. 7(d). The effects of the random dopant number and position on the DC characteristics of the DMG and control devices are confirmed from results of our recent work,<sup>18</sup> as shown in Figs. 8(a)–8(d). The increase in dopant number with the equivalent channel doping concentration substantially alters  $V_{th}$ ,  $I_{on}$ , and  $I_{off}$ . Additionally, the position of random dopants induces rather different fluctuations in characteristics in spite of the same number of dopants used, as shown in the inset of Fig. 8(d). Finally, Table I shows a summary of the results obtained using different suppression techniques for devices with the DMG structure; compared with those obtained in our recent studies,<sup>18,39–41</sup> the achieved improve-

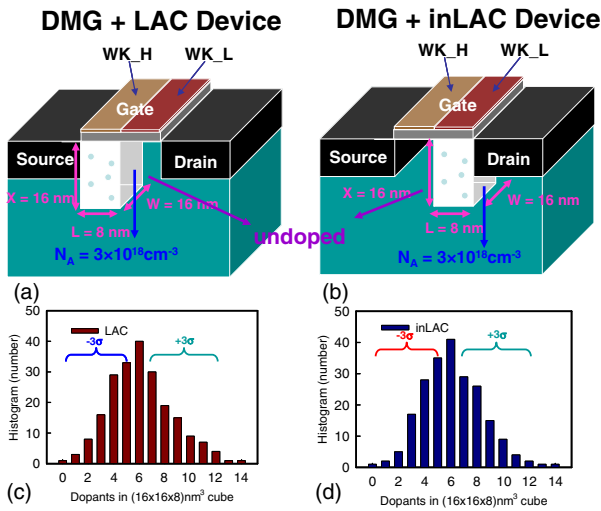
**Table I.** Summary of improvements in DC characteristic fluctuations in this work.

Improvement	DMG	inLAC <sup>a)</sup>	Vertical doping profile <sup>b)</sup>	Reduce EOT to 0.4 nm <sup>c)</sup>	Increase WK <sup>d)</sup>
$V_{th}$ fluctuation (%)	28	33.6	14	20	—
$I_{on}$ fluctuation (%)	12.3	32.2	22	36	—
$I_{off}$ fluctuation (%)	59	—	2	21.2	—

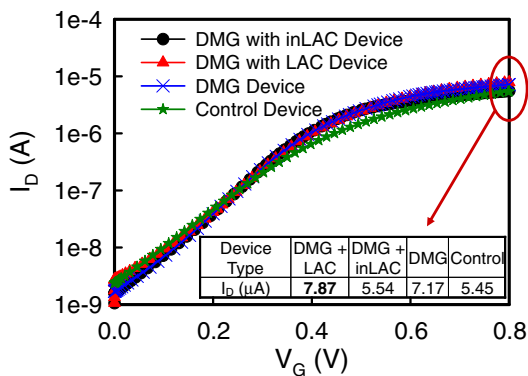
a) Ref. 39. b) Ref. 41. c) Ref. 42. d) Ref. 18.

ments of the DMG structure for suppressing RD-induced  $V_{th}$ ,  $I_{on}$ , and  $I_{off}$  fluctuations are 28, 12.3, and 59%, respectively.

Devices showing the LAC and inLAC doping profiles have been reported in our recent work<sup>39</sup> on the suppression of RD-induced characteristic fluctuations, where the DC and AC characteristics were examined and compared for 16 nm MOSFET devices and circuits. We observed in that work that a device with dopants near the drain end exhibits less characteristic fluctuations owing to the well-controlled major fluctuation source of the gate-drain capacitance.<sup>39</sup> Therefore, to further suppress the fluctuation, the channel-engineering techniques of the LAC and inLAC together with the DMG approach are advanced for the 16 nm devices studied. The adopted near-source-end doping profile implemented with the DMG (i.e., DMG + LAC) device and the near-drain-end channel doping profile implemented with the DMG (i.e., DMG + inLAC) device are shown in Figs. 9(a) and 9(b), respectively. In order to estimate the combined effect for the proposed approaches, both methods are also intensively simulated. Only half of the channels are



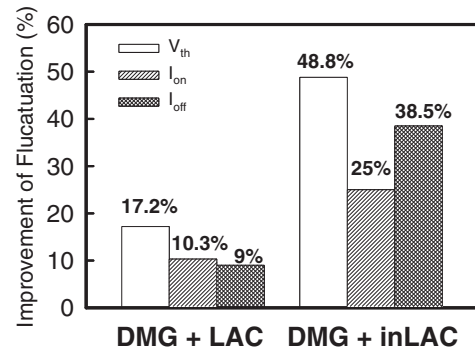
**Fig. 9.** (Color online) Adopted (a) near-source-end doping profile implemented with DMG device (i.e., DMG + LAC) and (b) near-drain-end channel doping profile implemented with DMG device (i.e., DMG + LAC). Histograms of the dopants in 216 subcubes (subcube size is  $16 \times 16 \times 8 \text{ nm}^3$ ) for the (c) near-source-end and (d) near-drain-end channel doping profiles.



**Fig. 10.** (Color online)  $I_D$ - $V_G$  characteristics of the nominal control, DMG, DMG + LAC, and DMG + inLAC devices.

doped and 1327 dopants are randomly generated in a large rectangular solid [the dimensions (gate width, source-drain direction, and channel depth) are  $96 \times 48 \times 96 \text{ nm}^3$ ]. Therefore, the effective channel doping concentration is still equal to  $1.5 \times 10^{18} \text{ cm}^{-3}$ . Then, the large cube is partitioned into 216 subcubes (the subcube dimensions are  $16 \times 8 \times 16 \text{ nm}^3$ ) and mapped into the drain end (or source end) of the channel region for discrete dopant simulation. The number of dopants in the subcubes may vary from zero to 14 (average, 6), as shown in Figs. 9(c) and 9(d).

To determine the advantages of the LAC and inLAC devices,<sup>42,43</sup> the simulated  $I_D$ - $V_G$  characteristics of the nominal control, DMG, DMG + LAC, and DMG + inLAC devices are examined, as shown in Fig. 10. We observe that the characteristics of the DMG, DMG + LAC, and DMG + inLAC devices are superior to those of the control sample. In addition, the  $I_{on}$  of the DMG + LAC device is better than those of the DMG and DMG + inLAC devices, as shown in Fig. 10. However, from the aspect of RD-induced characteristic fluctuation, the fluctuation of injection velocity



**Fig. 11.** Comparison of various DC characteristic fluctuations between the proposed DMG + LAC and DMG + inLAC devices. We have compared the DMG + LAC and DMG + inLAC devices with the control device, where the  $V_{th}$  fluctuation of the control device is 42.8 mV. The  $V_{th}$  fluctuation decreased from 42.8 mV for the control device to 35.4 mV for the DMG + LAC device; therefore, a 17.2% improvement was obtained.

will be observed at the source end of the LAC device, and thus the  $V_{th}$  fluctuation increases from 30.7 mV for the DMG device to 35.4 mV for DMG + LAC device (about 17.2% improvement; this is because the  $V_{th}$  fluctuation decreases from 42.8 mV for the control device to 35.4 mV for the DMG + LAC device), as shown in Fig. 11. Fortunately, the nominal DMG + inLAC device not only has a large  $I_{on}$  compared with the control device owing to the inLAC device gaining a high carrier velocity from the structure of the DMG, but also shows a small RD-induced  $V_{th}$  fluctuation (about 48.8% improvement, relative to that of the control sample, has been estimated similarly). The suppressions result from the channel doping profile and the gate electrode of the DMG + inLAC device. Therefore, the calculated improvement of RD-induced characteristic fluctuation for the DMG + inLAC device has more than one clearly dissimilar aspect: one is based mainly on the well-controlled major fluctuation source of the gate-drain capacitance in the inLAC channel and the other is the small potential deviation in the DMG, as discussed in §3.

**4. Conclusions**

We have studied the DMG and inverse DMG techniques for suppressing RD-induced characteristic fluctuations for 16 nm MOSFET devices. The use of a device with the DMG structure is an effective means of reducing DC characteristic fluctuations, compared with that of the inverse DMG and control samples. The suppression of the RD-induced characteristic fluctuations of the DMG + inLAC device was also explored. This study has provided insight into the design of gate- and channel-engineering techniques for suppressing RD-induced characteristic fluctuations and has shown a design trade-off between performance and fluctuation. The suppression of the AC characteristic fluctuations of the devices studied is under investigation. We are currently conducting sample fabrication and measurement to evaluate this technique.

**Acknowledgments**

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- 1) A. Asenov, S. Kaya, and A. R. Brown: *IEEE Trans. Electron Devices* **50** (2003) 1254.
- 2) G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov: *IEEE Trans. Electron Devices* **53** (2006) 3063.
- 3) H. P. Tuinhout, A. H. Montree, J. Schmitz, and P. A. Stolk: *IEDM Tech. Dig.*, 1997, p. 631.
- 4) A. R. Brown, G. Roy, and A. Asenov: *IEEE Trans. Electron Devices* **54** (2007) 3056.
- 5) R. W. Keyes: *Appl. Phys. A* **8** (1975) 251.
- 6) R. P. Joshi and D. K. Ferry: *Phys. Rev. B* **43** (1991) 9734.
- 7) P. Francis, A. Terao, and D. Flandre: *IEEE Trans. Electron Devices* **41** (1994) 715.
- 8) J.-R. Zhou and D. K. Ferry: *IEEE Comput. Sci. Eng.* **2** (1995) 30.
- 9) X.-H. Tang, V. K. De, and J. D. Meindl: *IEEE Trans. VLSI Syst.* **5** (1997) 369.
- 10) K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto, and C. Hu: *IEEE Trans. Electron Devices* **45** (1998) 809.
- 11) P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen: *IEEE Trans. Electron Devices* **45** (1998) 1960.
- 12) D. Vasileska, W. J. Gross, and D. K. Ferry: *Ext. Abstr. Int. Workshop Computational Electronics*, 1998, p. 259.
- 13) W. J. Gross, D. Vasileska, and D. K. Ferry: *IEEE Electron Device Lett.* **20** (1999) 463.
- 14) H.-S. Wong, Y. Taur, and D. J. Frank: *Microelectron. Reliab.* **38** (1999) 1447.
- 15) N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama: *IEDM Tech. Dig.*, 2000, p. 175.
- 16) C. Y. Chang and S. M. Sze: *ULSI Technology* (McGraw-Hill, New York, 1996).
- 17) Y. Li and S.-M. Yu: *Jpn. J. Appl. Phys.* **45** (2006) 6860.
- 18) Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang: *IEEE Trans. Electron Devices* **55** (2008) 1449.
- 19) F.-L. Yang, J.-R. Hwang, and Y. Li: *IEEE Custom Integrated Circuits Conf.*, 2006, p. 691.
- 20) Y. Li, S.-M. Yu, and H.-M. Chen: *Microelectron. Eng.* **84** (2007) 2117.
- 21) Y. Li and C.-H. Hwang: *J. Appl. Phys.* **102** (2007) 084509.
- 22) Y. Li and S.-M. Yu: *IEEE Trans. Semicond. Manuf.* **20** (2007) 432.
- 23) Y. Li and S.-M. Yu: *J. Comput. Electron.* **5** (2006) 125.
- 24) A. R. Brown, A. Asenov, and J. R. Watling: *IEEE Trans. Nanotechnol.* **1** (2002) 195.
- 25) A. Asenov and S. Saini: *IEEE Trans. Electron Devices* **46** (1999) 1718.
- 26) K. Takeuchi, T. Tatsumi, and A. Urukawa: *IEDM Tech. Dig.*, 1997, p. 841.
- 27) R. Tanabe, Y. Ashizawa, and H. Oka: *Proc. IEEE Int. Conf. Simulation of Semiconductor Processes Device*, 2006, p. 103.
- 28) B. Cheng, S. Roy, G. Roy, and A. Asenov: *Int. Solid-State Integrated Circuit Technol. Conf.*, 2006, p. 1290.
- 29) H. Mahmoodi, S. Mukhopadhyay, and K. Roy: *IEEE J. Solid-State Circuits* **40** (2005) 1787.
- 30) B. Cheng, S. Roy, G. Roy, A. Brown, and A. Asenov: *Proc. 36th European Solid-State Device Research Conf.*, 2006, p. 258.
- 31) S. Chakraborty, A. Mallik, and C. K. Sarkar: *IEEE Trans. Electron Devices* **55** (2008) 827.
- 32) M. G. Ancona and H. F. Tiersten: *Phys. Rev. B* **35** (1987) 7959.
- 33) S. Odanaka: *IEEE Trans. Comput.-Aided Des. IC Syst.* **23** (2004) 837.
- 34) T.-W. Tang, X. Wang, and Y. Li: *J. Comput. Electron.* **1** (2002) 389.
- 35) G. Roy, A. R. Brown, A. Asenov, and S. Roy: *J. Comput. Electron.* **2** (2003) 323.
- 36) Y. Li and S.-M. Yu: *J. Comput. Appl. Math.* **175** (2005) 87.
- 37) Y. Li, H.-M. Lu, T.-W. Tang, and S. M. Sze: *Math. Comput. Simulation* **62** (2003) 413.
- 38) Y. Li, S. M. Sze, and T. S. Chao: *Eng. Comput.* **18** (2002) 124.
- 39) K.-F. Lee, Y. Li, and C.-H. Hwang: *Semicond. Sci. Technol.* **25** (2010) 045006.
- 40) Y. Li, C.-H. Hwang, T.-C. Yeh, and H.-M. Huang: *Proc. IEEE Int. Conf. Simulation of Semiconductor Processes and Devices*, 2008, p. 22-1.
- 41) M.-H. Han, Y. Li, and C.-H. Hwang: *Jpn. J. Appl. Phys.* **49** (2010) 04DC02.
- 42) J. Hoentschel, A. Wei, M. Wiatr, A. Gehring, T. Scheiper, R. Mulfinger, T. Feudel, T. Lingner, A. Poock, S. Muehle, C. Krueger, T. Herrmann, W. Kliex, R. Stenzel, R. Stephan, P. Huebler, T. Kammler, P. Shi, M. Raab, D. Greenlaw, and M. Horstmann: *IEDM Tech. Dig.*, 2008, p. 649.
- 43) K. Narasimhulu, M.-P. Desai, S.-G. Narendra, and V.-R. Rao: *IEEE Trans. Electron Devices* **51** (2004) 1416.