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Nanosized-Metal-Grain-Induced Characteristic Fluctuation in 16 nm Complementary Metal–Oxide–Semiconductor Devices and Digital Circuits

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In this work, we investigate the effect of random work functions (WKs) resulting from the nanosized grains of a metal gate on 16 nm metal–oxide–semiconductor field-effect transistor (MOSFET) devices and circuits. The random number and position of nanosized metal grains induce rather different random WKs on a MOSFET gate, which cannot be modeled using an averaged WK; thus, we consider each WK of the metal gate, according to the size of partitioned grains, in three-dimensional device simulation. The results of this study indicate that the random-WK-induced threshold voltage fluctuation of N- and P-MOSFETs are about 1.5 and 1.6 times higher than the results calculated by the recently reported averaged WK fluctuation method. This is because even if the devices have similar threshold voltages, they may exhibit quite different combinations of WKs owing to the random position of nanosized metal grains on the devices' gate. Coupled device-circuit simulation is further adopted to explore the timing fluctuations of complementary metal–oxide–semiconductor (CMOS) inverter circuits. The random position of nanosized metal grains results in 10 and 12% variations in the timing fluctuation and power consumption of the CMOS inverter circuit.
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1. Introduction

The feature dimensions of field-effect transistors (FETs) have been rapidly scaled down and thus characteristic variability has become one of the major challenges in complementary metal–oxide–semiconductor (CMOS) technologies.[1–7] Diverse approaches to examining intrinsic parameter fluctuations in CMOS devices and circuits have recently been presented.[8–23] Devices with a high-κ/metal gate compose a technology for suppressing such intrinsic parameter fluctuations.[24] The advantages of this approach are as follows: small gate leakage current, increased gate capacitance, reduced sheet resistance, and weak threshold voltage's pinning effect and phonon scattering effect; these have been recognized as the key to the sub-45-nm device era. However, the grain orientation of metals on small gate areas is uncontrollable during fabrication processes.[25,26] Recently, the averaged work function fluctuation (AWKF) method of estimating the WKF in device and circuit variability has been reported,[27] but this approach does not consider the effects of the random number or position of nanosized metal grains simultaneously in studying the random work functions (WKs) on the devices' characteristics. It will be interesting to study whether the dependence of WK on metal grains[28,29] can be considered in assessing characteristic variability in 16-nm-gate CMOS devices.

In this work, we study the effects of WKF, resulting from nanosized grains of a metal gate, on 16 nm CMOS device and circuit characteristics, as shown in Fig. 1. To estimate the impact of random WKs on device and circuit characteristics, we simultaneously consider each WK of a metal gate, according to the size of partitioned grains, in three-dimensional (3D) device simulation. The random-WK-induced threshold voltage fluctuations (σV_{th}) of N- and P-metal–oxide–semiconductor field-effect transistors (MOSFETs) are about 1.5 and 1.6 times higher than the results of the AWKF method. One of the main reasons for this is that even if the devices have similar threshold voltages, they may still exhibit quite different combinations of WKs owing to the random position of nanosized metal grains on their gate. This effect cannot be explained by the AWKF method. Owing to the lack of a well-established compact model for 16 nm devices, coupled device-circuit simulation is further adopted to explore the random-WK-induced timing fluctuations of CMOS inverter circuits. We find that the WKF results in 10% variation in timing using the method presented in this study; in contrast, a 5% variation is obtained using the AWKF method. Furthermore, a random-WK-induced 12% fluctuation in the power consumption is observed.

This paper is organized as follows. In §2, we briefly describe the simulation procedure. In §3, we compare the σV_{th} and gate capacitance fluctuations (σC_{G}) of the studied 16 nm devices between the AWKF and our methods. The random-WK-induced characteristic fluctuation of a CMOS inverter circuit is also explored. Finally, we draw the conclusion and suggest future works in §4.

2. Simulation Technique

The control N-MOSFET used is a 16 nm device (device width: 16 nm) with amorphous-based titanium nitride/hafnium oxide gate stacks with a 4.52 eV effective work function and an effective oxide thickness (EOT) of 0.8 nm. Instead of using tungsten nitride and molybdenum nitride as gate materials of the P-MOSFET used, a titanium nitride gate with a 4.76 eV effective work function is simulated, which could be achieved by aluminum (Al) incorporation.[30] Owing to this, the work function is tuned by the dipole formation of the hafnium oxide/oxide interface; the Al incorporation will give a fixed offset of the work function. The adopted material properties, and device settings and characteristics are respectively listed in Tables I, II and III. Unlike in the AWKF method, we directly partition the region of the devices' metal gate into many subregions according to the experimentally observed grain size.[31] Then, we randomly generate WKs for each subregion according to the material properties and map them into the devices' gate for the experimentally calibrated 3D device simulation,[6,7] as shown in Fig. 1(a), where approximately two hundred statistically random devices are generated to examine random-WK-induced fluctuations.

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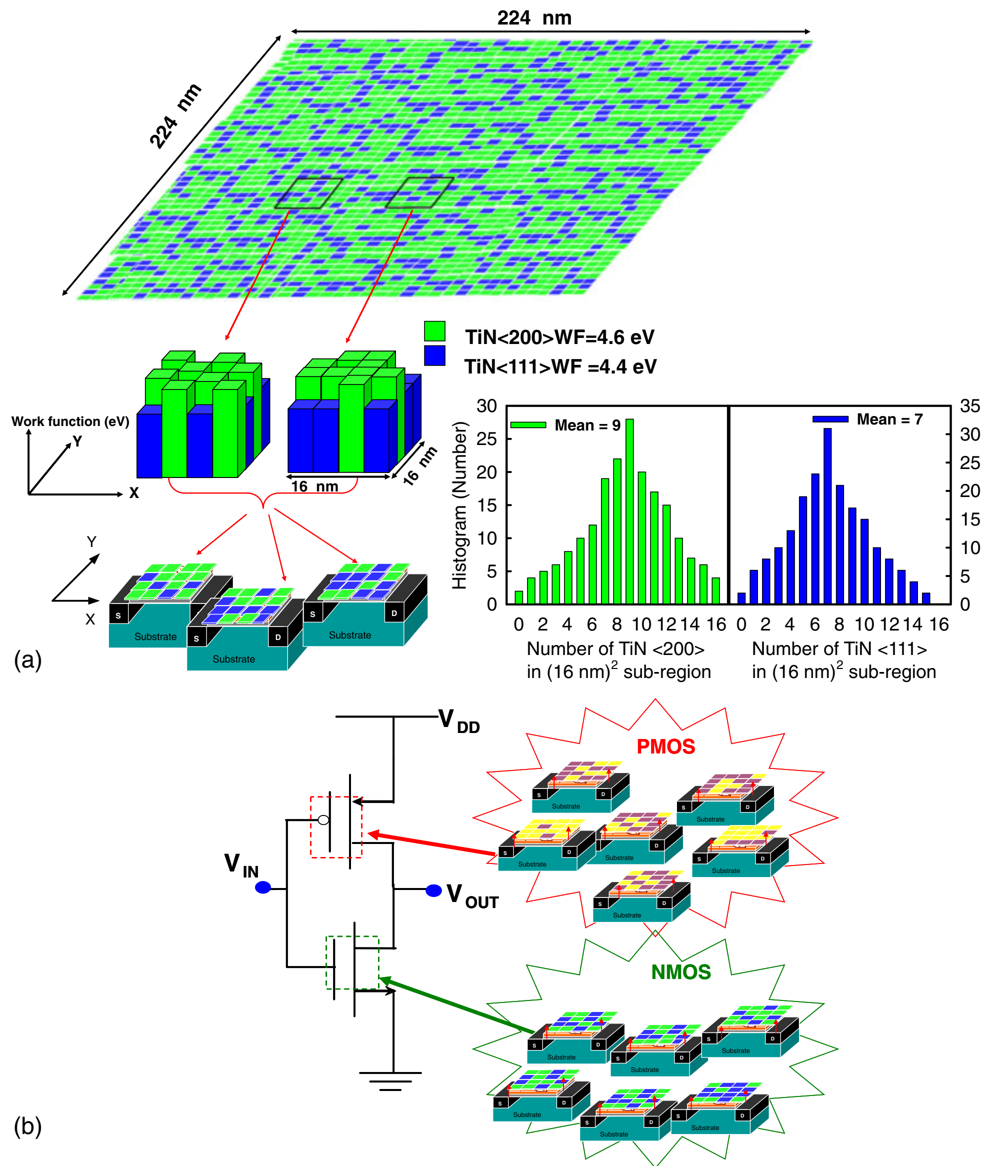

Fig. 1. (Color online) (a) 3136 metal grains are randomly generated in a large area of $224 \times 224\,\text{nm}^2$, where the size of each metal grain is $4 \times 4\,\text{nm}^2$ and only two orientations, ⟨200⟩ and ⟨111⟩, are considered. The histograms show the distribution of the number of grains generated for orientations TiN⟨200⟩ and TiN⟨111⟩, where the means are nine and seven, respectively. (b) The generated N- and P-MOSFETs of the orientations TiN⟨111⟩ and TiN⟨200⟩ are mapped into an inverter circuit.

Table I. Metal properties used in this work.

	N-MOSFET		P-MOSFET	
Grain orientation of material	TiN⟨200⟩	TiN⟨111⟩	TiN⟨200⟩+Al	TiN⟨111⟩+Al
Probability (%)	60	40	60	40
Work function (eV)	4.6	4.4	4.84	4.64
Effective work function (eV)	4.52		4.76	

Table II. Device parameter settings used in this work.

Channel doping (cm^{-3})	1.5×10^{18}
S/D doping (cm^{-3})	2×10^{20}
LDD doping (cm^{-3})	4×10^{19}
Work function (eV)	4.52 (N-MOSFET), 4.76 (P-MOSFET)
Oxide thickness (nm)	EOT = 0.8
Junction depth	8 nm to maintain the subthreshold leakage

Table III. The list of device performance following ITRS for low-operating-power (LOP) applications.

	Performance (For LOP)			
	V_t (mV)	I_{on} (μA/μm)	I_{off} (nA/μm)	SS (mV/dec)
N-MOSFET	250	521	200	147
P-MOSFET	−250	390	198	149

To estimate the circuit properties, the device characteristics in the case of the tested inverter circuit are first calculated by 3D device simulation. The obtained result is then used as initial guesses in the coupled device-circuit simulation.[7] The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are solved simulta-

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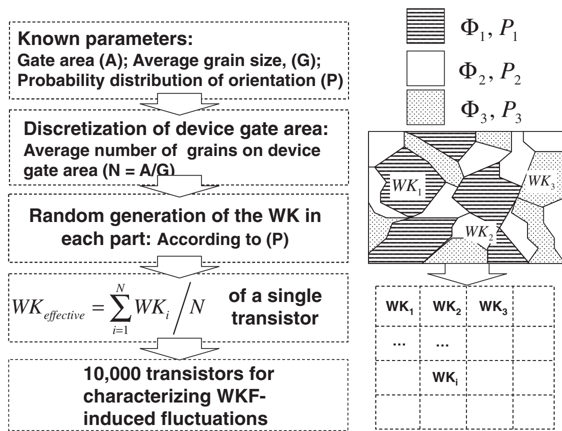
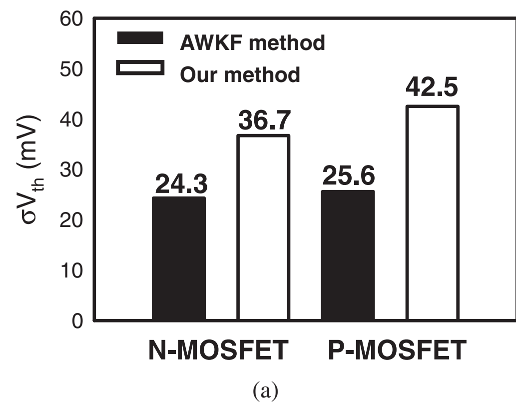


Fig. 2. Flowchart of AWKF method and schematic of a metal gate consisting of grains with three different orientations, where the different work function values are Φ_1, Φ_2, and Φ_3 and the occurrence probabilities are P_1, P_2, and P_3, respectively.



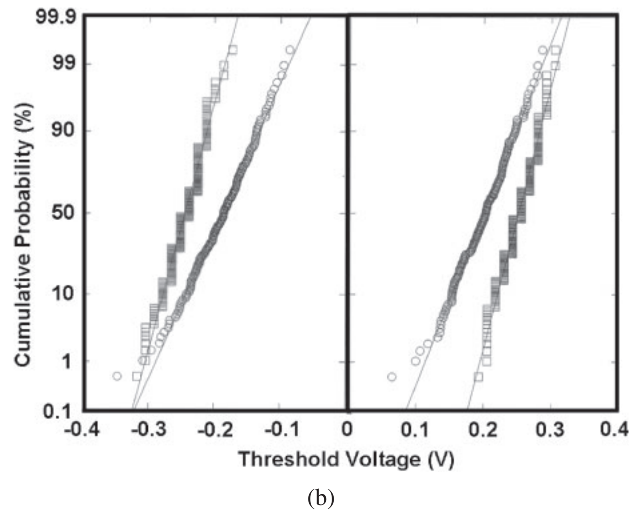


Fig. 3. (a) $\sigma V_{\rm th}$'s calculated by using AWKF method and our method for N- and P-MOSFETs, respectively. Cumulative probability plot of $V_{\rm th}$ for (b) N- and P-MOSFETs, where the open circle and square symbols denote results obtained by our method and the AWKF method; the straight line fit indicates the randomness of variation.

neously to obtain the circuit characteristics. We notice that the device characteristics obtained by device simulation, such as the distributions of potential and current densities, are input in the circuit simulation through device contacts. The coupled device-circuit simulation is illustrated in Fig. 1(b). In the AWKF method,[7,27] as shown in Fig. 2, the Monte Carlo approach is implemented for examining such an effect. Each grain orientation has a different work function; therefore, the gate work function is a probabilistic distribution rather than a deterministic value. First, the gate area is partitioned into several parts according to average grain size. Then, the grain orientation of each part and the total gate work function are randomly generated on the basis of the properties of the metal. The work function of each partitioned area (WK_i) is a random value. The summation of WK_i is then averaged to obtain the effective work function of the transistor and used for WKF-induced $\sigma V_{\rm th}$ estimation. We note that the method presented in this study has different WKs but that the AWKF only has an averaged work function value in the gate region.

3. Results and Discussion

Figure 3(a) shows that the random-WK-induced $\sigma V_{\rm th}$ values of the 16 nm N- and P-MOSFETs are 1.5 and 1.6 times higher than the results of the AWKF method. Owing to the P-MOSFET having a relatively high metal resistivity, the $\sigma V_{\rm th}$ of the P-MOSFET is higher than that of the N-MOSFET. Therefore, the metal gate work function of the P-MOSFET tuned by Al incorporation will result in a lower metal resistivity and may decrease the control of the channel surface potential, which will result in a slightly higher $\sigma V_{\rm th}$. The $V_{\rm th}$ distribution is evaluated under a constant current (10^{-7} A). Figure 3(b) shows the typical cumulative probability plots for N- and P-MOSFETs, which indicate the distribution is statistically random for our method. The open circle and square symbols denote data for our method and the AWKF method, respectively. The AWKF method shows a smaller $V_{\rm th}$ fluctuation than our method owing to the recurring work function, as shown in Fig. 3(b). As shown in Fig. 4(a), we know that the $\sigma V_{\rm th}$ is a function of the number of TiN⟨111⟩ orientation (lower work function). As the number of TiN⟨111⟩ orientation decreases, the effective WK of a single device increases, resulting in a low $V_{\rm th}$. We also find that, even for devices with the same number of TiN⟨111⟩ orientation inside the gate, the difference in nanosized grain position induces different characteristics fluctuations. For example, Figs. 4(b) and 4(c) show the distributions of off-state channel surface potential with the same number of TiN⟨111⟩ orientation on the metal gate. However, the potential distributions are different owing to different locations of TiN⟨111⟩ orientation on the gate area, where the threshold voltages in these two cases are 269 and 196 mV, respectively.

Figure 5(a) shows the fluctuated gate capacitance–gate voltage ($C_{\rm G}$–$V_{\rm G}$) curves obtained by the AWKF method and the simulation method of this work, where the red line denotes the nominal case. The results show that the $\sigma C_{\rm G}$ calculated by the method presented in this work is about 3.5 times higher than that obtained by the AWKF method owing to the effect of random position, especially for devices operating at high gate voltages. To account for the effect of random position, two cases are further chosen randomly, as shown in the zoom-in $C_{\rm G}$–$V_{\rm G}$ plot in Fig. 5(b). Figure 5(c) shows that the effect of random position influences the charge distribution of the inversion layer, which results in a

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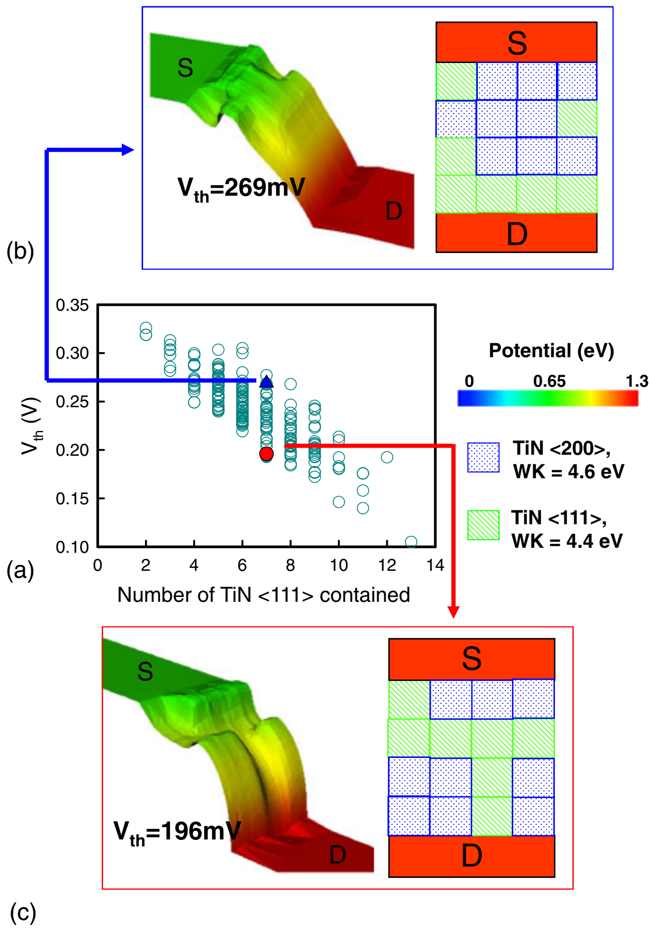

Fig. 4. (Color online) (a) Threshold voltage vs the number of TiN⟨111⟩ orientation in (16 nm)^2, where $V_G = V_S = 0$ V and $V_D = 0.8$ V. For the same number of TiN⟨111⟩ orientation, the potential distributions of device with different positions of TiN⟨111⟩ orientation resulting in (b) high and (c) low threshold voltages.

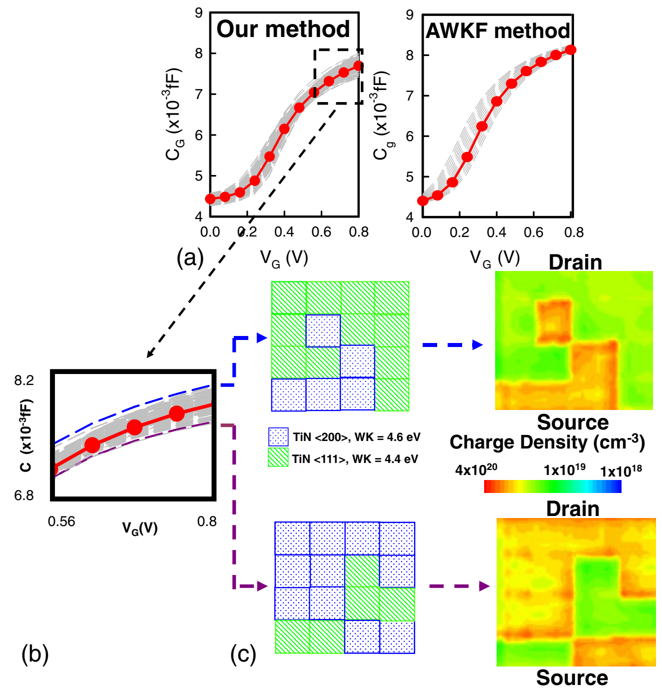

Fig. 5. (Color online) (a) Fluctuated gate capacitance (C_G) curves vs the gate voltage (V_G) calculated by the AWKF method and our method. (b) Zoom-in C_G–V_G plot for devices operating on large V_G. (c) Corresponding surface charge distributions of the largest and smallest gate capacitances for devices under strong inversion ($V_G = 0.8$ V), as shown in (b).

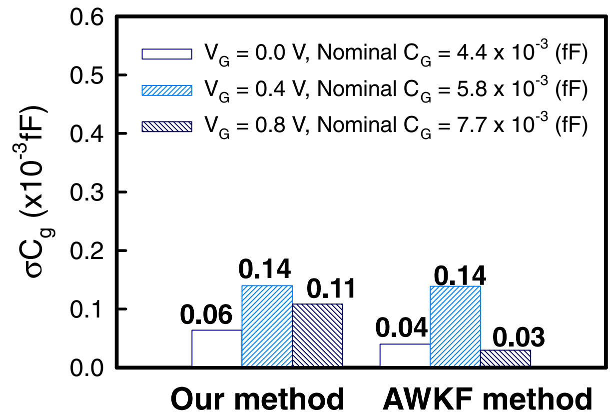

Fig. 6. (Color online) Summarized values of the random WK fluctuated C_G, which is calculated by the AWKF method and our method for N- and P-MOSFETs.

relatively large C_G fluctuation, compared with the result of the AWKF method. The calculated σC_G versus gate bias is shown in Fig. 6. At a zero gate bias, the accumulation layer screens the impact of WKF. Additionally, at $V_G = 0.8$ V, the total gate capacitance decreases owing to the increase in the area of the depletion region. Therefore, the associated σC_G is small. This implies that the capacitive response is dominated by the increment of inversion. Note that the highest fluctuation occurs at $V_G = 0.4$ V, which is less than 3% of the nominal value (= 0.14/5.8) and indicates that the WKF has less effect on σC_G.

Next, the dynamic property of the 16 nm CMOS inverter circuit, as shown in Fig. 1(b), is determined by performing coupled device-circuit simulation.[7] Figure 7 shows plots of the input (upper plot) and output (lower plot) signals of the inverter, where the effective WKs in the nominal case (red solid line) are 4.52 and 4.76 eV for N- and P-MOSFETs, respectively, and the dashed lines show those in fluctuated cases. The rise time (t_r), fall time (t_f), and hold time of the input signal are 2, 2, and 30 ps, respectively. Figures 7(b) and 7(c) show zoom-in plots of the t_f and t_r of the output signal, where t_f and t_r are calculated from the output voltage (V_{out}) falling from 90% of the logic "1" level to 10% of the logic "1" level and that rising from 10% of the logic "1" level to 90% of the logic "1" level, respectively. The low-to-high delay time (t_{LH}) and high-to-low delay time (t_{HL}) are defined as the differences between the times of the 50% points of the input and output signals during the rising and falling of the output signal, respectively. For the high-to-low and low-to-high transitions, on-state N- and P-MOSFETs start to discharge load capacitance. Therefore, the fluctuations are determined by the σV_{th}'s of N- and P-MOSFETs. In our 3D simulation, the fluctuating t_f ($0.076/0.8 \times 100\% = 10\%$), t_{HL} ($0.093/1.25 \times 100\% = 7\%$), t_r ($0.131/1.04 \times 100\% = 13\%$), and t_{LH} ($0.165/1.45 \times 100\% = 11\%$) induced by WKF are about 10% of their respective nominal values, as listed in Table IV, where the t_f, t_{HL}, t_r, and t_{LH}

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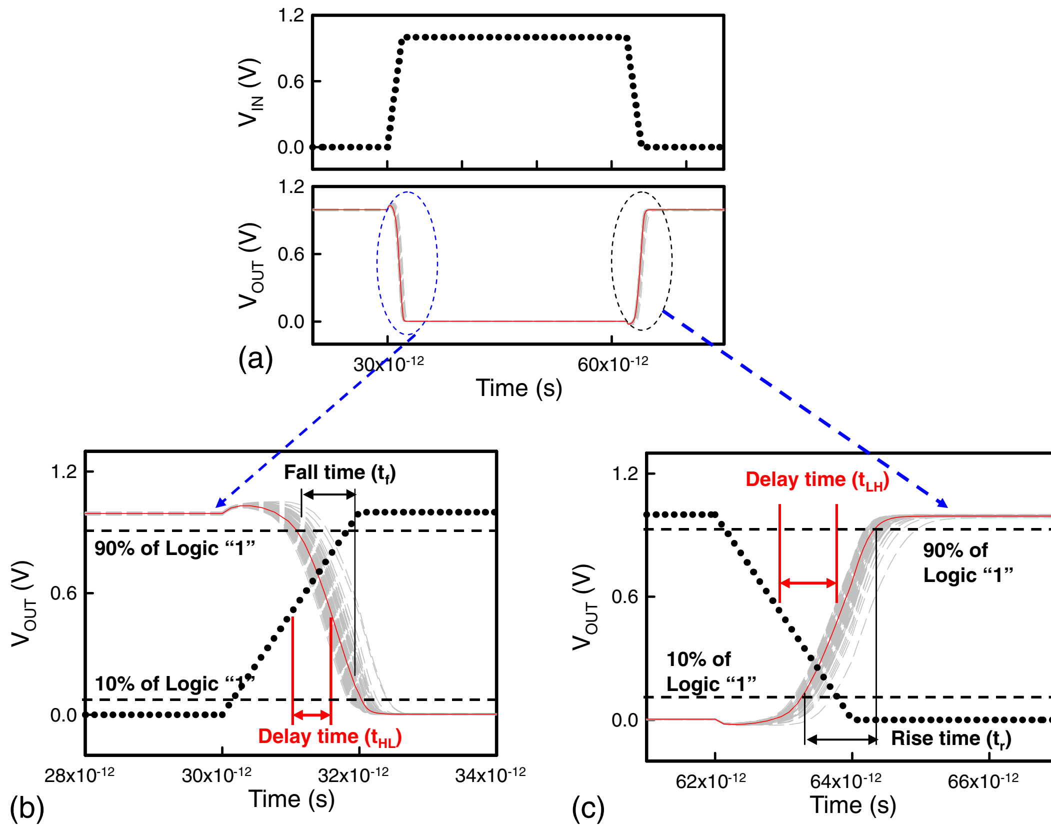

Fig. 7. (Color online) (a) Plots of input and output signals of inverter. The enlarged plots show the random WK fluctuated (b) falling (c) and rising transitions of the output signal, where the rise time, fall time, high-to-low delay time, and low-to-high delay time are indicated in the plots.

Table IV. Summary of nominal values and timing (rise time, fall time, high-to-low delay time, and low-to-high delay time) fluctuations calculated by AWKF method and our method.

	Nominal value (ps)		Timing fluctuation (ps)	
	AWKF method	Our method	AWKF method	Our method
t_f	0.8	0.8	0.018	0.076
t_{HL}	1.25	1.25	0.056	0.093
t_r	1.04	1.04	0.078	0.131
t_{LH}	1.45	1.45	0.076	0.165

Table V. Summary of nominal values and power (dynamic power, short circuit power, static power, and total power) fluctuations.

	Nominal value (nW)		Power fluctuation (nW)	
	AWKF method	Our method	AWKF method	Our method
P_{dyn}	21	21	0.56	0.62
P_{sc}	19	19	2.13	3.56
P_{stat}	5	5	2.61	3.74
P_{total}	45	45	3.42	5.20

in the nominal case are 0.8, 1.25, 1.04, and 1.45 ps, respectively. However, the fluctuations calculated by the AWKF method are underestimated, where the fluctuated t_f ($0.018/0.8 \times 100\% = 2\%$), t_{HL} ($0.056/1.25 \times 100\% = 4\%$), t_r ($0.078/1.04 \times 100\% = 8\%$), and t_{LH} ($0.076/1.45 \times 100\% = 5\%$) induced by WKF are about 5% of their respective nominal values.

We further estimate the power dissipation for the studied 16 nm CMOS inverter. Total power (P_{total}) is defined as the sum of the dynamic power (P_{dyn}), short circuit power (P_{sc}), and static power (P_{stat}), defined as below, where the estimated nominal values are 21, 19, and 5 nW, respectively:

$$P_{dyn} = C_{load} V_{dd}^2 f_{0\to 1}, \tag{1}$$

$$P_{sc} = f_{0\to 1} V_{DD} \int_T I_{SC}(\tau)\, d\tau, \tag{2}$$

$$P_{stat} = V_{DD} I_{leakage}. \tag{3}$$

$f_{0\to 1}$ is the clock rate (15 GHz). I_{sc} is the short circuit current, which is observed as both N- and P-MOSFETs are turned on resulting in a DC path between the power rails. T is the switching period. $I_{leakage}$ is the leakage current when operating in the static state, where P_{dyn} is determined by the load capacitance, P_{sc} is determined by the time of the existence of the DC path between the power rails and the short circuit current, and P_{stat} is determined by the production of the applied voltage and leakage current of the inverter. After calibrating the V_{th} of the device, P_{sc} is then determined by I_{sc} owing to its dependence on the saturation current of the device. In the nominal case, P_{dyn} (21 nW) and P_{sc} (19 nW) are the dominant factors in power dissipation. Table V shows the dynamic power fluctuations (σP_{dyn}), short circuit power fluctuations (σP_{sc}), static power fluctuations (σP_{stat}), and the total power fluctuations ($\sigma P_{total} = [(\sigma P_{dyn})^2 + (\sigma P_{sc})^2 + (\sigma P_{stat})^2]^{0.5}$) calculated by our 3D simulation method. Here, to estimate each power dissipation's fluctuation, we simply assume that these three powers are statistically independent of each other, so that the fluctuation of the total power consumption could be

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approximated by the square root of the sum of the squares of the three power fluctuations. However, this approximation should be subjected to further correction for more accurate calculation. The AWKF shows a weaker effect owing to the small gate capacitance fluctuations in σP_{dyn}. Differently from the results of σP_{dyn}, the AWKF starts to play an important role in P_{sc} because of the significant σV_{th} induced by WKF in the device. Although P_{stat} is not an important part in P_{total}, σP_{stat} is the largest term in σP_{total} owing to the exponential relationship between the leakage current and V_{th}. The σP_{total}'s calculated by the AWKF method and our method are 3.42 and 5.20 nW, which are about 7.6% ($\sigma P_{total}/P_{total} \times 100\% = 3.42/45 \times 100\%$) and 12% ($\sigma P_{total}/P_{total} \times 100\% = 5.2/45 \times 100\%$) of the power consumption, respectively. We note that the result of our method is larger than that of the AWKF method because the random number and position of nanosized metal grains are considered in our approach.

4. Conclusions

In this work, we have examined the WKF using full 3D device simulation of high-κ/metal gate technology. This approach considers the effect of the local crystal orientation of nanosized metal grains, differently from the recently reported AWKF method.[27] Estimation using the AWKF method might underestimate WKF because it does not consider the random position of metal grains in the calculation. The WKF-induced σV_{th} and σC_G of CMOS devices including the fluctuations in the timing and power of the CMOS inverter circuit were studied. We are currently studying suppression techniques for WKF.

Acknowledgments

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1) G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov: IEEE Trans. Electron Devices **53** (2006) 3063.
2) K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto, and C. Hu: IEEE Trans. Electron Devices **45** (1998) 809.
3) K.-F. Lee, Y. Li, and C.-H. Hwang: Semicond. Sci. Technol. **25** (2010) 045006.
4) Y. Li and C.-H. Hwang: J. Appl. Phys. **102** (2007) 084509.
5) Y. Li and C.-H. Hwang: IEEE Trans. Microwave Theory Tech. **56** (2008) 2726.
6) Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang: IEEE Trans. Electron Devices **55** (2008) 1449.
7) Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han: IEEE Trans. Electron Devices **57** (2010) 437.
8) T. Tsunomura, A. Nishida, and T. Hiramoto: Jpn. J. Appl. Phys. **49** (2010) 054101.
9) P. Francis, A. Terao, and D. Flandre: IEEE Trans. Electron Devices **41** (1994) 715.
10) X.-H. Tang, V. K. De, and J. D. Meindl: IEEE Trans. VLSI Syst. **5** (1997) 369.
11) K. Takeuchi, T. Tatsumi, and A. Furukawa: IEDM Tech. Dig., 1997, p. 841.
12) P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen: IEEE Trans. Electron Devices **45** (1998) 1960.
13) A. Asenov: IEEE Trans. Electron Devices **45** (1998) 2505.
14) W. J. Gross, D. Vasileska, and D. K. Ferry: IEEE Electron Device Lett. **20** (1999) 463.
15) A. Asenov and S. Saini: IEEE Trans. Electron Devices **46** (1999) 1718.
16) Y. Yasuda, M. Takamiya, and T. Hiramoto: IEEE Trans. Electron Devices **47** (2000) 1838.
17) N. Sano and M. Tomizawa: Appl. Phys. Lett. **79** (2001) 2267.
18) Y. Li and S.-M. Yu: Jpn. J. Appl. Phys. **45** (2006) 6860.
19) Y. Li and C.-H. Hwang: J. Appl. Phys. **102** (2007) 084509.
20) Y. Li, C.-H. Hwang, and H.-W. Cheng: Jpn. J. Appl. Phys. **47** (2008) 2580.
21) Y. Li and S.-M. Yu: IEEE Trans. Semicond. Manuf. **20** (2007) 432.
22) A. Brown and A. Asenov: J. Comput. Electron. **7** (2008) 124.
23) Y. Li, C.-H. Hwang, and H.-W. Cheng: Microelectron. Eng. **86** (2009) 277.
24) J. Fujiki, N. Yasuda, R. Fujitsuka, W. Sakamoto, and K. Muraoka: IEDM Tech. Dig., 2009, p. 952.
25) K. Ohmori, T. Matsuki, D. Ishikawa, T. Morooka, T. Aminaka, Y. Sugita, T. Chikyow, K. Shiraishi, Y. Nara, and K. Yamada: IEDM Tech. Dig., 2008, p. 409.
26) H. Dadgour, K. Endo, V. De, and K. Banerjee: IEDM Tech. Dig., 2008, p. 705.
27) H. Dadgour, V. De, and K. Banerjee: IEEE Int. Conf. Computer-Aided Design, 2008, p. 270.
28) T. Matsukawa, S. O'uchi, K. Endo, Y. Ishikawa, H. Yamauchi, Y. X. Liu, J. Tsukada, K. Sakamoto, and M. Masahara: IEEE Symp. VLSI Technology Tech. Dig., 2009, p. 118.
29) P. Majhi, C. Young, G. Bersuker, H.-C. Wen, G. A. Brown, B. Foran, R. Choi, P. M. Zeitzoff, and H. R. Huff: Euro. Solid-State Device Research Conf., 2004, p. 185.
30) H.-C. Wen, S. C. Song, C. S. Park, C. Burham, G. Bersuker, K. Choi, M. A. Quevedo-Lopez, B. S. Ju, H. N. Alshareef, H. Niimi, H. B. Park, P. S. Lysaght, P. Majhi, B. H. Lee, and R. Jammy: IEEE Symp. VLSI Technology Tech. Dig., 2007, p. 160.
31) M. Sato, S. Kamiyama, Y. Sugita, T. Matsuki, T. Morooka, T. Suzuki, K. Shiraishi, K. Yamabe, K. Ohmori, K. Yamada, J. Yugami, K. Ikeda, and Y. Ohji: IEDM Tech. Dig., 2008, p. 119.

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