行政院國家科學委員會專題研究計畫　成果報告

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計畫類別：整合型計畫
計畫編號：NSC94-2215-E-009-052-
執行期間：94 年 08 月 01 日至 95 年 07 月 31 日
執行單位：國立交通大學電機與控制工程學系(所)

計畫主持人：蘇朝琴

計畫參與人員：林柏成

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智慧型混合信號感測電路設計

計畫類別：☐ 個別型計畫　☑ 整合型計畫
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共同主持人：無
計畫參與人員：林柏成

成果報告類型(依經費核定清單規定繳交)：☑精簡報告　☐完整報告

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執行單位：國立交通大學電機與控制工程學系

中　華　民　國　95　年　7　月　14　日

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***Abstract* –This paper presented an inverter based 3rd order sigma-delta ADC. Cascode structure and auto-zeroing mechanism are proposed for the gain enhancement and offset cancellation. The ADC has been implemented in TSMC 2P6M 0.18μm CMOS technology with a core area of 0.54mm^2. The measurement results show that for the 1-V supply, 20-KHz bandwidth, and 2-MHz sampling rate, the power consumption is 42μW and the dynamic range of 66.02dB.**

I Introduction

For an aging society of the next decade, health and environmental monitoring devices are forecasted to be the next killer applications. In order to be portable, batter-powered and long lasting, the power consumption is required to be less than 1mW. For this, *analog-to-digital converters* (ADC) require special consideration because it bridging the analog part of the sensing devices and the digital part of the processing unit.

Over the last years, due to its versatile architecture, *sigma-delta* (ΣΔ) ADC has developed into a wide rage of performance aspects for varies applications. It is able to achieve a *dynamic range* (DR) of over 100dB for high-fidelity audio and instrumentation applications [1]. For wireless communications, over 10-bit resolution and 10-MHz sampling rate is also achievable with reasonable power consumption [2]. For sensors and portable applications, power in μW range can be achieved using simple system architecture [4~9].

For low-power ΣΔ ADC, the operational amplifier is the key component. It dominates the performance and requires more design efforts than other part of the circuits. In this paper, we propose a very simple amplifier structure, a cascode inverter. With which, the design effort can be minimized and power consumption can be reduced. Of course, such a simple structure is not without drawbacks. The offset voltage is a major one. For this, a simple auto-zeroing technique is proposed to nullify the offset.

In the rest of the paper, the system architecture is outlined in Section II, the circuit structure is studied in Section III, the chip implementation and measurement results are presented in Section IV, and the conclusions are given in Section V.

II. System Architecture

For low power design, the system architecture and circuit structure must be as simple as possible to reduce overall circuit area and stray capacitance. Figure 1 shows a single-loop multi-feedback ΣΔ modulator. Here, $I(z)=z^{-1}/1-z^{-1}$ is the integrator and a_i is its coefficient. As compared to the MASH (Multi-stAge noise SHaping) structure, it has a much simpler

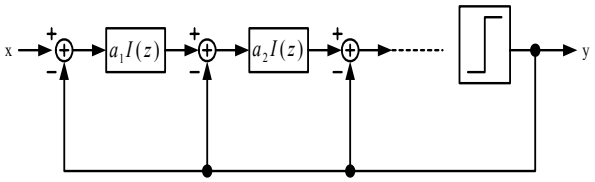

Figure 1, System architecture of a single-loop ΣΔ modulator

circuit structure. It may suffer from the stability problem when the order is high. However, the stability can also be guaranteed by selecting the coefficient carefully, using the following procedure. The noise transfer function of the ΣΔ modulator is as follows [3].

$$N_{TF}=\frac{1}{1+\sum_{i=1}^{n}\prod_{j=i}^{n}a_j\cdot k\cdot\left(\frac{z^{-1}}{1-z^{-1}}\right)^{n-i+1}} \tag{1}$$

Here, n is the order and k is the gain of the quantizer. The amplitude of the noise transfer function can be approximated by

$$\left|N_{TF}\right|\approx\frac{\left|1-z^{-1}\right|^n}{\prod_{i=i}^{n}a_i\cdot k}=\frac{\left|2\sin(\pi f/f_S)\right|^n}{\prod_{i=i}^{n}a_i\cdot k}. \tag{2}$$

So, the noise energy can be derived as

$$P_Q=\left(\frac{\Delta}{2}\right)^2\cdot\frac{1}{3\pi(2n+1)\left(\prod_{i=i}^{n}a_i\cdot k\right)^2}\cdot\left(\frac{\pi}{OSR}\right)^{2n+1}. \tag{3}$$

As a result, the *signal-to-noise ratio* (SNR) is calculated as

$$SNR=\frac{3\pi}{2}\cdot(2n+1)\cdot\left(\prod_{i=i}^{n}a_i\cdot k\right)^2\cdot\left(\frac{OSR}{\pi}\right)^{2n+1}. \tag{4}$$

From (4), we learn that we are able to improve the SNR by increasing the coefficient a_i. However, it becomes unstable when a_i is too large. To be stable, $\max_{\omega}\left|N_{TF}\left(e^{j\omega}\right)\right|<1.5$. Therefore, to have high SNR yet guarantee the stability, the coefficients are bounded by [3]

$$\prod_{i=i}^{n}a_i\cdot k=1,\quad \text{n}=2,3,4. \tag{5}$$

In this design, behavioral simulation is conducted to chose (0.2, 0.4, 0.4) as the coefficient for the proposed 3rd order ΣΔ modulator. The noise and signal transfer functions are

$$N_{TF}(z)=\frac{(z-1)^3}{(z-0.7409)(z^2-1.859z+0.9826)}. \tag{6}$$

$$S_{TF}(z)=\frac{0.032}{(z-0.7409)(z^2-1.859z+0.9826)}. \tag{7}$$

Under the *over sampling rate* (OSR) of 128, it has a theoretical SNR of 96dB and a DR of 102dB. The three poles, located at (0.7409+j0), (0.9295+j0.3444), and (0.9295-j0.3444), are all inside the *region of convergence* (ROC). The stability is guaranteed. Although one is able to move the zero closer to the pole to improve the SNR. However, the hardware overhead can be large because an additional feedback loop is required. As a result, the (0.2, 0.4, 0.4) is selected as the system parameters.

III. Circuit Structure

Inverter Amplifier

The basic building block of a ΣΔ ADC is the *switched-capacitor* (SC) integrator. Of which, the core module is an *operational amplifier* (OPAmp). It is the decisive factor for power consumption. The OPAmp structure is selected according to the performance requirement. For power in micro watt range, operating in subthreshold or weak inversion region may be desirable. However, process variation may create many uncertainties. Considering the overhead and power consumption, inverter based amplifier is considered.

Figure 2 shows a conventional inverter amplifier (left) and the proposed one (right). An inverter can be regarded as a push-pull class AB amplifier. Area and power efficiency are high. Its gain can be derived as

$$|A_v| = (g_{m1} + g_{m2})(r_{o1} // r_{o2}). \quad (8)$$

It is difficult to achieve high gain and bandwidth at the same time. Note that, the unit-gain bandwidth is linearly proportional to I_D (biasing current); while the gain is proportional to the inverse of the square-root of I_D. It is difficult to obtain sufficient high gain for the SC applications. Therefore, certain modification is desirable. The proposed amplifier is shown in Figure 2. It is a cascode amplifier, the gain is boosted to

$$|A_v| = (g_{m1} + g_{m2})(g_{m1} \cdot r_{o1} \cdot r_{o3} // g_{m2} \cdot r_{o2} \cdot r_{o4}). \quad (9)$$

Auto Zeroed SC Integrator

The major concern for using inverter as amplifier is the DC offset due to the mismatch of the push (N) and pull (P) devices. Therefore, an auto-zeroed SC integrator is proposed in Figure 3.

In ϕ_1, C_1 is charged with $Q_{C1} = C_1(V_{in} - V_{os})$. Here, V_{OS} is the offset voltage. In ϕ_2, C_1 is charged with $Q_{C1} = -C_1 V_{os}$. As a result, the charge being transferred to C_2 is . $\Delta Q_{C1} = -C_1 V_{in}$, which is independent of V_{OS}. Note that, S4 and S5 are for the reduction of clock feed-through.

1-bit Quantizer

Figure 4 shows the quantizer within a 1st order ΣΔ ADC. It includes a preamplifier and a 1-bit quantizer. The quantizer is composed of a dynamic comparator and an SR latch, as shown in Figure 5.

$\overline{\phi 2a}$ is a precharge phase for M3a and M3b to precharge the data lines. After $\overline{\phi 2a}$ transits from low to high, M2a and M2b are turned on, M1a and M1b compare the input data. The remaining transistors serve as an SR latch. Note that, the phase of $\overline{\phi 2a}$ is a little ahead of ϕ_2 in order to prevent clock feed through.

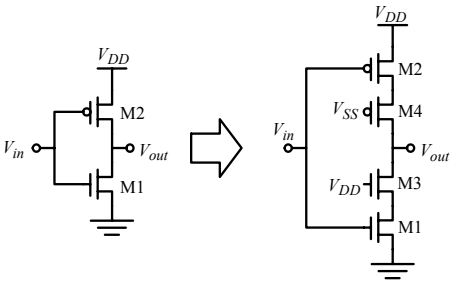

Figure 2, Inverter amplifiers

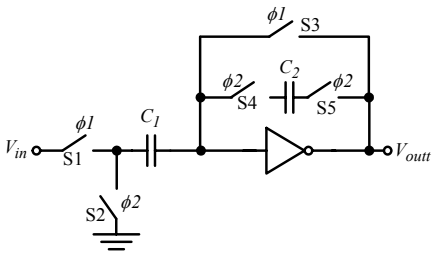

Figure 3, Auto-zeroed SC integrator

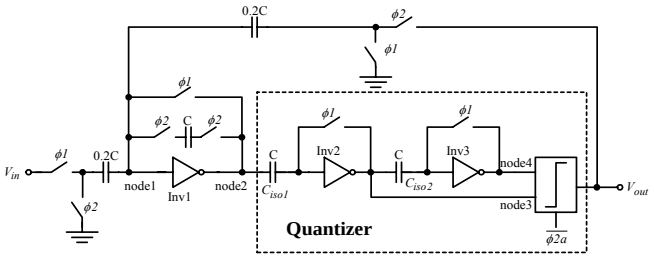

Figure 4, The quantizer in a 1st order ΣΔ ADC.

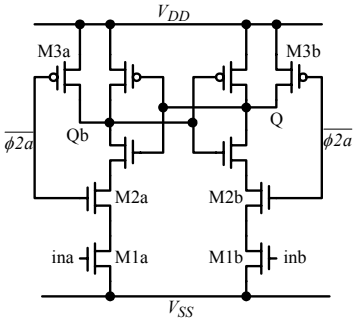

Figure 5, The quantizer circuit diragram.

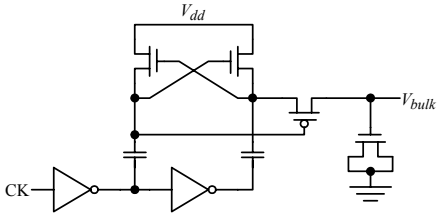

Figure 6, The clock bootstrap circuit.

Clock Bootstrap

Due to that 1-V power supply is insufficient to turn on the

switches completely, a bootstrap circuit is used to raise the voltage level of the clock. Figure 6 shows the bootstrap circuit. It is able to raise the clock level to 1.8V.

Overall Circuits

The overall circuit is shown in Figure 7 . It is a 3rd order single-loop multi-feedback ΣΔ ADC. Figure 8 shows the simulation results its *power spectrum density* (PSD) for 2-MHz sampling rate, 3.9-KHz sinusoidal waveform, and 0.35-V amplitude. Figure 9 shows the SNR and SNDR (*signal to noise and distortion ratio*) under different input amplitudes. The simulation results shown that the peak SNR is 75.74dB, the peak SNDR is 69.01dB, and DR is 76.61dB.

IV Chip Implementation and Measurement

The proposed inverter based 3rd ΣΔ ADC has been implemented using TSMC 0.18μm 2P6M CMOS process. Figure 10 shows the die photo. The chip has been measured using an audio precision analyzer and a logic analyzer. The sampled data is transferred to a host computer and analyzed by the MATLab software. Figure 11 and 12 shows the PSD and SNR/SNDR under the same condition as that for Figure 8 and 9. The measured SNR is 65.87dB, the SNDR is 61.96dB, and the DR is 66.02dB. The *effective number of bits* (ENoB) is 10 bits.

Table 1 shows the chip summary and comparison. The difference is about 10dB. The major source of the difference is the noise in the printed circuit board environment. The noise floor in the simulation environment (Figure 8) is -100dB; while it is -90dB (Figure 101) in the measurement setup. Because of this, we believe that through more careful test board design, the performance can be improved significantly. Table 2 shows measured results under different sampling frequency (SF). It shows that the chip have an ENoB of 8/7 bits under 4/8-MHz sampling rate.

Table 1, Chip summary and comparison

Specification	Simulation	Measurement
Dynamic Range	76.61dB	66.02dB
Peak SNR	75.74dB	65.87dB
Peak SNDR	69.01dB	61.96dB
Power Consumption	40μW	42μW
Signal Bandwidth	20k Hz	
Sampling Frequency	2M Hz	
Supply Voltage	1V	
Chip/Core Size	$0.99\times0.99\,/\,0.73\times0.74\ mm^2$	
Technology	0.18μm	

Table 2, Measured results under 2/4/8-MHz sampling rate.

SF	BW	SNR	SNDR	DR
2MHz	20kHz	65.87dB	61.96dB	66.02dB
	40kHz	57.13dB	53.82dB	58.06dB
4 MHz	20kHz	63.56dB	54.61dB	64.37dB
	40kHz	58.03dB	54.25dB	59.12dB
8 MHz	20kHz	55.93dB	42.23dB	56.67dB
	40kHz	52.39dB	41.95dB	53.28dB

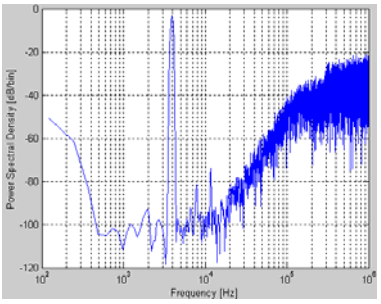

Figure 8, The simulated PSD

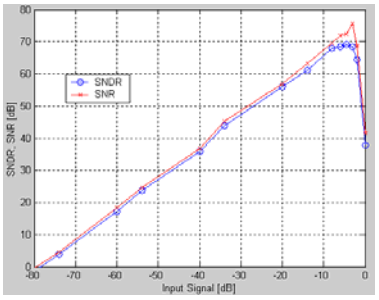

Figure 9, The simulated SNR and SNDR v.s. input amplitude.

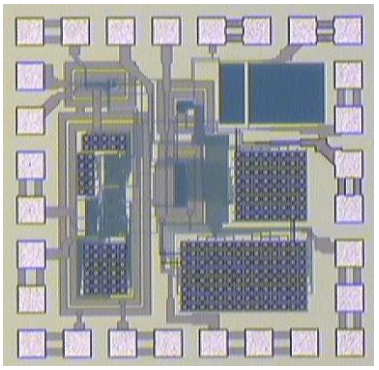

Figure 10, The die photo.

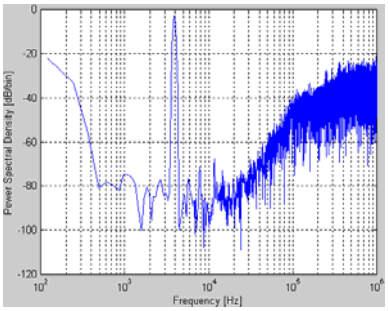

Figure 11, The measured PSD

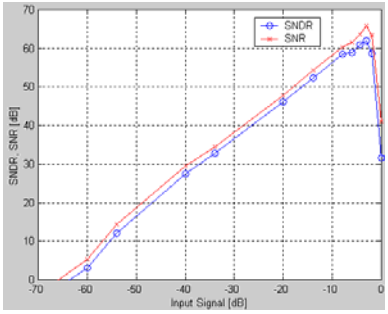

Figure 12, The measured SNR and SNDR v.s. input amplitude

In order to compare to other designs, a *figure of merit* (FOM) need to be defined. Because the area is technology dependent, we only consider resolution, bandwidth, and power. The FOM is defined as follows,

$$FOM = \frac{resolution \times bandwidth}{Power} = \frac{10^{(DR-1.78)/20} \times BW}{P}. \quad (10)$$

The FOM is the same as that defined in [6] except that the area is not considered.

Table 3 shows the FOM comparisons for the sigma-delta modulators of recent years. For the measured performance, this work is the third with less than one third the power consumption, 42μW v.s. 140 μW [4] and 134 μW [5]. In addition, the circuit structure is simple and easy to design.

V Conclusions

This paper has presented an inverter based 3rd order sigma-delta ADC. Two novel techniques are implemented. First, cascode inverters are proposed for the gain enhancement. Second, auto-zeroed integrators are designed to cancel the offset. The simulation results show that the proposed design is able to achieve a DR of 76.6dB at 42-μW under 1-V supply, 20-KHz bandwidth, 2-MHz sampling rate. The chip has been implemented in TSMC 2P6M 0.18μm CMOS technology with a core area of 0.54mm^2. The measured results show that under the same condition, the power consumption is 42μW and the DR is 66.02dB. The 10.6dB difference between the simulated and the measured performance is due to the difference in the noise floor.

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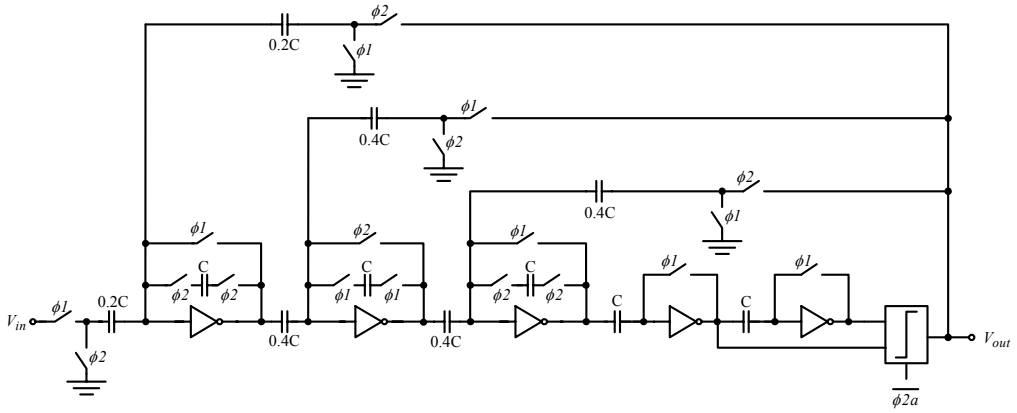

Figure 7, The proposed single-loop multi-feedback 3rd order ΣΔ ADC.

Table 3, The FOM comparisons.

Name & Year	V_{DD}	DR	BW	Power	Area	Process	FOM ($\times 10^9 Hz/W$)
Yao, 2004 [4]	1.0V	88dB	20kHz	140 μW	0.18 mm^2	90 nm CMOS	2916
Gerfers, 2003 [5]	1.5V	80dB	25kHz	135 μ W	-	0.5 μ m CMOS	1525
Sauerbrey, 2002 [6]	0.7V	75dB	8kHz	80 μ W	0.082 mm^2	0.18 μ m CMOS	457
Qunying, 2001 [7]*	1.2V	75dB	3.4kHz	38 μ W	-	0.35 μ m CMOS	408
Gerfers, 2001 [8]	1.5V	75dB	25kHz	230 μ W	1.2 mm^2	0.5 μ m CMOS	496
Dessouky, 2000 [9]	1.0V	88dB	25kHz	950 μ W	0.63 mm^2	0.35 μ m CMOS	537
This Work (Sim.)	**1.0V**	**76.6dB**	**20kHz**	**40 μ W**	**0.54** mm^2	**0.18 μ m CMOS**	**2747**
This Work (Meas.)	**1.0V**	**66.0dB**	**20kHz**	**42 μ W**	**0.54** mm^2	**0.18 μ m CMOS**	**781**