行政院國家科學委員會專題研究計畫　成果報告

利用基於積分方程式之快速電磁解答器實現晶片導線之頻域及時域分析

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計畫主持人：趙學永
共同主持人：陳念偉
計畫參與人員：郭益廷　王義志　方國誌　莊肇堂

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主持人: 趙學永　國立交通大學電信工程系所
共同主持人：陳念偉　國立中央大學電機工程系所
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中文摘要

當積體電路設計進入深次微米及數十億赫茲的時代，導線分析逐漸顯現其重要性。由於半導體元件體積縮小，導線寄生元件所造成的時間延遲遠大於邏輯閘所造成的延遲。此外，當高速數位訊號包含更多的高頻成份時，訊號在導線上傳輸時將會遇到更多的振鈴、反射、及串音等效應。為了正確分析晶片上導線的時域及頻域特性，本計畫發展了基於電場積分方程式的多層介質解答器之數種關鍵技術。其中包含低頻電磁裡多層介質格林函數之電磁分解、萃取複雜結構圈與樹基底函數之快速演算法及寬頻等效電路生成之最佳演算法。

關鍵詞：導線分析、電場積分方程式、圈與樹基底函數分解、寬頻等效電路生成

Abstract

Interconnect analysis becomes increasingly important as IC design enters the deep-submicron and multi-gigahertz era. As device sizes shrink, the time delay due to interconnect parasitics far exceeds the gate delay. Besides, high-speed digital signals encounter more ringing, reflection, and crosstalk as their spectrums consist of more high-frequency components. In order to accurately capture frequency- and time-domain characteristics of on-chip interconnects, we have developed several key technologies for multilayered electromagnetics solvers based on the electric field integral equation, including decomposition of multilayered Green's functions at low frequencies, fast algorithms of loop-tree extraction for complex structures, and optimal algorithms for broadband equivalent circuit generation.

Keywords: Interconnect analysis, integral equation, loop-tree decomposition, broadband equivalent circuit generation

I. Introduction

Integral-equation (IE)-based methods for interconnect analysis are under avid research in recent years. On-shelf commercial tools based on the finite element method (FEM), such as Ansoft HFSS and Q3D, are too computationally expensive for calculating S-parameters or equivalent circuits in whole-chip simulation. Since IE-based methods only involves surface unknowns, the number of unknowns is far less than that of FEM. Therefore, the former is more promising for solving large-scale problems than the latter. However, the superior computational efficiency of the IE-based method is not without cost. The multilayered Green's function involves singular integral in spectral domain and is much harder to be formulated and implemented than the FEM. Besides, the multilayered Green's function becomes unstable when the dimension of the structure is less than one wavelength. The only remedy is to decompose the electric current by loop and tree functions at low frequencies, so the magnetostatic and electrostatic contributions to the field can be captured accurately. Furthermore, the results obtained from frequency-domain EM simulation, such as S-parameters, cannot be readily used in timing analysis of interconnects. Therefore, it is necessary to convert system transfer functions into broadband equivalent circuits, so the net lists can be incorporated seamlessly into SPICE-like circuit simulators.

In this report, we will introduce key accomplishments of the one-year project, including the decomposition of multilayered Green's function at low frequencies, fast algorithms for loop and tree extraction, and an optimal algorithm for broadband equivalent circuit extraction.

II. Decomposition of the Multilayered Green's Function at Low Frequencies

For interconnects embedded in dissimilar dielectric layers, the most efficient way to analyze signal propagation is to apply IE-based methods, such as the method of moments (MoM) with dyadic Green's functions for multilayered media [1]. If we apply the surface integral formulation, currents are assumed to flow on the surface of conductors. Since only surface unknowns are involved, it generally requires less computational resources than volume-unknown based methodsm, such as FEM and finite-difference time-domain (FDTD) method.

The dyadic Green's function can be decomposed into TM and TE contributions [2]. We further separate the divergence-free and non-divergence-free contributions from the TM and TE components to make the integral equation stable at low frequencies.

If both source and observation points are located in the same layer of dielectric materials, the dyadic Green's function has the form

$$\begin{aligned}\bar{\mathbf{G}}^{RWG}(\mathbf{r},\mathbf{r}') = {} & \left(\bar{\mathbf{I}} + \frac{\nabla\nabla}{k_m^2}\right) g_m^{p}(\mathbf{r},\mathbf{r}') \\ & + \left(\frac{\nabla\nabla_z}{k_m^2} + \mathbf{zz}\right) g_m^{TM,R}(\mathbf{r},\mathbf{r}') \\ & + \left(\frac{\nabla\nabla_s}{k_m^2} - \frac{\nabla_s\nabla_s}{k_s^2}\right) g_{mh}^{TM,R}(\mathbf{r},\mathbf{r}') \\ & + \left(\bar{\mathbf{I}}_s + \frac{\nabla_s\nabla_s}{k_s^2}\right) g_m^{TE,R}(\mathbf{r},\mathbf{r}'),\end{aligned}$$

where $\bar{\mathbf{G}}^{RWG}$ represents the interaction between points on RWG basis functions.

If the source and field points are in different layers, the dyadic Green's function assumes a different form

$$\bar{\mathbf{G}}^{RWG}(\mathbf{r},\mathbf{r}') = \frac{1}{k_m^2}\left(\nabla\nabla_z + k_n^2\mathbf{zz}\right) g_n^{TM}(\mathbf{r},\mathbf{r}') - \frac{1}{k_m^2}\left(\frac{k_n^2}{k_m^2}\nabla_s\nabla_s - \nabla\nabla_s\right) g_{nh}^{TM}(\mathbf{r},\mathbf{r}') + \left(\bar{\mathbf{I}}_s + \frac{\nabla_s\nabla_s}{k_s^2}\right) g_n^{TE}(\mathbf{r},\mathbf{r}'),$$

where the above equation is equivalent to the previous one when the layer indices m and n are the same.

Using the divergence-free property of the loop basis, the dyadic Green's function can be reduced when either basis or testing function is a loop basis. The above equations become

$$\bar{\mathbf{G}}^{L}(\mathbf{r},\mathbf{r}') = \mathbf{zz} g_m^{TM}(\mathbf{r},\mathbf{r}') + \bar{\mathbf{I}}_s g_m^{TE}(\mathbf{r},\mathbf{r}')$$

and

$$\bar{\mathbf{G}}^{L}(\mathbf{r},\mathbf{r}') = \mathbf{zz}\frac{k_n^2}{k_m^2} g_n^{TM}(\mathbf{r},\mathbf{r}') + \bar{\mathbf{I}}_s g_n^{TE}(\mathbf{r},\mathbf{r}'),$$

respectively. Since the dyadic Green's function can be reduced for a loop basis, it takes less time to compute the impedance matrix elements associated with loop bases.

III. Fast Loop-Tree Extraction in Low-Frequency Electromagnetics

Traditional loop-tree extraction algorithms generate loop and tree basis functions separately. Since trees can be generated easily by graph traversing algorithms, we exploit the information embedded in the tree to generate loops, i.e. closing the acyclic paths by chords. Since the procedure is totally independent of the geometry of the structure, it is also called a topological loop-tree extraction.

However, the fundamental loops are quite long and their total length far exceeds that of the minimal loop basis. We use the fact that local loops are located in between comb-like branches of breadth-first-search trees and further reduced the fundamental loops by shortcuts [3]. By applying the algorithm, loops on a donut-shaped ground plane (Fig. 1) can be extracted in linear time as the electric size of the plane increases (Fig. 2).

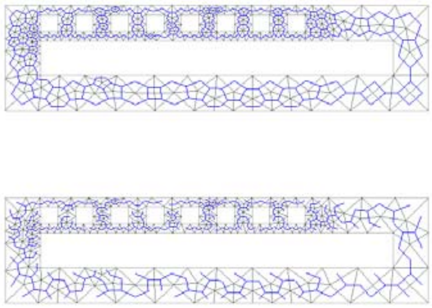

Fig. 1. The surface mesh of a donut structure with many holes and the corresponding graph (top) and the spanning tree (bottom) [3].

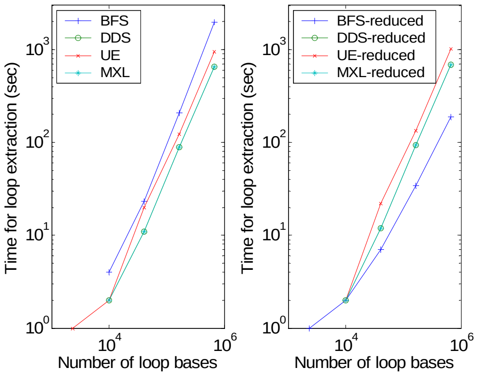

Fig. 2. The CPU time for extracting loop bases from BFS, DDS, UE, and MXL trees with (right) and without (left) loop reduction [3].

We further develop an efficient loop reduction algorithm is to reduce global loops [4], so the overall loop sizes is close to minimal. Comparing with the greedy method [5], our algorithm is more efficient for extracting loops on structures with large surfaces and a few interconnects. Hence, it is especially advantageous for the analysis of interconnects in between large reference planes.

IV. Broadband Equivalent Circuit Generation for Large-Scale Interconnect Analysis

For the broadband equivalent circuit generation, we find that the vector fitting method (VFM) [6] is superior to the complex frequency hopping (CFH) method [7]. The main reason is that VFM can predict poles outside of the range of sampling frequencies, where CFH can not. More detailed comparison of the two methods can be found in Wang's thesis [8], where broadband macromodels (i.e. equivalent circuits) are generated for simple antenna systems. For dipole antennas with clear resonant/anti-resonant peaks, there must be one pole associated with each peak. Only VFM can extract the correct poles associated with the resonant/anti-resonant peaks.

We further modify VFM for macromodel generation of a 32-port PCI Express bus on a PCB. With proprietary technologies, the number of circuit elements generation by our in-house code is 32% less than the traditional VFM (291,230 vs. 427,584). The reduction in circuit simulation time is even more obvious (1,890 vs. 10,593 sec). As the number of ports increases, our algorithm exploits the distinctive characteristic of individual transfer function. Therefore, the number of poles for the state-space realization is significantly reduced. A statistic model has also been developed for predicting the percentage reduction of circuit elements prior to equivalent model generation. Detailed results will be shown in [9].

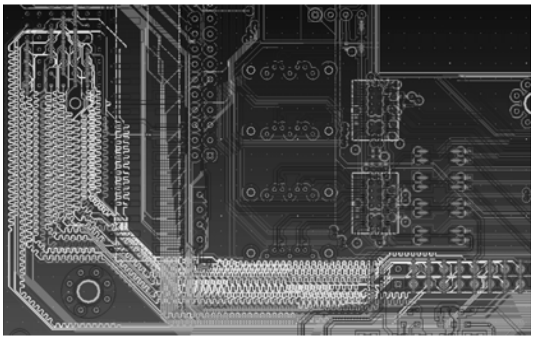

Fig. 3. Schematic capture of the PCI Express bus on a PCB.

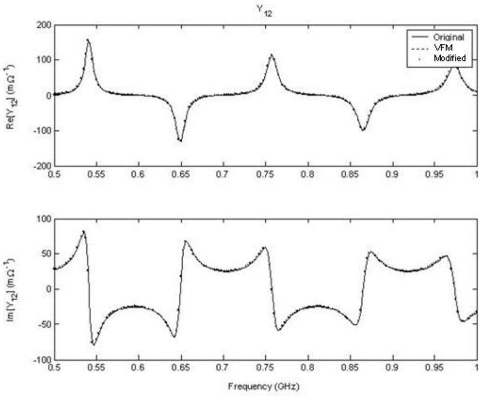

Fig. 4. Frequency responses of the original full-wave simulation, fittings by VFM and our modified algorithm.

V. Conclusions

We have developed three key technologies for interconnect analysis at low frequencies. Using the topologically based algorithm for loop-tree extraction, there is no need to discern the types of basis functions. The loop reduction process guarantees the independence of loops. Therefore, there is no need to perform independence check repetitively as in the greedy method. Besides, the decomposition of multilayered Green's function at low frequencies enables us to see divergence-free (loop) and non-divergence-free (tree) current components even before the surface current is discretized. It also make the computation of MoM impedance matix efficient and stable. In addition, our algorithm for macromodel generation significantly saves circuit simulation time because it can represent a single frequency response with less number of circuit components, as compared with the original VFM.

VI. Self-Evaluation

Under the sponsorship from NSC, we have developed two programs: one for fast loop-tree extraction and another for broadband equivalent circuit generation. Results related to the project have been presented at the 2006 IEEE AP-S Symposium [3] and have received widespread interests from the audience. More results are in preparation for submission to the Journal of Experimental Algorithms [4] and the IEEE Transactions on Circuits and Systems [9].

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附件一

可供推廣之研發成果資料表

□ 可申請專利　■ 可技術移轉　　日期：95 年 10 月 20 日

國科會補助計畫	計畫名稱：利用基於積分方程式之快速電磁解答器實現晶片導線之頻域及時域分析 計畫主持人：趙學永 計畫編號：NSC 94－2213－E－009－068－ 學門領域：電信
技術/創作名稱	低頻電磁中圈與樹基底函數之快速萃取演算法
發明人/創作人	趙學永
技術說明	中文：電場積分方程式在低頻運作下並不穩定，要藉由圈與樹基底函數分解才能有效模擬靜電及靜磁效應。利用圖學及拓樸理論可在近線性的複雜度之下找出樹與圈函數並加以簡化。 英文：EFIEs are unstable at low frequencies. However, one can model the separation of electrostatics and magnetostatics by tree and loop basis functions. Using graph and topology theories, tree and loop functions can be extracted and reduced in almost linear time for complex structures.
可利用之產業及可開發之產品	國防工業、電腦輔助軟體設計、半導體及電子業。 電磁及高頻電子相關電腦輔助設計軟體。
技術特點	易於加於現有基於電場積分方程式的電磁模擬程式中。
推廣及運用的價值	計畫中發展的數值技術可節省電磁及高頻電子模擬軟體開發及測試時間。

※　1. 每項研發成果請填寫一式二份，一份隨成果報告送繳本會，一份送 貴單位研發成果推廣單位（如技術移轉中心）。

※　2. 本項研發成果若尚未申請專利，請勿揭露可申請專利之主要內容。

※　3. 本表若不敷使用，請自行影印使用。