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矽奈米線之製備與相關元件之研製與分析

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奈米線之製備與相關元件之研製與分析

"Preparation and Device Fabrication of Si Nanowires"

計畫編號：NSC 94-2215-E-009-073

執行期間：94 年 8 月 1 日 至 95 年 7 月 31 日

主持人：林鴻志 交通大學電子工程系副教授

一、摘要

中文摘要

本專題計畫提出一種成本不高、製程步驟簡易的新穎矽奈米線之製備方式，目的為改善一般由 top-down 製造矽奈米線的主要缺點：製程設備昂貴或流程複雜。此方法主要是在矽晶圓上沉積薄絕緣層，利用 I-line stepper 微影和化學濕蝕刻方式將此絕緣層微縮至奈米級大小。以此微影蝕刻後之絕緣層當作硬遮蔽層(hard mask)，再乾蝕刻矽基板，便可使形成奈米線結構。此製備方式除了製程簡單和低成本之優點外，其所形成之奈米線的直徑、長度和晶格座向更可精確地控制。此外，經由穿透式顯微鏡(TEM)之分析，可證實所製備出來之矽奈米線擁有良好之結晶特性。因此，相信本製造方法可提供再現性高和可靠度佳之矽奈米線，以應用至相關之元件產品。

英文摘要

In this project, a novel approach for preparation of silicon naonwires (SiNWs) via straightforward and economic process is proposed and demonstrated. This technique utilizes non-critical photolithography and etching steps to define the NWs with good control over the structural parameters such as the orientation, diameter and length. It is superior to conventional top-down manners in terms of lower cost and simplified process flow. In this process, I-line photolithography is used to define the original diameter of hard mask patterns to a sub-micrometer feature size. By using chemical wet etching, the size of hard mask is further shrunk to sub-100 nm. With this nano-scale hard mask, SiNWs can be acquired after an anisotropic dry etching of Si substrate, albeit no expensive lithography tool is involved in the process flow.

二、計畫的緣由與目的

矽奈米線結構近來已受到各個研究團隊的矚目。藉由其高表面積/體積比，奈米結構表面的狀況將會對奈米線內部的載子傳導有深切的影響。利用此性質，奈米線對於感測元件應用可提供相當高的偵測靈敏度[1]。一般製備奈米線的方式主要分為兩類，一是 bottom-up [2]，另一為 top-down [3]。在大部份 bottom-up 的方式中，以金屬催化成長來形成奈米線是最為常見的。此法可用來製備不同材料的奈米線，除了矽奈米線外，還有鍺(Ge)奈米線[4]、磷化銦(InP)奈米線[5]等。因此這個方式為各個相關研究機構主要的研究方法。但是金屬催化成長目前仍有一些問題存在，如奈米線的長度、直徑和晶格座向皆無法受到良好的控制，以及在晶圓上無法準確地定位，這意味其有著再現性不高的疑慮。同時，金屬奈米粒子的使用亦是一個潛在污染的議題。所以，這些問題的存在，將會限制一要求高性能表現之奈米線電子元件的製作。一般以 top-down 製作奈米線的方法，如使用 deep UV [6]和 e-beam [7]等曝光設備，或許可以解決這些課

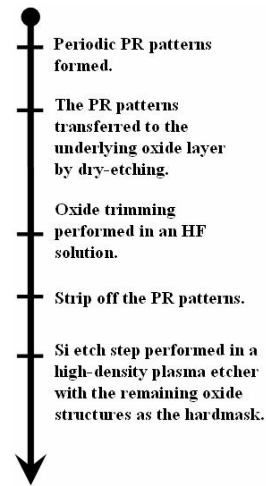
題。但是這些設備所費不貲，並且常需要 SOI (Silicon-on-Insulator)晶圓當作基板材料，故製作成本的付出相當昂貴。

鑑此，本研究計畫提出一新穎奈米線之製備方式，利用一般半導體製程設備和技術，以避免 bottom-up 法對於奈米線直徑、長度和晶格座向無法精準控制的問題，和有金屬污染或殘留缺陷的疑慮，以及傳統 top-down 法製造成本高等之缺點。此製備方法最大特點是：(1)可準確地控制奈米線直徑和長度，(2)易調變奈米線之摻雜型式，(3)無金屬污染，(4)矽晶圓可重複利用。目前以成本低和簡易步驟的製程技術，來實現可重複性高且可量產之奈米線，是各個相關研究單位爭相追求的，相信以此矽奈米線製備方式，可以達成高品質的矽奈米線以及量產化的目標，並可進一步將其應用至相關電子元件。

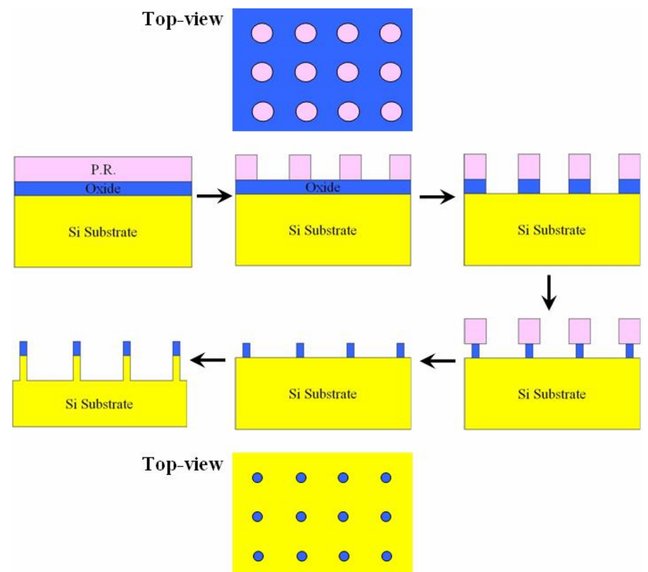
三、研究方法及成果

研究方法

製作矽奈米線之流程圖和示意圖如圖一和圖二所示。首先，將一矽基板表面形成氧化層，然後以 I-line stepper 定義出奈米線位置，並以乾蝕刻方式將無光阻覆蓋之氧化層去除。之後利用氫氟酸以濕蝕刻方式將氧化層微縮(oxide trimming)。氧化層圖形之直徑可藉由氫氟酸的濃度和蝕刻時間來控制。此步驟可將圖形微縮至奈米級尺寸，而不需昂貴曝光設備和複雜之技術。在氧化層微縮後，將其表面的光阻移除，然後以此氧化層當作硬遮蔽層(hard mask)，利用非等向性電漿乾蝕刻矽基板，此時便可得到矽奈米線結構。藉由仔細調控蝕刻條件和時間，我們便可精準地控制奈米結構之直徑和長度。



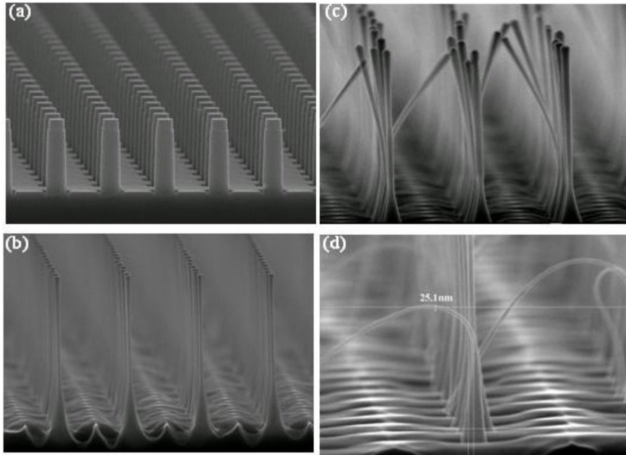
圖一、製作矽奈米線之流程圖。



圖二、矽奈米線製作之示意圖。

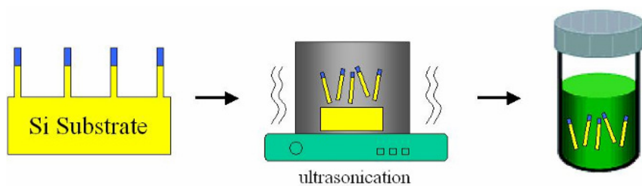
研究成果

圖二為不同直徑之矽奈米線 SEM 側視圖，其高度皆約為 2 μm。圖二(a)中的試片之氧化層未接受微縮處理，因此蝕刻後矽奈米線的直徑約為 1.3 μm。而圖二(b)~(d)則是氧化層受到不同時間之微縮處理，所以奈米線直徑可控制到 40 和 30 nm，甚至可達 30 nm 以下。此外，由這些 SEM 圖我們可觀查出當奈米線直徑約至 30 nm 以下，其結構便開始具有可彎曲性，所以當採收下來之奈米線，相信可應用至一些相關奈米線開關(nanowire switch)元件[8]。



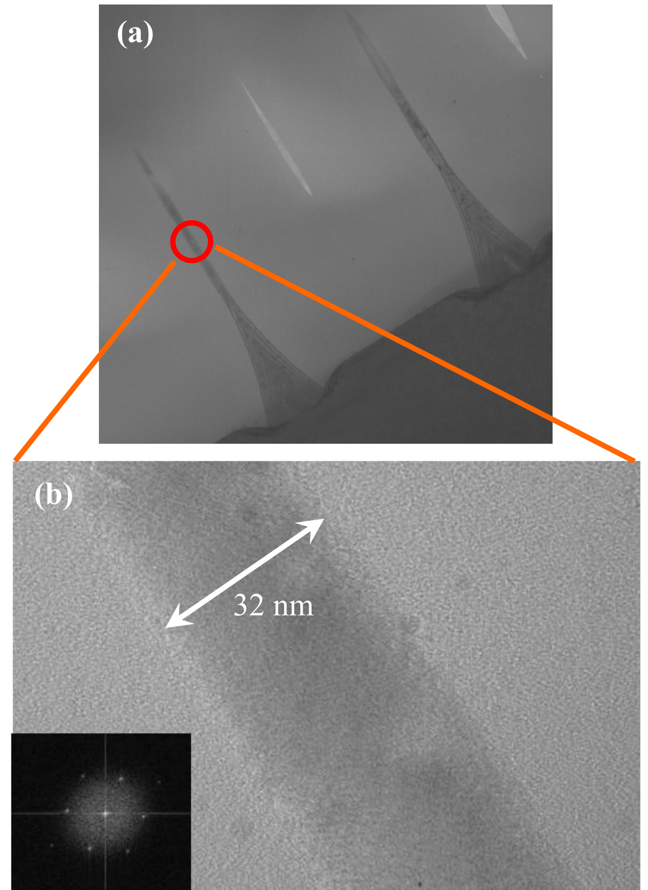
圖三、不同直徑之矽奈米線 SEM 影像 (a) 1.3 μm，(b) 40 nm，(C) 30 nm，(d) < 30 nm。

當奈米線蝕刻完成後，我們將含有矽奈米線之矽基板浸入乙醇中，利用超音波震盪使奈米線根部與矽基板分離(圖四)。之後將矽基板從溶液中移除，此時乙醇溶液中的矽奈米線可藉由一般排列對準方式[9-10]，放置到不同之基板上，使形成不同種類之電子元件，如矽奈米線場效電晶體[11]和矽奈米線感測器[12]。另外值得注意的是將奈米線移除後之矽基板，後續仍可用來進行另一批次的矽奈米線之製備，故可降低材料之消耗和成本。



圖四、利用超音波震盪將矽奈米線採收下來，並可保存於乙醇(ethanol)中。

圖五(b)為一矽奈米線之高解析度 TEM 及其繞射圖。由此結果我們可得知矽奈米線在經過蝕刻和採收後，並無受到很大之製程傷害，而仍保有良好之結晶特性。因此，本研究計畫所提出之奈米線製備方式相信可提供高品質的矽奈米線，進而能應用到相關元件之製作，以達高性能之表現。



圖五、(a) 矽奈米線之側視 TEM 圖，(b) 矽奈米線高解析 TEM 影像及繞射圖。

四、結論與討論

在此研究計畫中，我們已完成並證實一以簡易步驟和低成本之方式來製作矽奈米線。以此方式所製作出之奈米線具有單晶性質，以及其直徑、長度和晶格座向可良好地受到控制，同時具有再現性高之特性。利用此矽奈米線，可有效地應用到奈米線相關電子產品之製作，如場效電晶體和生物化學感測器，相信必能有高可靠度之表現。

此外，本計畫之研究成果已於 2006 年 9 月在日本橫濱舉行的國際固態元件與材料(Solid State Devices and Materials, SSDM)會議中發表[13]，如附件。

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附件

A Novel Method for the Preparation of Si Nanowires

Raymond Lin[1], Horng-Chih Lin[1, 2,] *, Jung-Yen Yang[1],
Shih-Wen Shen[1], and Chun-Jung Su[2]

[1]National Nano Device Laboratories
[2]Department of Electronics Engineering and Institute of Electronics Engineering, National Chiao Tung University
1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, ROC
*Phone: 886-3-571-2121 ext:54193, Fax: 886-3-572-4361, E-mail: hclin@faculty.nctu.edu.tw

1. Introduction

Si nanowire (SiNW) structures have recently attracted a lot of attentions. By taking advantage of the high surface-to-volume ratio inherent in the structure, NWs can provide high surface sensitivity for sensing device applications [1], [2]. The preparation methods of NWs could be categorized into two types, namely, top-down and bottom-up [3]. Among a number of bottom-up approaches, catalytic growth is probably the most popular. This method is suitable for preparing various kinds of NW materials and can even be applied for forming NW heterostructures [4]. It is thus very flexible and suitable for the feasibility study in laboratories. However, there also exist some issues, such as the difficulty in controlling the NW dimensions including length and diameter, as well as the NW orientation [5]. Moreover, the use of metal nano particles as the catalyst represents a potential contamination issue. These issues may hinder practical applications. Besides, the manufacturing of NW devices may suffer from the uncontrollability of structural parameters such as NW's length and diameter. Thus the precise positioning of the NWs represents another major obstacle for reliable device fabrication. These issues probably could be overcome by using the top-down approaches that usually rely on advanced lithography tools, like the DUV steppers and e-beam lithography technique [6], to form the NW structures. Nevertheless, the process cost could be high owing to the use of costly lithography tools.

In this work we proposed and demonstrated a simple and promising approach that could effectively address the above issues. This approach belongs to the top-down category albeit no costly lithography step is involved.

2. Preparation and Characterization of SiNWs

Detailed process sequence is illustrated in Fig. 1. Firstly, the starting Si wafers were oxidized, then a g-line stepper was used to form periodic PR patterns on the surface. The PR patterns were transferred to the underlying oxide layer by a plasma etch step. Oxide trimming was subsequently performed in an HF solution to further shrink the dimension of the oxide structure. This step allows us to scale the patterns into nano-scale dimension without resorting to expensive equipments. With careful tuning of the etching conditions, the precise control over the structural dimensions is feasible. After the oxide trimming, the PR patterns were stripped off, followed by a Si etch step performed in a high-density plasma etcher with the remaining oxide structures as the hardmask.

Figure 2 shows several Si pillar structures having a height of around 2 μm. Figure 2(a) shows a sample that did not receive the oxide trimming treatment and the diameter is 1.3 μm. Figure 2(b)~(d) are the formed NW structures with diameter of 40, 30, and <30 nm, respectively. Note that the structure becomes very flexible when scaled below 30 nm.

Using the above samples, we've also developed a method to prepare a solution that contains Si NWs, as shown in Fig. 3. Wafers were then immersed in the solution and treated with megasonic oscillation to break the NWs from their root. Afterwards, wafers were removed and the solution was harvested. The solution could then be used as a source for forming aligned Si NWs on many kinds of substrates for electronic applications [7], [8].

Figure 4 shows the TEM image and the corresponding diffraction pattern of a SiNW structure. It is seen that good crystallinity could be retained.

3. Conclusion

In conclusion, we have proposed and demonstrated a very simple and low-cost method to fabricate silicon nano wires without resorting to expensive tools or complex processes. Besides, the processed wafers could be recycled and reused after suitable treatment. In contrast to the conventional approach using metal catalytic growth, the new method is essentially metal free and provides good control over the NW length, diameter, and orientation.

Acknowledgments

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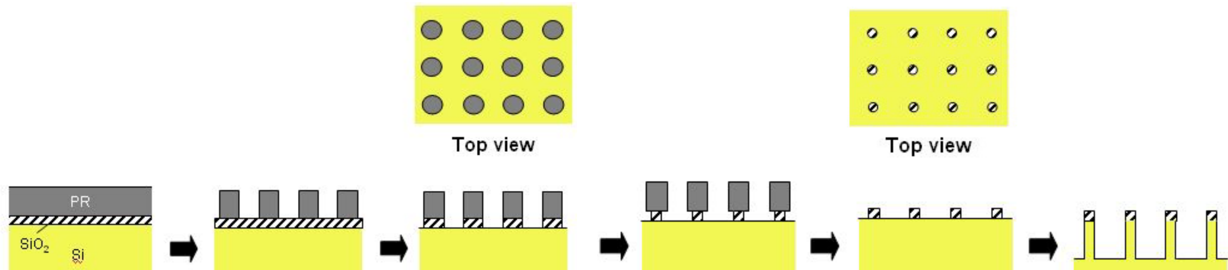

Fig.1 Process flow for the preparation of SiNWs.

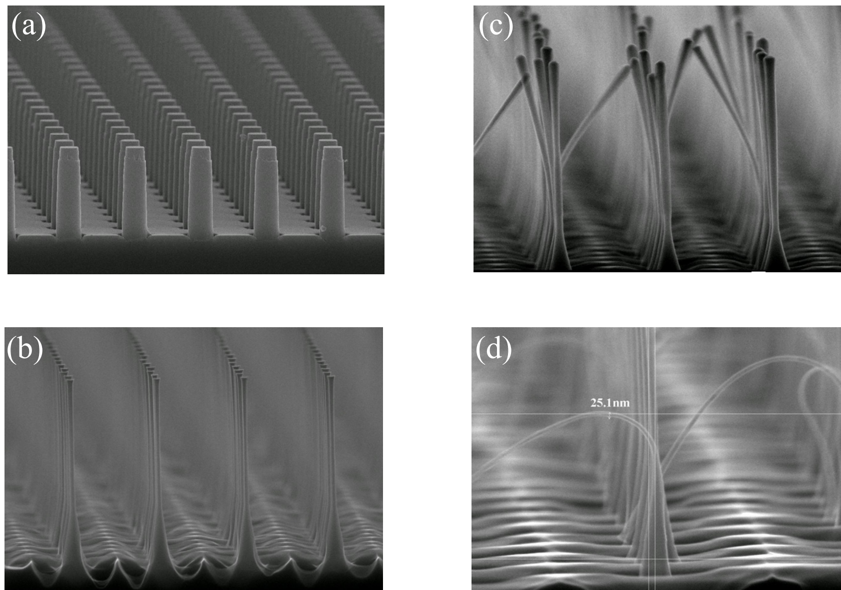

Fig.2 SEM pictures of the patterned Si pillar structures with diameter (a) 1.3 µm, (b) 40 nm, (c) 30 nm, and (d) <30 nm.

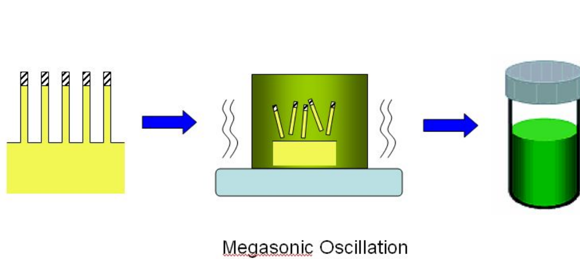

Fig.3 Preparation of NW solution.

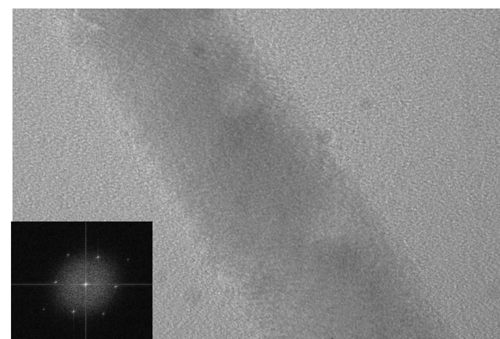

Fig.4 TEM image of the SiNW.