Characterization of Enhanced Stress Memorization Technique on nMOSFETs by Multiple Strain-Gate Engineering

Tsung-Yi Lu, Tien-Shun Chang, Shih-An Huang, and Tien-Sheng Chao

***Abstract*—To extend a carrier mobility improvement by strain engineering in high-density and small-gate-space complementary metal–oxide–semiconductor (CMOS) circuits, we have proposed a new stress memorization technique (SMT) that uses a strain proximity free technique (SPFT) to demonstrate the mobility improvement through multiple strain-gate engineering. The electron mobility of n-channel metal–oxide–semiconductor (MOS) field-effect transistors with the SPFT exhibits a 14% increase over counterpart techniques. Compared with the conventional SMT, the SPFT avoids the limitation of the stressor volume for the performance improvement in high-density CMOS circuits. We also found that the preamorphous layer (PAL) gate structure in combination with the SPFT can improve the mobility further to 31% greater than standard devices. Moreover, an additional 30% mobility enhancement can be achieved by using a dynamic threshold-voltage MOS and combining the PAL gate structure with the SPFT, respectively. The gate-oxide reliability and the channel-hot-carrier reliability are also analyzed. Our results show a mobility improvement by the SPFT, a slightly increased gate leakage current, and degraded channel-hot-carrier reliability.**

***Index Terms*—Mobility, n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs), strain.**

I. Introduction

IN PURSUE of high-speed circuit applications, mobility enhancement by local stressor engineering in high-performance complementary metal–oxide–semiconductor (CMOS) transistors has been intensively studied using techniques such as contact etch-stop layer (CESL) and embedded SiGe in the source/drain (S/D) area [1]–[4]. Recently, a stress memorization technique (SMT) has been reported to enhance the electron mobility on n-channel MOS field-effect transistors (nMOSFETs) and has been widely studied using a variety of approaches [5]–[7]. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate density. As the scaling of design rules such as poly pitch shrinks in high-density static-random-access-memory circuits (as shown at the top of Fig. 1), the mobility enhancement will be limited by the stressor volume and process integration issues. The introductions of the longitudinal tensile stress and the vertical compressive stress into the channel region are well-known principles of mobility enhancement in nMOSFETs [8]. However, the longitudinal tensile stress will be limited as the stressor volume reaches its saturation point, causing performance degradation [9]. Moreover, poor Ni-silicide formation and contact process integration issues will be induced by the stressor residue in high-density CMOS circuits.

In this paper, we propose a strain proximity free technique (SPFT) to circumvent the limitation of the stressor volume for the performance improvement in high-density circuits. A stacked a-Si/poly-Si gate structure has been reported to enhance the channel stress and the electron mobility [10]. We have proposed a preamorphous layer (PAL) gate structure using the implantation process to further improve the performance on nMOSFETs.

The dynamic threshold-voltage MOS (DTMOS), which lowers the threshold voltage of MOSFETs only in an active operation, is proposed for high-speed and low-power applications [11], [12]. The DTMOS realizes a higher saturation current in the active mode and a lower leakage current in the standby mode. We have applied the DTMOS and combined it with the SPFT to demonstrate a further performance improvement without increasing the standby power consumption. The gate-oxide reliability and the channel-hot-carrier reliability are also discussed for characterizing the performance improvement and the device reliability on the strain engineering.

II. Experiment and Characterization

The nMOSFETs were fabricated on 6-in wafers using a conventional MOSFET process flow, including local oxidation of device isolation, gate oxide, S/D extension (SDE) implantation, sidewall spacer formation, deep S/D implantation, contact patterning, and metallization processing, as listed in Fig. 1. All the nMOSFETs characterized in this paper had a 2.5-nm-thick gate oxide and a 150-nm-thick poly-Si layer as the gate electrode, grown in a vertical furnace. The PAL gate structure was proposed by arsenic atom implantation. Two arsenic dosages were split in this paper for achieving different thicknesses of the

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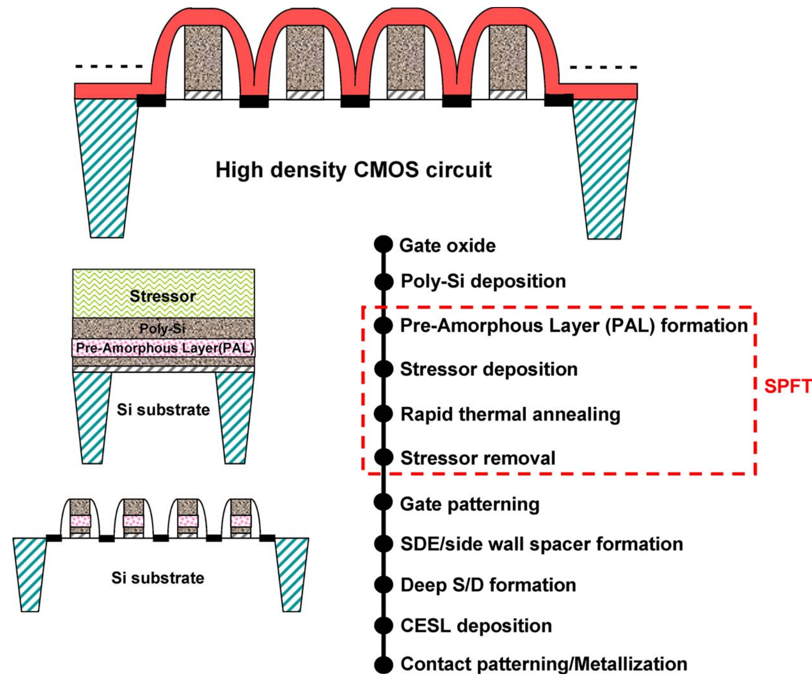


Fig. 1. High-density CMOS circuit-structure process flow for the SPFT.

amorphous layer in the gate electrode. The arsenic energy and dosage split in the experiment were 50 KeV and 1×10^{15} cm^{-2}, and 50 KeV and 5×10^{15} cm^{-2}, respectively. The PAL is located between the gate oxide and the poly-Si layer. The SPFT process flow is inserted between the poly-Si layer deposition and the gate patterning. Before the patterning on the poly-Si gate, the SPFT is introduced by high tensile-stressor deposition, rapid thermal annealing (RTA), and stressor removal processes. The stressor of the SPFT in this experiment is a high tensile Si_3N_4 film with a 100-nm thickness by low-pressure chemical vapor deposition (LPCVD). The stress level of this film is nearly 1.3 GPa. The RTA was processed by spike annealing in a 1050 °C ambient. Two-step dry-and-wet etching was used in the stressor removal process. To protect the poly-Si from plasma damage under the dry etch, 90% of the stressor thickness was removed by plasma etching, and the remainder was stripped by a thermal H_3PO_4 acid. Photo patterning and plasma etching to define the gate electrode were then carried out. After the gate patterning, SDE formation by arsenic implantation, sidewall spacer formation, and deep S/D implantation were processed. After the S/D dopant activation by spike RTA, a 100-nm LPCVD tensile Si_3N_4 CESL was deposited on all transistors. After the interlayer dielectric film deposition and contact patterning, a four-level metallization (Ti–TiN–Al–TiN) was carried out in the physical vapor deposition system.

The device characteristics were measured by a Keithly-4200 semiconductor parameter analyzer. The electron mobility is determined by the field effective mobility extraction as $\mu_{\rm EF} = (G_m \times L)/(W \times C_{\rm ox} \times V_d)$, where G_m is the transconductance, $C_{\rm ox}$ is the gate-oxide capacitance, V_d is the drain voltage, and W and L are the channel width and length, respectively. The threshold voltage was determined by the constant drain-current method when the drain current was set to 40 nA/μm. The linear- and saturation-mode threshold voltages, i.e., Vt_lin and Vt_sat, were extracted at drain voltages of 0.1 and 1.5 V, respectively.

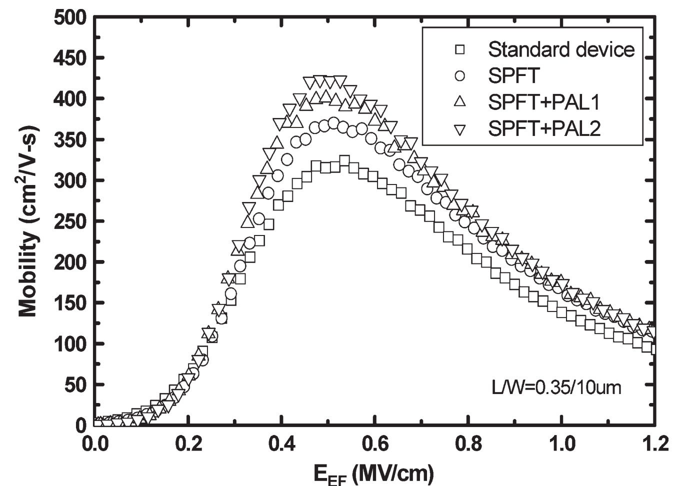


Fig. 2. Electron mobility of the nMOSFET for the SPFT and combining the SPFT with the PAL gate structure with channel width/length = 10/0.35 μm.

III. Results and Discussion

The gate-oxide reliability is confirmed by testing the breakdown voltage $V_{\rm BD}$. The SPFT shows a $V_{\rm BD}$ $(= 5\ {\rm V})$ performance comparable with standard devices. The performance improvement for the nMOSFET is illustrated in Fig. 2. The standard device here is an unstrained device without the SPFT and the PAL gate structure. The SPFT without the PAL gate structure shows a 14% mobility improvement on the device channel width/length = 10/0.35 μm. The corresponding I_d–V_d characteristic of the SPFT is also shown in Fig. 3. The SPFT shows an 8% I_d improvement, as compared with that of the standard device.

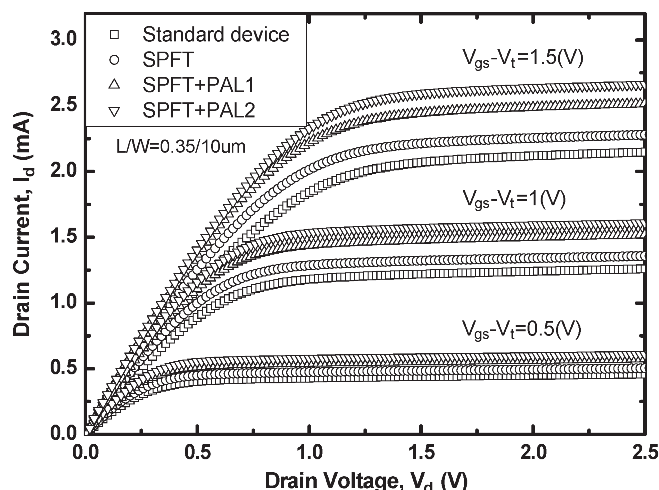


Fig. 3. Corresponding I_d–V_d characteristic of the nMOSFET for the SPFT and combining the SPFT with the PAL gate structure with channel width/length $= 10/0.35\ \mu$m.

Since the SPFT is applied to introduce the stress into the channel region before the gate patterning, it can prevent the problems of stressor volume and small gate pitch in high-density circuits. A simple model is proposed to explain the mechanism of the SPFT. In [13] and [14], it was reported that the vertical compressive stress is the major component of the stress in SMT processes. In the SPFT approach, the RTA has transferred the high tensile stress from the disposable stressor to the gate poly-Si, resulting in the induction of a plastic strain in the poly-Si. To compensate for this external stress from the disposable stressor, a very high vertical compressive strain is induced in the poly-Si. The deformation of the poly-Si is expanded in the longitudinal direction and compressed in the vertical direction. This further creates the longitudinal tensile stress and the vertical compressive stress in the Si channel. After the stressor removal, the high longitudinal tensile stress and vertical compressive stress will be memorized in the channel region. This mechanism appears to explain the increased stress resulting from the use of the SPFT to enhance the electron mobility. Moreover, previous studies have shown that the poly-Si got a smaller grain size after processing with the SMT [7]. Our scanning electron microscope (SEM) pictures show that the mean grain size of the typical poly-Si is 77–106 nm, whereas the mean grain size for the SPFT poly-Si is 64–86 nm, as shown in Fig. 4. The grain-size change during the SPFT may affect the interface between the poly-Si and the gate oxide, which modulates the energy barrier height in the poly-Si.

A significant improvement of the mobility on the SPFT with a PAL gate structure is found, as shown in Fig. 2. It appears that the SPFT with the PAL gate structure can further increase the mobility to 24% for PAL 1 and 31% for PAL 2, dosing with 50 KeV and 1×10^{15} and 5×10^{15} cm^{-2} of arsenic implantation, respectively. Moreover, the I_d increase of 21% and 28% (as shown in Fig. 3) may be achieved when using both the SPFT and the PAL gate structure. The mechanism of the stress enhancement in the PAL gate structure may be as follows: The recrystallization of the amorphous region during the SPFT process leads to the shrinkage of the total thickness of the gate and results in a residual compressive strain. The PAL gate structure with the optimization of the arsenic implantation of the PAL provides more vertical compressive stress and longitudinal tensile stress to the channel region. For a recent high-k/metal gate structure, a thin metal layer below the poly-Si plays a role in the work function adjustment. Since the metal layer that we usually use is thinner than 10 nm, we believe that the SPFT combined with the PAL gate structure can be efficient for improving the electron mobility in the advanced technology [15]–[17]. The gate leakage current under the SPFT combined with the PAL gate structure is slightly higher than that in a conventional gate structure device, which is nearly 30 pA$/\mu$m, as shown in Fig. 5. The higher gate leakage current in the PAL 2 gate structure may come from the thicker PAL, which is inducing the interface roughness between the gate oxide and the Si substrate during the SPFT.

The DTMOS is applied for a further performance boost to the SPFT. This was proposed by connecting the poly-Si gate to the Si body (well region). We present the gate-length dependence of the threshold voltage for a standard device and the DTMOS device in Fig. 6. The saturation threshold voltage Vt_sat for the DTMOS SPFT was nearly 100-mV Vt_sat lower than the standard SPFT device. A better explanation for the reduction of the threshold voltage is a forward Si body to the source junction bias. Furthermore, an insignificant Vt_sat difference is found when using the SPFT to improve the electron mobility. As shown in Fig. 7, the electron mobility is improved by 32% and 46% using the DTMOS standard device and the DTMOS SPFT, as compared with the simple standard device. Moreover, a nearly 60% mobility enhancement can be achieved by combining a PAL 2 gate structure with the DTMOS SPFT. The corresponding I_d–V_g characteristic of the DTMOS SPFT is illustrated in Fig. 8. The drain current at the $I_{\mathrm{on},(V_g=0.7\ \mathrm{V},V_d=0.1\ \mathrm{V})}/I_{\mathrm{off},(V_g=0\ \mathrm{V},V_d=0.1\ \mathrm{V})}$ state and the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio are also illustrated in the inset of this figure. It is shown that the I_{off} current of the DTMOS SPFT and the PAL gate structure combined with the DTMOS SPFT is comparable with the simple standard device. A higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio can be achieved by combining the PAL gate structure with the DTMOS SPFT. It enables the realization of the lower threshold-voltage operation and the higher electron mobility for high-speed circuit applications.

The dependence of the channel-hot-carrier reliability is shown in Fig. 9. We found that the shift in the threshold voltage $\triangle V_{\mathrm{th}}$ and the electron mobility degradation are slightly higher in the SPFT as a function of the stress time. This result is attributed to the improved drain current under the same bias conditions and the induced higher substrate current. Since the mobility enhancement is related to the stress-induced energy band-gap narrowing, it will accompany the modification of the impact ionization rate and the channel hot carriers in the Si substrate. The SPFT with the PAL gate structure introduces more stress into the channel region. As shown in Fig. 10, $\triangle V_{\mathrm{th}}$ and the mobility degradation are slightly higher than that for the single SPFT device. This paper explored both the performance improvement and the device reliability on the SPFT device, finding that the higher strain provided higher electron mobility but degraded the device reliability.

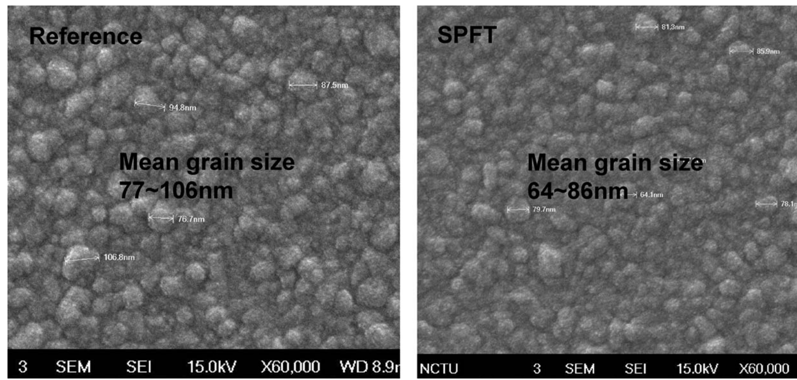


Fig. 4. SEM pictures with the mean grain size of the poly-Si for the SPFT.

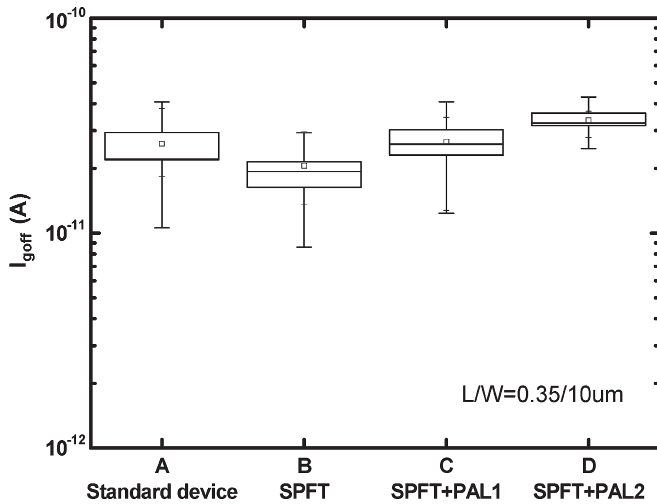


Fig. 5. Gate leakage current of the nMOSFET for the SPFT and combining the SPFT with the PAL gate structure with channel width/length $= 10/0.35$ μm.

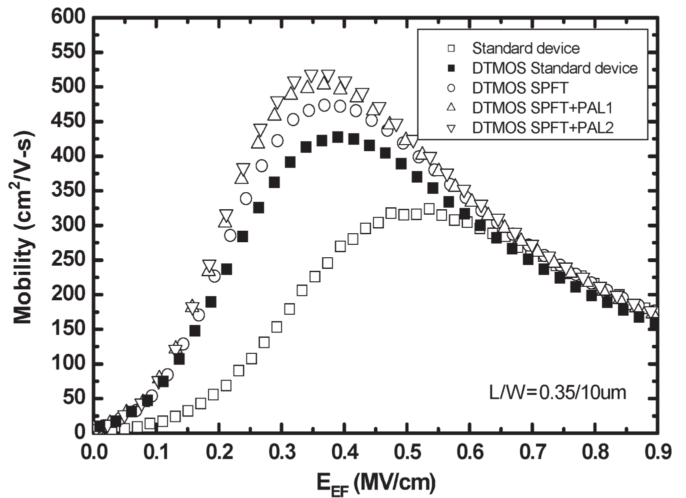


Fig. 7. Electron mobility of the nMOSFET for the DTMOS SPFT and combining the SPFT with the PAL gate structure with channel width/length $=$ $10/0.35$ μm.

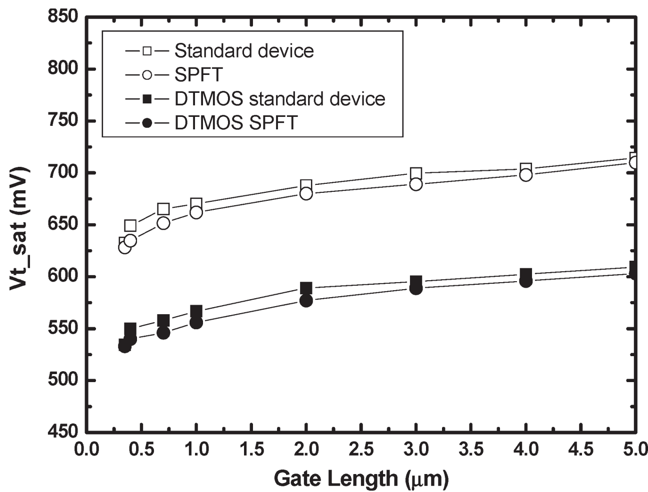
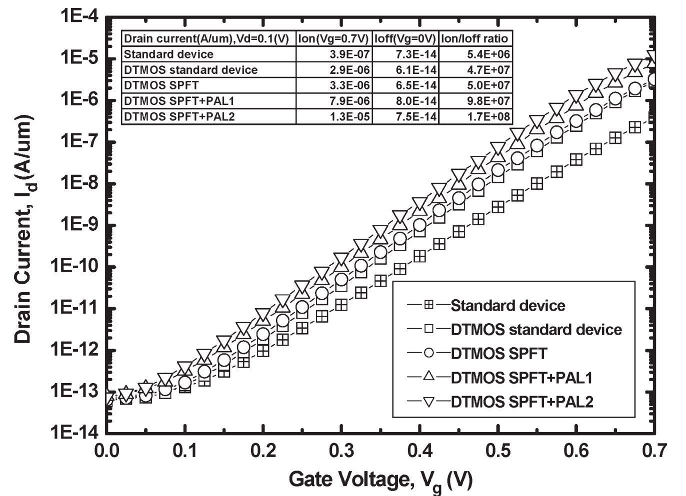


Fig. 6. Saturation threshold voltage Vt_sat of the nMOSFET for the SPFT and the DTMOS SPFT.



Drain current(A/um),Vd=0.1(V)	Ion(Vg=0.7V)	Ioff(Vg=0V)	Ion/Ioff ratio
Standard device	3.9E-07	7.3E-14	5.4E+06
DTMOS standard device	2.9E-06	6.1E-14	4.7E+07
DTMOS SPFT	3.3E-06	6.5E-14	5.0E+07
DTMOS SPFT+PAL1	7.9E-06	8.0E-14	9.8E+07
DTMOS SPFT+PAL2	1.3E-05	7.5E-14	1.7E+08

Fig. 8. Corresponding I_d–V_g characteristic of the DTMOS SPFT and combining the PAL gate structure with the DTMOS SPFT with channel width/length $= 10/0.35$ μm. (Inset) The drain current at the $I_{\mathrm{on},(V_g=0.7\ \mathrm{V},V_d=0.1\ \mathrm{V})}/I_{\mathrm{off},(V_g=0\ \mathrm{V},V_d=0.1\ \mathrm{V})}$ state and the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio.

IV. Conclusion

We have proposed a multiple strain-gate engineering that uses the SPFT and the PAL gate structure. The electron mobility and the current drivability may be improved by controlling the SPFT process and the thickness of the PAL gate structure. Moreover, the SPFT in combination with the DTMOS can achieve a lower threshold-voltage operation and a higher performance boost. The channel-hot-carrier reliability is slightly

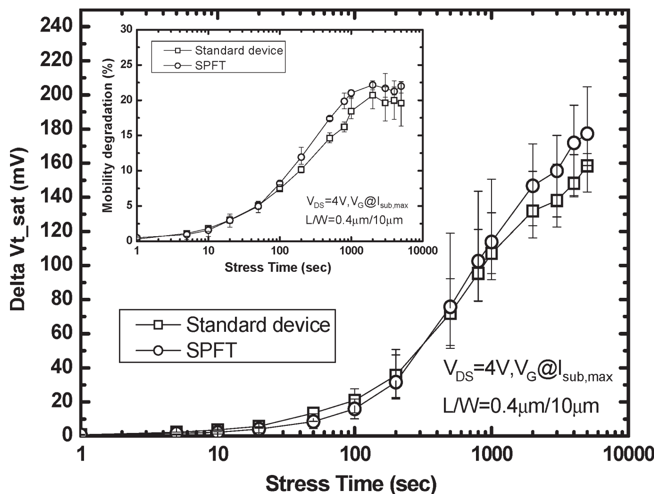


Fig. 9. Threshold-voltage shift $\triangle V_{\mathrm{th}}$ for the SPFT under the hot-carrier stressing at $V_{\mathrm{DS}} = 3.5$ V and $V_g = V_{g,(\text{maximum substrate current})}$. Channel width/length $= 10/0.4$ μm. (Inset) Mobility degradation under identical stress conditions.

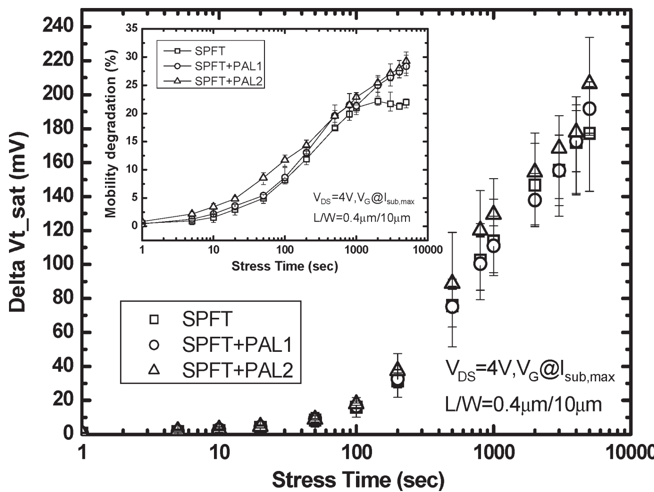


Fig. 10. Threshold-voltage shift $\triangle V_{\mathrm{th}}$ for the SPFT combined with the PAL gate structure under the hot-carrier stressing at $V_{\mathrm{DS}} = 3.5$ V and $V_g = V_{g,(\text{maximum substrate current})}$. Channel width/length $= 10/0.4$ μm. (Inset) Mobility degradation under identical stress conditions.

degraded as the channel stress is increased. Without the limitation of the stressor volume in high-density CMOS circuits, we believe that this scheme that combines the SPFT with the PAL gate structure and the DTMOS will serve as an important guide for the continued improvement in the future CMOS technology.

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