

Temperature-Dependent Remote-Coulomb-Limited Electron Mobility in n^+ -Polysilicon Ultrathin Gate Oxide nMOSFETs

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Abstract—Additional electron mobility due to remote scatterers in n^+ -polysilicon 1.65-nm gate oxide (SiO_2) n-channel metal–oxide–semiconductor field-effect transistors is experimentally extracted at three different temperatures (i.e., 233, 263, and 298 K). The core of the extraction process consists of simulated temperature-dependent universal mobility curves and Matthiessen’s rule in a mobility universality region. Resulting additional mobility for the first time experimentally exhibits a negative temperature coefficient, confirming interface plasmons in a polysilicon depletion region to be dominant remote Coulomb scatterers. We also present corroborative evidence as quoted in the literature, including: 1) calculated temperature-dependent remote Coulomb mobility due to ionized impurity atoms in a polysilicon depletion region; 2) experimentally assessed additional mobility at room temperature; and 3) simulated remote Coulomb mobility due to interface plasmons in a polysilicon depletion region as well as its temperature coefficient. Validity of Matthiessen’s rule used in this paper is verified.

Index Terms—Gate oxide, high- k , interface plasmons, metal gate, mobility, metal–oxide–semiconductor field-effect transistors (MOSFETs), phonons, polysilicon, remote Coulomb, scattering, surface roughness.

I. INTRODUCTION

ON n^+ -polysilicon gate oxide n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs), Takagi *et al.* [1] have experimentally found that inversion layer electron mobility is a combination of three distinct scattering mechanisms: 1) Coulomb scattering due to ionized impurity atoms in a substrate; 2) acoustic–optical phonon scattering in an inversion layer; and 3) surface roughness scattering

near a SiO_2/Si interface. However, mobility degradation was frequently encountered in a scaling direction, which means that additional scattering mechanisms exist. On the one hand, electron plasmons in a source/drain highly doped region can be significant according to Fischetti and Laux [2], as demonstrated in recent experiments by Cros *et al.* [3] and Barral *et al.* [4], [5]. On the other hand, degraded mobility with decreasing gate oxide thickness has been observed, particularly in moderate and high vertical effective field regions [6]–[8]. Because a long-channel device was used in mobility measurement [6]–[8], hence, the effect of source/drain electron plasmons can be insignificant; scattering mechanisms responsible for observed mobility degradation should in principle stem from scatterers in a remote region situated away from that of Takagi *et al.* [1].

However, origins of remote scatterers remained controversial in the past decades [7], [9]–[12]. In the beginning, Krishnan *et al.* [9] ascribed remote scattering to ionized impurity atoms in a polysilicon depletion region. Following that, Yang *et al.* [7] applied a remote Coulomb mobility model due to Stern and Howard [13] and found that corresponding remote Coulomb scattering (RCS) is too weak to constitute measured mobility degradation. In contrast, Fischetti [10] favored electron counterparts in a polysilicon depletion region, which can act as plasmons at a poly/ SiO_2 interface. Excitation and absorption of interface plasmons will further affect underlying 2-D electrons via long-range Coulomb interactions, a well-known phenomenon also called the Coulomb drag effect [14]. Simulated remote Coulomb mobility in a coupled interface plasmons/inversion layer system [10], [15] appeared to elucidate observed mobility degradation in [7] and [8]. In addition, the remainder of remote scatterers such as remote surface roughness [16] received somewhat attention [11], [12]. Through Monte Carlo simulation, Gámiz and Roldan [11] argued that remote surface roughness scattering is insignificant in moderate and high vertical electric field regions.

Recently, there have been two specially designed experiments concerning validity of an interface plasmon or a drag hypothesis [17], [18]. Again, these two experiments led to controversial arguments. In the first experiment dedicated to drag measurement, Solomon and Yang [17] claimed that in a gate oxide thickness range of 1.9–2.5 nm, interface plasmons in a polysilicon region did not appear to explain oxide-scaling-induced mobility degradation. Oppositely, throughout a calibrated C – V splitting technique, the second experiment by Lime *et al.* [18] pointed out that mobility degradation is not due

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to increased surface roughness but due to interface plasmons, which is valid for gate oxide thicknesses down to 1.2 nm.

Thus, reexamination of remote scattering sources in polysilicon ultrathin gate oxide nMOSFETs is essential and crucial. Additionally, it is worth noticing that the aforementioned experiments [6]–[8], [17], [18] were all conducted at room temperature only. In other words, so far, temperature dependence of remote scattering mechanisms was not experimentally taken into account in the case of polysilicon ultrathin SiO₂ gate stacks. However, a temperature-dependent experiment was shown to be useful in an analysis of remote scatterers in high-*k* gate stacks [19]–[21].

In this paper, we elaborate on a temperature-oriented experimental method dedicated to polysilicon ultrathin gate oxide stacks. The core of the method comprises two main parts: simulated temperature-dependent universal mobility curves, without conventional thick gate oxide test vehicle fabrication [6]–[8], [17], [18], and Matthiessen's rule, particularly in a mobility universality region. Additional scattering of inversion layer electrons by remote scatterers in a polysilicon region can straightforwardly be assessed. For the first time, temperature dependence of additional mobility is experimentally obtained, making possible the clarification of remote scattering mechanisms. In addition, presented is corroborative evidence in terms of a remote Coulomb mobility model, as cited in [7]; simulated values of the additional mobility and its temperature coefficient, as drawn from [10]; and experimental mobility degradation data at room temperature as available elsewhere [6]–[8]. Validity of Matthiessen's rule used in this paper is addressed as well.

II. EXPERIMENT, VALIDATION, AND EXTRACTION

An n-channel device under test was fabricated in a conventional 90-nm process. In this process, a SiO₂ film was thermally grown, followed by NO annealing. A measured *C*–*V* characteristic is depicted in Fig. 1. A self-consistent Schrödinger and Poisson's equation solver, as constructed elsewhere [22], was employed to fit the *C*–*V* data, leading to the following process parameters of the device: the n⁺-polysilicon doping concentration $N_{\text{poly}} = 9 \times 10^{19} \text{ cm}^{-3}$, the gate oxide thickness $t_{\text{ox}} = 1.65 \text{ nm}$, and the p-type substrate doping concentration $N_{\text{sub}} = 8 \times 10^{17} \text{ cm}^{-3}$. The fitting quality, as demonstrated in Fig. 1, is good. In addition, shown in the figure for comparison is another fitting line by the available self-consistent Schrödinger and Poisson's equations solver Schred [23], with the same process parameters as inputs. The channel width and length of the device had the same value of 10 μm . Inversion layer mobility was measured using a conductance method [1] over two V_D points of 10 and 25 mV. Measured effective mobility is plotted in Fig. 2 versus the vertical effective electric field E_{eff} for three measurement temperatures of 233, 263, and 298 K. Here, the formula $E_{\text{eff}} = q(0.5N_{\text{inv}} + N_{\text{dep}})/\epsilon_s$ was used, in which ϵ_s is the silicon permittivity, and the inversion layer electron density N_{inv} and the depleted bulk density N_{dep} were both obtained through self-consistent Schrödinger and Poisson's equations solving [22].

To produce temperature-dependent universal mobility curves, we performed the self-consistent Schrödinger and Poisson's

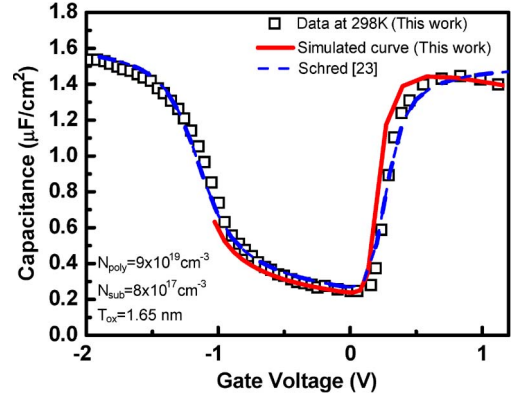


Fig. 1. Comparison of the measured (symbol) and simulated (lines) gate capacitance versus gate voltage. The lines came from the self-consistent Schrödinger and Poisson's equation solvers [22], [23].

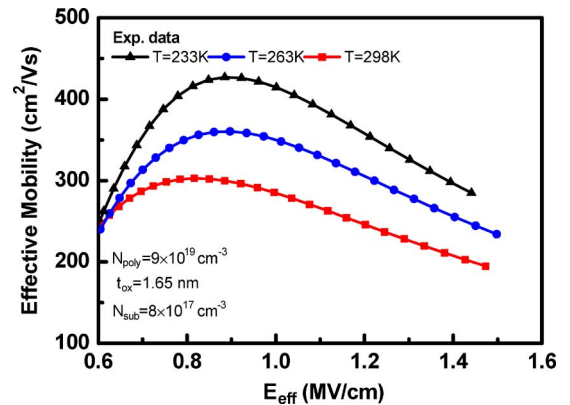


Fig. 2. Measured electron effective mobility (solid lines with symbols) versus vertical effective electric field for the three temperatures.

equations solving [22] to deliver subband levels and wave functions. Straightforwardly, universal mobility was calculated based on published formalisms of both phonon scattering and surface roughness scattering [24], [25]. Material parameters used were all the same as or close to those in [26]–[28], e.g., the acoustic deformation potential $D_{\text{ac}} = 12 \text{ eV}$, the deformation potential of the k th intervalley phonon $D_k = 8 \times 10^8 \text{ eV/cm}$, the energy of the k th intervalley f -type phonon $E_{k(f)} = 59 \text{ meV}$, and the energy of the k th intervalley g -type phonon $E_{k(g)} = 63 \text{ meV}$. In a universal mobility calculation, the following formula was used:

$$\frac{1}{\mu_{\text{univ}}^i} = \left\langle \frac{1}{\mu_{\text{ph}}^i(E)} + \frac{1}{\mu_{\text{sr}}^i(E)} \right\rangle \quad (1)$$

where μ_{univ}^i is the universal mobility of the subband i due to phonon and surface roughness scattering mechanisms, and brackets $\langle \rangle$ represent averaging over energy for the microscopic phonon mobility μ_{ph}^i and the surface roughness mobility μ_{sr}^i . Detailed simulation work can be found elsewhere [22]. The resulting universal mobility for a correlation length of the surface roughness λ of 14.9 \AA and a root mean square height of the surface roughness amplitude Δ of 2.4 \AA was found to fit the experimental data well for two different temperatures [1], as depicted in Fig. 3. This confirms the validity of the temperature-dependent universal mobility simulation work. Since different manufacturing processes may lead to different mobility

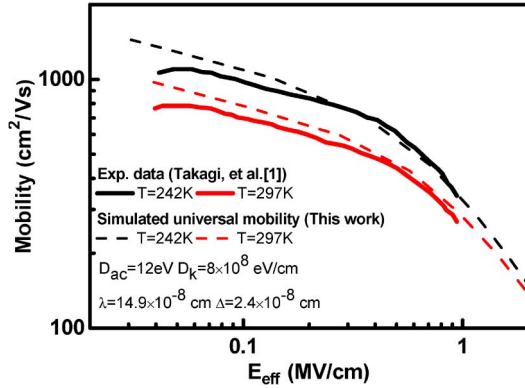


Fig. 3. Comparison of the experimental (solid lines) electron universal mobility curves for two temperatures of 242 and 297 K [1] with the simulated ones in this paper (dotted lines).

universality [29], the varying surface roughness amplitude Δ , with the other material parameters kept unchanged, was taken into account. Subsequently, we quoted a physically based Coulomb-limited mobility model due to ionized impurity atoms in a substrate [30] as follows:

$$\mu_C = \frac{1.1 \times 10^{21} T_n^{1.5}}{\ln(1 + \gamma_{BH}^2) - \frac{\gamma_{BH}^2}{1 + \gamma_{BH}^2}} \frac{1}{N_{sub}} \quad (2)$$

where $\gamma_{BH}^2 = (2 \times 10^{19} / N_{inv} / z) T_n^2$ is the Brooks–Herring coefficient, $T_n = (T/300 \text{ K})$ is the normalized temperature T with respect to 300 K, and z is the average inversion layer thickness as can be determined by simulated wave functions. Consequently, the thick oxide effective mobility can be obtained according to Matthiessen's rule as

$$\frac{1}{\mu_{thick}} = \frac{1}{\mu_C} + \frac{1}{\mu_{univ}}. \quad (3)$$

Care must be taken while experimentally applying Matthiessen's rule [31], [32]. This issue will be addressed later.

With the aforementioned process parameters as inputs, thick oxide effective mobility was obtained for three temperatures of 233, 263, and 298 K, as plotted in Fig. 4, versus E_{eff} for Δ of 1.4, 1.6, 1.8, and 2 Å. It can be seen that for $E_{eff} > 0.7 \text{ MV/cm}$, the calculated effective mobility approaches the universal one, as expected. While comparing the measured effective mobility μ_{eff} in the figure, the additional scattering of inversion layer electrons by remote scatterers in the polysilicon region can be assessed according to Matthiessen's rule as follows:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{thick}} + \frac{1}{\mu_{add}} \quad (4)$$

where μ_{thick} is the thick gate oxide mobility in the absence of remote scatterers, and μ_{add} is the additional mobility caused solely by remote scatterers. Again, the validity of (4) will be treated later. The resulting additional mobility values are shown in Fig. 5 for the three temperatures versus E_{eff} with the surface roughness amplitude Δ as a parameter. In addition, produced simultaneously is the temperature coefficient η , as defined by

$$\eta = \frac{\mu_{add}(233 \text{ K}) - \mu_{add}(298 \text{ K})}{233 \text{ K} - 298 \text{ K}}. \quad (5)$$

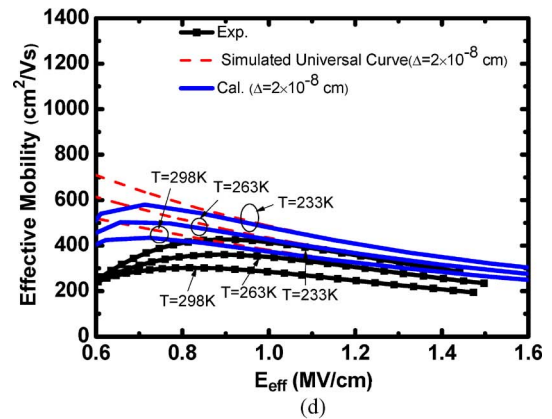
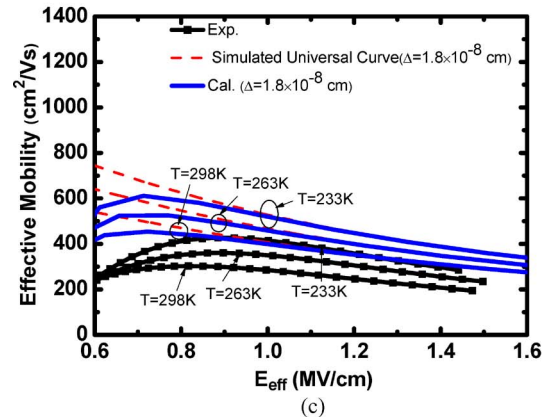
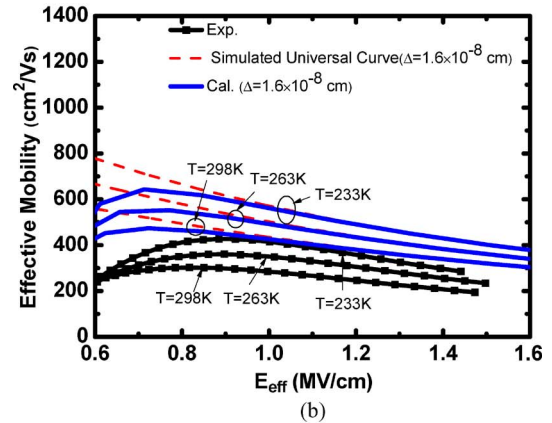
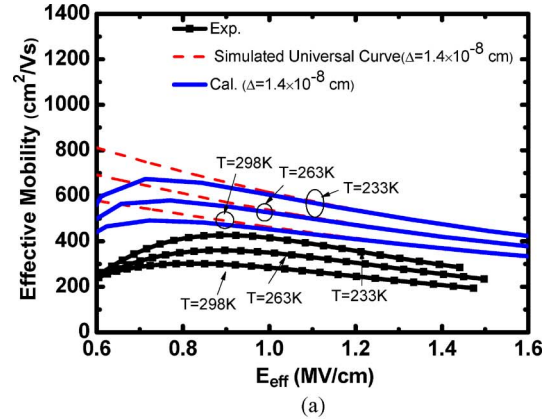


Fig. 4. Calculated effective mobility (solid lines), simulated universal mobility curves (dotted lines), and measured effective mobility (lines with symbols) for the three temperatures of 233, 263, and 298 K, plotted versus vertical effective electric field for (a) $\Delta = 1.4 \text{ \AA}$, (b) $\Delta = 1.6 \text{ \AA}$, (c) $\Delta = 1.8 \text{ \AA}$, and (d) $\Delta = 2 \text{ \AA}$.

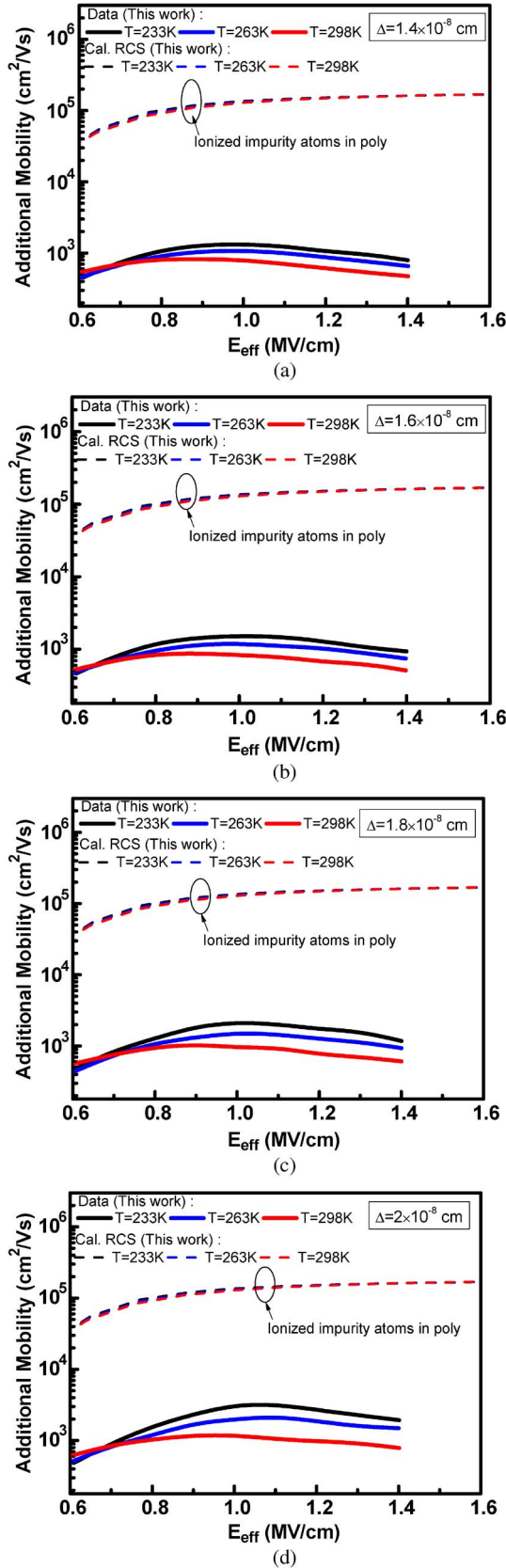


Fig. 5. Experimentally assessed additional mobility for the three temperatures, plotted versus the vertical effective electric field for (a) $\Delta = 1.4 \text{ \AA}$, (b) $\Delta = 1.6 \text{ \AA}$, (c) $\Delta = 1.8 \text{ \AA}$, and (d) $\Delta = 2 \text{ \AA}$. In addition, shown is the calculated RCS-limited mobility (dotted lines) due to ionized impurity atoms in a polysilicon depletion region for three different temperatures.

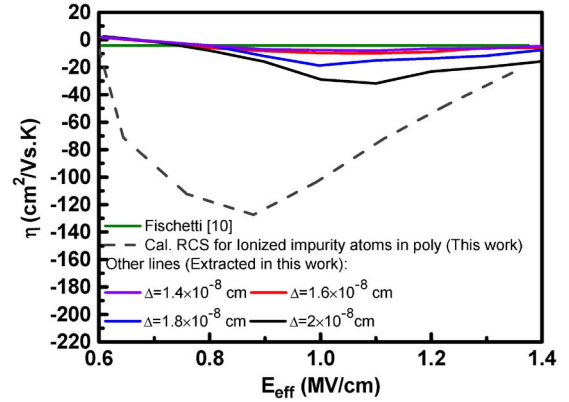


Fig. 6. Comparison of the temperature coefficient of the extracted additional mobility (solid lines) in this paper with that of the calculated RCS-limited mobility (dotted lines) due to ionized impurity atoms in a polysilicon depletion region. In addition, labeled is the possible range where the simulated temperature coefficient [10] yielded a value of $-4.15 \text{ cm}^2/\text{V} \cdot \text{s} \cdot \text{K}$.

The calculated temperature coefficient η is given in Fig. 6, plotted versus E_{eff} for different Δ values.

III. ORIGIN AND EVIDENCE

From Fig. 5, it can be seen that in a universal mobility dominant region, as aforementioned ($E_{\text{eff}} > 0.7 \text{ MV/cm}$), additional mobility increases with decreasing temperature, regardless of Δ used. This constitutes the merits of the proposed method, without the knowledge of realistic surface roughness parameters. We attribute the observed increasing trend with decreasing temperature to interface plasmons [6] in the presence of electrons in a polysilicon depletion region. The explanations are given below.

First, a positive temperature coefficient may be expected for ionized impurity atoms in a poly side, but owing to decreased screening with increasing temperature, the trend is likely to be reversed [30]. To examine this, we quoted the detailed formula by Yang *et al.* [7] to calculate remote-Coulomb-limited mobility due to ionized impurity atoms in a polysilicon depletion region. The results are separately plotted in Figs. 5 and 6. Fig. 5 clearly points out that the calculated remote-Coulomb-limited mobility due to ionized impurity atoms in a poly side is around two orders of magnitude larger than the experimentally extracted one. In Fig. 6, the calculated η value due to ionized impurity atoms in a polysilicon depletion region also exhibits a large discrepancy. Thus, we must rule out the possibility of ionized impurity atoms in a polysilicon depletion region.

Then, remote surface roughness scattering can be insignificant in a mobility universality dominant region ($E_{\text{eff}} > 0.7 \text{ MV/cm}$), as drawn from the Monte Carlo simulation by Gámiz *et al.* [11]. Thus, the origin of mobility degradation in this paper is determined to be interface plasmons [6]. This is reasonable because an increase in temperature can enhance absorption and emission of interface plasmons, which will in turn reduce inversion layer mobility. Extra evidence does exist. First, the published experimental [6]–[8] and simulated [10] mobility degradation values at room temperature [6]–[8] can deliver the additional mobility for comparison, as shown in Figs. 7 and 8. In the two figures, one can see that these additional mobility data created from different sources [6]–[8], [10] are all

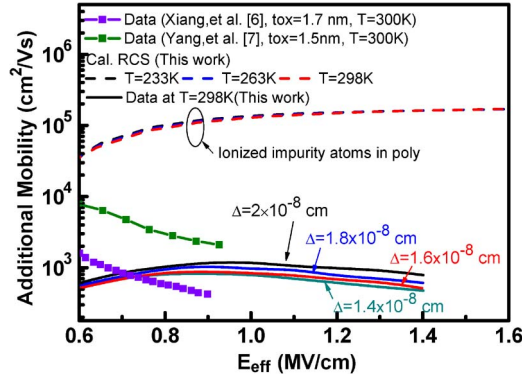


Fig. 7. Comparison of the experimentally extracted additional mobility (solid lines) near room temperature versus the effective field with that (lines with symbols) of [6] and [7]. In addition, shown is the calculated RCS-limited mobility (dotted lines) for the three different temperatures due to ionized impurity atoms in a polysilicon depletion region.

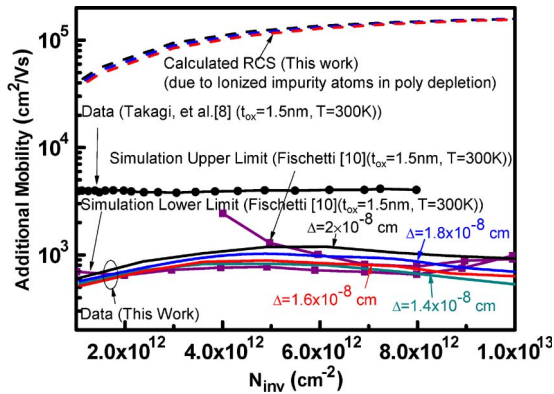


Fig. 8. Comparison of the experimentally assessed additional mobility (solid lines) near room temperature, plotted versus inversion layer electron density, with the simulated (lines with squares) remote-Coulomb-limited mobility due to interface plasmons [10], the experimentally extracted (line with circle) additional mobility from [8], and the calculated RCS-limited mobility (dotted lines for the three different temperatures) due to ionized impurity atoms in a polysilicon depletion region.

comparable with or close to ours, within the error of Matthiessen's rule, as will be explained later. In addition, it is noteworthy that the calculated remote Coulomb limited mobility due to ionized impurity atoms in a polysilicon depletion region is still too large to match the data [6]–[8], [10]. Particularly, we noticed that in the simulation study by Fischetti [10], simulated temperature-dependent mobility was available but only under limited conditions: the average electron density n_g of $3 \times 10^{19} \text{ cm}^{-3}$, the inversion layer electron density N_{inv} of 10^{13} cm^{-2} , and the gate oxide thickness t_{ox} of 1 nm. The corresponding η value was estimated to be $-4.15 \text{ cm}^2/\text{V} \cdot \text{s} \cdot \text{K}$ using the extracted values in [10]: $\mu(233 \text{ K}) \sim 900 \text{ cm}^2/\text{Vs}$ and $\mu(298 \text{ K}) \sim 630 \text{ cm}^2/\text{Vs}$. Strikingly, this value obtained in the context of interface plasmons is quite close to ours as long as the Δ value is smaller than 1.8 \AA , as demonstrated in Fig. 6.

Finally, we want to stress that the use of Matthiessen's rule in this paper is adequate. The primary reasons are that this paper is focused on a high E_{eff} value. To give a quantitative estimate of the error, extra work was done in calculating universal mobility according to Matthiessen's rule as follows:

$$\frac{1}{\mu_{univ}^i} = \left\langle \frac{1}{\mu_{ph}^i(E)} \right\rangle + \left\langle \frac{1}{\mu_{sr}^i(E)} \right\rangle. \quad (6)$$

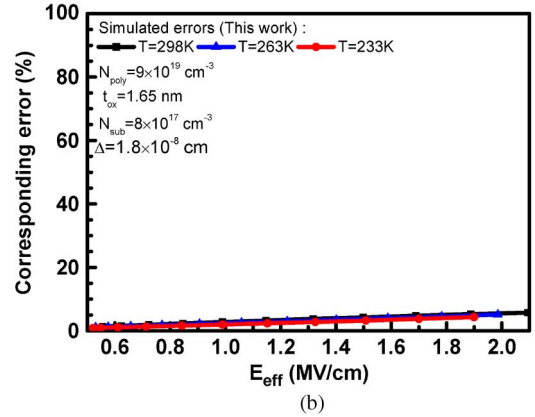
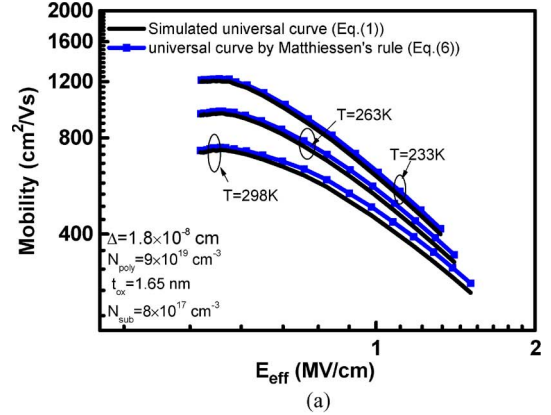


Fig. 9. (a) Comparison of the simulated universal mobility from two different formalisms (1) and (6), plotted versus E_{eff} with temperature as a parameter, and (b) the corresponding errors.

The results are given in Fig. 9 for comparison with those of (1), which are plotted versus E_{eff} with temperature as a parameter. Evidently, the maximum error of the universal mobility caused by the use of Matthiessen's rule is below merely 5%. This error is much less than the relative difference between the measured effective mobility and the simulated universal mobility in Fig. 3. Thus, the validity of Matthiessen's rule used in this paper is verified. Straightforwardly, the induced error may lead to the uncertainty of the extracted additional mobility. In this sense, the additional mobility data created from different sources [6]–[8], [10] all fall within the error of Matthiessen's rule.

IV. CONCLUSION

We have experimentally extracted the temperature-dependent additional electron mobility due to remote scatterers in n^+ -polysilicon ultrathin gate oxide nMOSFETs. Experimentally validated temperature-dependent universal mobility simulation has been highlighted. The resulting additional mobility has exhibited a negative temperature coefficient for the first time, thus confirming interface plasmons in a polysilicon depletion region to be the underlying remote Coulomb scatterers. The experimental and simulation evidence, as quoted in the open literature, has been demonstrated. The validity of Matthiessen's rule used in this paper has been verified.

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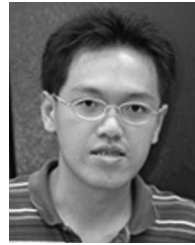
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