Channel Film Thickness Effect of Low-Temperature Polycrystalline-Silicon Thin-Film Transistors

William Cheng-Yu Ma, Tsung-Yu Chiang, Chi-Ruei Yeh, Tien-Sheng Chao, *Senior Member, IEEE*, and Tan-Fu Lei

***Abstract*—In this paper, the channel-film-thickness effect of low-temperature polycrystalline-Si thin-film transistors (LTPS-TFTs) is investigated. Greater channel film thickness can provide a higher field-effect mobility μ_{FE}, rising from 14.33 to 22.33 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, as the channel film thickness increases from 55 to 120 nm, due to grain-size effect. In addition, varying the channel film thickness of LTPS-TFTs results in different junction leakage current due to the source/drain (S/D) junction area effect. Moreover, the S/D series resistance also significantly increases when the channel film thickness is reduced from 120 to 35 nm, leading to poor field-effect mobility μ_{FE} and driving current. Consequently, the optimum channel film thickness for active-matrix liquid-crystal displays may be identified.**

***Index Terms*—Channel film thickness, low-temperature polycrystalline-Si thin-film transistors (LTPS-TFTs), scaling down.**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon thin-film transistors (LTPS-TFTs) have been widely used in active-matrix liquid-crystal displays (AMLCD) with integrated peripheral circuits as the pixel array on the glass substrate [1]–[5]. In addition, the 3-D integration of very large scale integration (VLSI) technology by the employment of LTPS-TFTs has been developed to increase the device density [6], [7]. However, polycrystalline-silicon channel film has many grain boundaries between the poly-grains, resulting in large numbers of defects and trap density state in the channel [8]–[10]. The defects in the trap density of the grain boundary create potential barriers that lower the conductance of polycrystalline silicon [11]. In order to increase the conductance of the polycrystalline silicon, a great quantity of carriers is required to lower the potential barrier, resulting in a large operating voltage for the LTPS-TFTs [8]–[10]. Therefore, the behavior and distribution of the trap density state in the channel are strongly related to the performance of LTPS-TFTs.

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Grain size enlargement of the polycrystalline-silicon channel film is a direct method for improving the performance of TFTs by reducing the defects and trap density of the polycrystalline-silicon channel film. Different grain sizes of polycrystalline-Si channel film may be fabricated by controlling the deposition pressure of polycrystalline Si [12]. A comprehensive grain-size effect has been studied by Dimitriadis and Tassis [12]. However, conventional LTPS-TFTs are fabricated by depositing an amorphous-silicon film and then crystallizing. Many crystallization methods, such as the solid-phase crystallization (SPC), metal-induced lateral crystallization, and excimer laser crystallization [13]–[15], have been used to enhance the performance of LTPS-TFTs.

In addition to the crystallization method, the channel film thickness also affects the grain size of the polycrystalline-silicon film [16]. Therefore, the optimum channel film thickness of LTPS-TFTs requires investigation. In this paper, the channel-film-thickness effects of LTPS-TFTs are studied. In addition to the grain-size effect found in previous research [16], the channel film thickness induces a series resistance effect and an anomalous leakage current trend. Moreover, the rolloff behavior of the field-effect mobility μ_{FE} and subthreshold swing S.S. are also investigated. Consequently, the optimum channel film thickness of LTPS for the application of AMLCD and 3-D integration of VLSI technology may be found.

II. Experimental Procedure

The devices used in this paper were first fabricated by depositing an undoped amorphous Si (α-Si) layer at 550 °C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers capped with a 500-nm thick thermal oxide layer. Three thicknesses of α-Si, i.e., 35, 55, and 120 nm, are chosen for the study of channel-film-thickness effect. Then, the α-Si layer was recrystallized by SPC process in a furnace at 600 °C for 24 h in N_2 ambient. After crystallization of the channel film, the active region was patterned by dry etching. A 50-nm gate oxide was then deposited using a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C. *In situ* N^+ doped α-Si of 250 nm was deposited by LPCVD at 550 °C as the gate electrode. After the patterning of the gate stack, the gate and source/drain (S/D) regions were implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24-h annealing in N_2 ambient. A 500-nm PECVD oxide was deposited for the passivation layer. After patterning of contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices. In order to study the intrinsic electrical properties of the LTPS-TFTs,

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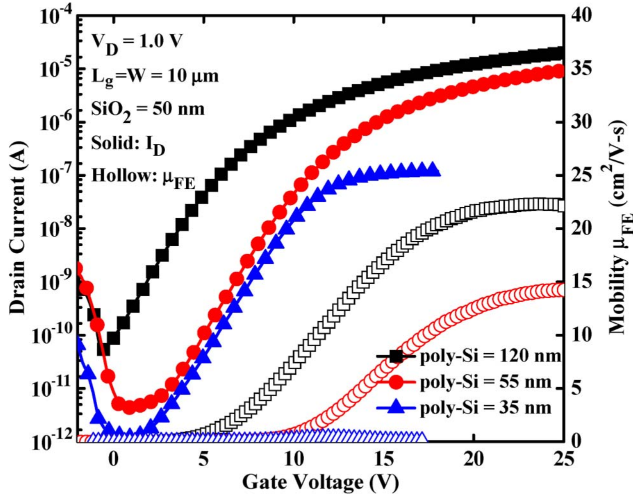

Fig. 1. Transfer curves (I_D–V_G) and field-effect mobility μ_{FE} of LTPS-TFTs with different channel film thicknesses and 50-nm gate oxide thickness.

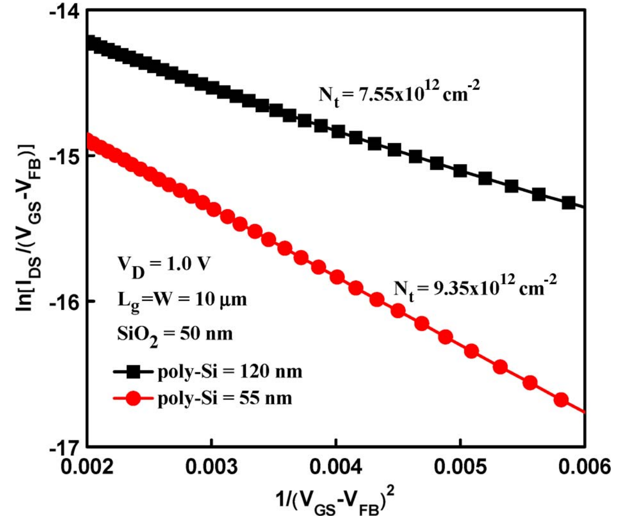

Fig. 2. Plot of $\ln[I_{DS}/(V_{GS}-V_{\mathrm{FB}})]$ versus $1/(V_{GS}-V_{\mathrm{FB}})^2$ curves at $V_{DS}=0.1$ V and high V_{GS}.

there was no passivation process in our fabrication of LTPS-TFTs. The threshold voltage V_{TH} was defined as the V_G at which the I_D reaches 100 nA $\times$ (W/L_g) and $V_D = 1.0$ V. The field-effect mobility μ_{FE} was extracted from the maximum transconductance G_m.

III. Results and Discussion

The transfer curves (I_D–V_G) and the field-effect mobility μ_{FE} of LTPS-TFTs with different channel film thicknesses and 50-nm gate oxide thickness are depicted in Fig. 1. Fig. 1 shows that the channel film thickness significantly affects the field-effect mobility μ_{FE} from 0.35 to 22.33 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ when the channel film thickness grows from 35 to 120 nm. The greater channel film thickness enables the formation of larger poly-grains after the crystallization of α-Si [16], [17]. The grain boundary trap state value N_{trap} is estimated by the Levinson and Proano method [18], [19], in which N_{trap} is extracted from the plot of the ln $[I_{DS}/(V_{GS}-V_{\mathrm{FB}})]$ versus $1/(V_{GS}-V_{\mathrm{FB}})^2$ curves at $V_{DS}=1.0$ V and high V_{GS}, as shown in Fig. 2. The flatband voltage V_{FB} is defined as the V_{GS}, yielding the minimum I_{DS} from the transfer characteristics I_D–V_G curve. Larger grain sizes of polycrystalline silicon have fewer grain boundaries and traps in the channel, resulting in higher field-effect mobility μ_{FE} of inversion carriers [20]. For TFTs of 120- and 55-nm channel film thickness, the latter have the smaller grain size, resulting in a high density of trap states and high barrier height of grain boundaries. A trap density state decreases the free charge, while a high grain boundary barrier height severely decreases the effective mobility.

In addition to the grain-size effect of channel film thickness on LTPS-TFTs, series resistance effect is also observed in the LTPS-TFT with 35-nm channel film thickness. The series resistance in the device with 35-nm channel film thickness causes a lower driving current and field-effect mobility μ_{FE}, as shown in Fig. 1. Fig. 3(a)–(c) show the S/D series resistances R_s extractions with the channel film thicknesses of 120, 55, and 35 nm, respectively. However, the V_{TH} of the 35-nm device may be misjudged due to its much lower driving current. In order to successfully extract the series resistance of the 35-nm device, we lower the definition current of V_{TH} to 10 nA $\times$ (W/L_g) for the 35-nm device. Compared with devices with channel film thicknesses of 55 and 120 nm, of which S/D series resistances R_s were 6.098 and 2.468 kΩ, respectively, a large S/D series resistance of ∼7973 kΩ is observed in the 35-nm channel film, as shown in Fig. 3(c). In addition, the subthreshold swing S.S. of the 35-nm channel film is also slightly higher than that of the 55- and 120-nm channel film, due to the impact of the large S/D series resistance R_s. In order to distinguish the impacts of the trap density and series resistance effects on the field-effect mobility μ_{FE} of the 35-nm channel film TFTs, the modified field-effect mobility μ'_{FE} is extracted by taking the series resistance into account as follows:

$$I_D = \frac{W}{L} C_{\mathrm{ox}} \mu_{\mathrm{eff}} (V_g - V_{\mathrm{TH}}) V_D \tag{1}$$

$$I_D = \frac{W}{L} C_{\mathrm{ox}} \mu'_{\mathrm{eff}} (V_g - V_{\mathrm{TH}}) V'_d \tag{2}$$

$$V'_d = V_D - I_D \times R_s \tag{3}$$

$$\mu'_{\mathrm{eff}} = \mu_{\mathrm{eff}} \times \frac{V_D}{V_D - I_D \times R_s}. \tag{4}$$

V_D is the total applied voltage. The voltage drop should occur in the series resistance and conductive channel of TFTs. V'_d is thus the real applied voltage across the channel of TFTs. Therefore, the modified field-effect mobility μ'_{FE} can be extracted without the impact of the series-resistance R_s effect, as shown in Table I. The important device parameters of the LTPS-TFTs with different channel film thicknesses are listed in Table I. The field-effect mobility μ_{FE} degrades about 4.6%, 6.8%, and 59.3% for TFTs with 120-, 55-, and 35-nm channel film thickness, respectively. Fig. 4 shows the I_D–V_D curve for LTPS-TFTs with 35-, 55-, and 120-nm channel film thickness. The driving current of the device with the 35-nm channel film thickness shows a lower current due to its low field-effect mobility μ_{FE} and poor S/D series resistance. In addition, the 120-nm channel film thickness device shows a higher current

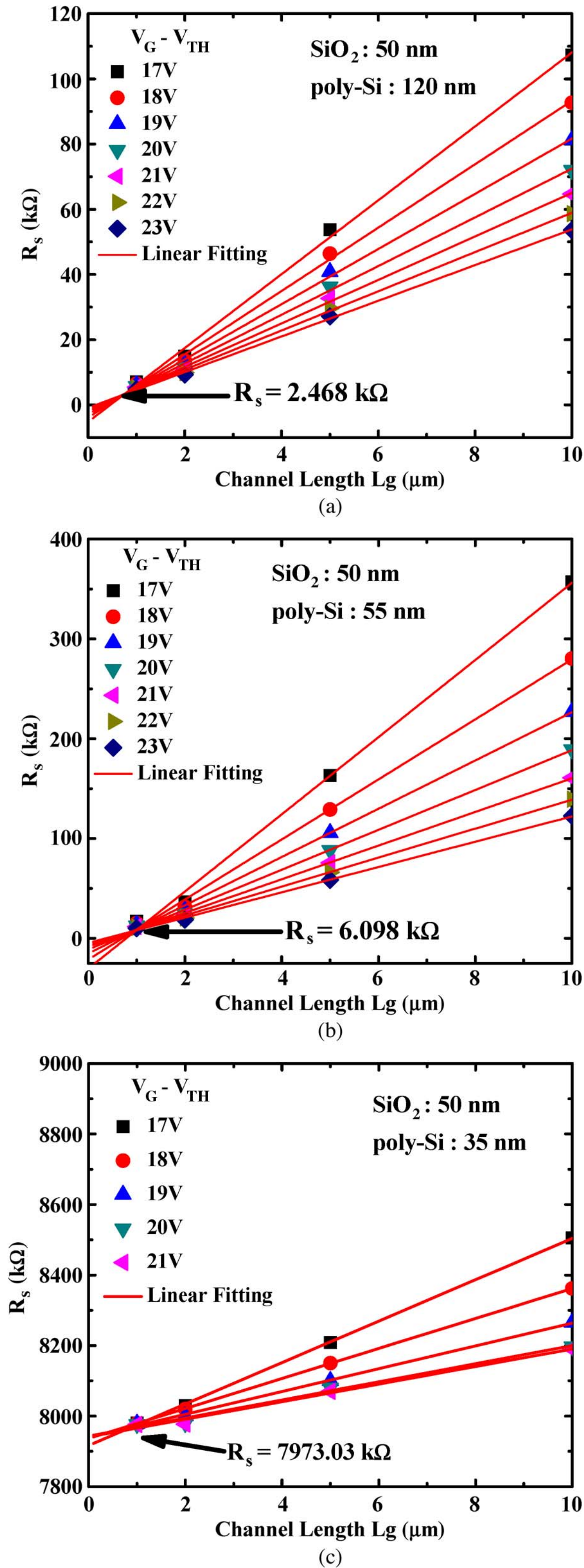

Fig. 3. (a)–(c) Extraction of S/D series resistances R_s for channel film thicknesses of 120, 55, and 35 nm, respectively.

TABLE I
IMPORTANT DEVICE PARAMETERS OF LTPS-TFTs WITH DIFFERENT CHANNEL FILM THICKNESSES, 50-nm GATE OXIDE THICKNESS, AND $W/L_g = 10\ \mu\text{m}/10\ \mu\text{m}$

Channel film thickness (nm)	V_{TH} (V)	S.S. (V/dec.)	μ_{FE} (cm²/V-s)	μ'_{FE} (cm²/V-s)	R_s (kΩ)	I_{on}/I_{min} (x10⁵)	I_{min} (pA)
120	5.92	1.813	22.33	23.40	2.468	4.53	53
55	10.87	1.797	14.33	15.37	6.098	27.96	4.4
35	N/A	1.867	0.35	0.86	7973.03	0.99	1.2

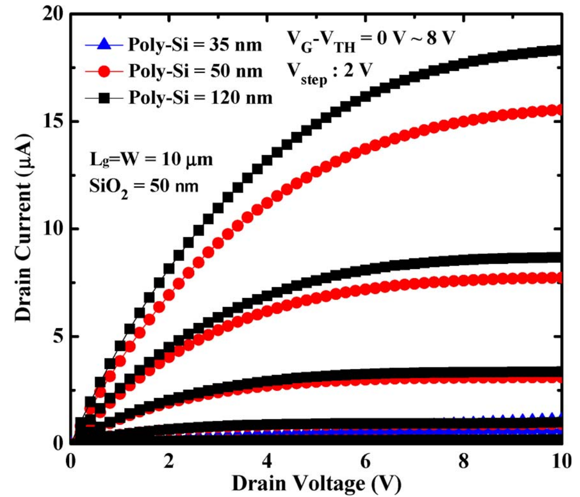

Fig. 4. I_D–V_D curve of LTPS-TFTs for 35-, 55-, and 120- nm channel film thicknesses.

due to the higher field-effect mobility μ_{FE} and a lower S/D series resistance.

In addition to the field-effect mobility μ_{FE} effect and the S/D series resistance effect of channel film thickness, the leakage current $I_{\min}$ is also affected by the channel film thickness. As shown in Fig. 1 and Table I, the device with 120-nm channel film thickness shows the highest leakage current $I_{\min} \sim 53$ pA, whereas the 55- and 35-nm devices show a lower leakage current $I_{\min}$ and ∼4.4 and 1.2 pA, respectively. The leakage current would be strongly related to the trap emission, which is a function of the electric field in the drain depletion region and the trap density of the grain boundaries [21]. When the channel film thickness decreases from 55 to 35 nm, the S/D series resistance significantly increases, as shown in Fig. 3(b) and (c), which decreases the lateral electric field in the drain depletion region [21], resulting in lower leakage current. On the other hand, the trap density of the grain boundary decreases when the channel film thickness increases from 55 to 120 nm due to the larger grain size. In addition, devices with thicker channel film show lower lateral electric fields in the drain depletion region [21], [22]. However, the leakage current $I_{\min}$ increases from 4.4 to 53 pA when the channel film thickness increases from 55 to 120 nm. Therefore, this high leakage current cannot be attributed to the traditional lateral electric field and trap density effects. The 120-nm channel film thickness provides a larger area of source and drain junction region in which the phosphorous of the S/D implantation is not distributed through whole polycrystalline-silicon thickness, as shown in Fig. 5, resulting in a higher junction leakage current for the 120-nm channel film thickness than the thinner channel film thicknesses of 55 and 35 nm [23]. Consequently, the 55-nm channel film thickness provides the highest $I_{\text{on}}/I_{\min}$ ratio of the three sizes in this paper, as shown in Fig. 1 and Table I.

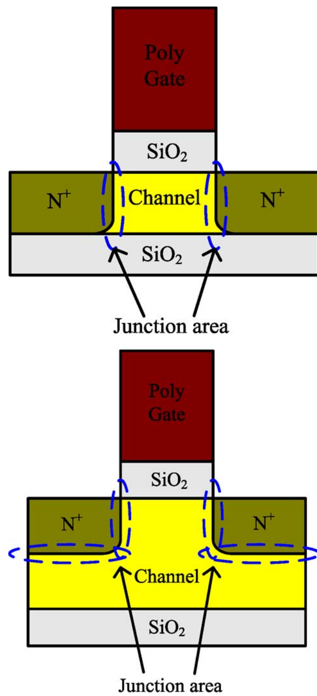

Fig. 5. Cross section of LTPS-TFTs with various channel film thicknesses.

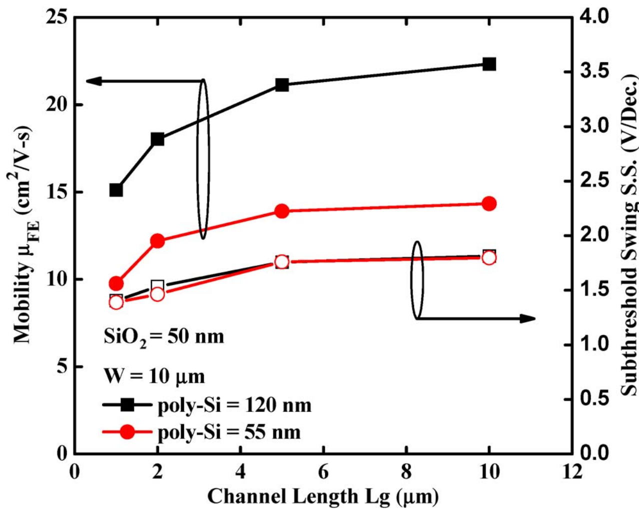

Fig. 6. Channel length L_g dependence of field-effect mobility μ_{FE} and subthreshold swing S.S. for 55- and 120-nm channel film thicknesses.

Fig. 6 shows the channel length L_g dependence of the field-effect mobility μ_{FE} and subthreshold swing S.S. for the 55- and 120-nm channel film thicknesses. The rolloff behavior of the field-effect mobility μ_{FE} is dominated by the S/D series resistance effect. As the channel length becomes smaller, the S/D series resistance decreases the drain voltage drop across the channel, resulting in lower driving current and field-effect mobility μ_{FE} [24]. Therefore, the rolloff percentage of the field-effect mobility μ_{FE} and the rolloff of the subthreshold swing S.S. is comparable for both 55- and 120-nm channel film TFTs, due to their similar S/D series resistance.

In sum, different channel film thicknesses between 50 and 120 nm of LTPS-TFTs would show comparable rolloff behavior of field-effect mobility μ_{FE} and subthreshold swing.

IV. Conclusion

The impacts of channel film thickness on LTPS-TFTs have been investigated in this paper. Significant grain size, junction leakage, and S/D series resistance effects have been observed. Devices with a thicker channel film thickness have lower S/D series resistance and large grain size of channel film, providing higher field-effect mobility μ_{FE} and driving current. However, greater channel film thickness has a larger S/D junction area, resulting in higher junction leakage. By contrast, lower channel film thickness has smaller grain sizes and higher S/D series resistance, resulting in poor driving current. The comparison of the electrical behavior of LTPS-TFTs with different channel film thicknesses shows that a channel thickness of about 55 nm appears to be the optimum choice for AMLCDs and 3-D integration.

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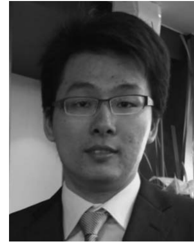

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