A Method of Extracting Metal-Gate High-k Material Parameters Featuring Electron Gate Tunneling Current Transition

Chih-Yu Hsu, *Student Member, IEEE*, Hua-Gang Chang, and Ming-Jer Chen, *Senior Member, IEEE*

***Abstract*—For metal-gate high-k dielectrics, there is a transition region in the electron gate tunneling current I_g, as characterized by a plot of $\mathrm{dlnI}_g/\mathrm{dV}_g$ versus V_g. In this paper, we systematically construct a new fitting over the region, which can accurately determine material parameters, including metal work function, high-k electron affinity, and tunneling effective masses of electrons. First of all, a calculation of gate current due to electron direct tunneling and/or Fowler–Nordheim tunneling from an inversion layer is performed, yielding the guidelines of the fitting. Experimental samples are presented with n-channel metal–oxide–semiconductor field-effect transistors having low effective oxide thickness (1.4 nm) TaC/HfSiON/SiON gate stacks. Underlying material parameters are extracted accordingly and remain valid for higher temperature and gate voltage. We also demonstrate that a conventional method without a $\mathrm{dlnI}_g/\mathrm{dV}_g$ fitting might lead to erroneous results. Thus, the $\mathrm{dlnI}_g/\mathrm{dV}_g$ fitting is crucial to metal-gate high-k material parameter assessment.**

***Index Terms*—HfSiON, high-k, metal gate, metal–oxide–semiconductor field-effect transistors (MOSFETs), tunneling.**

I. Introduction

OWING to dual advantages of eliminating polysilicon depletion and managing gate leakage current in a scaling direction, metal-gate high-k dielectrics are currently replacing conventional polysilicon gate oxide (SiO_2 or SiON) ones in metal–oxide–semiconductor field-effect transistor (MOSFET) manufacturing [1], [2]. Thus, it is imperative to experimentally construct a MOS system in terms of the following material and process parameters: metal work function, physical thickness, permittivity, and electron affinity of a high-k part and physical thickness, permittivity, and electron affinity of an interfacial layer (IL). In addition, the following conduction-related (tunneling in this paper) material parameters must be included as well: tunneling effective masses in a high-k layer and an IL. To achieve the goal, two standard methods [3]–[11] may be applied together: a fitting of gate capacitance C_g versus gate voltage V_g and a fitting of gate tunneling current I_g versus V_g. However, to further ensure precision of extraction results, use of other methods may be needed.

Recently, Zafar *et al.* [12] have proposed one such method in terms of a plot of $\mathrm{dlnI}_g/\mathrm{dV}_g$ versus V_g valid only for I_g dominated by direct tunneling and/or Fowler–Nordheim (F–N) tunneling. According to Zafar *et al.* [12], a peak of $\mathrm{dlnI}_g/\mathrm{dV}_g$ indicates a transition of direct tunneling and F–N tunneling across a high-k part, and as a consequence, the position of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ peak over V_g can provide a direct estimate of metal work function and high-k electron affinity. This unique feature was also applied elsewhere [13], [14]. However, other features concerning the height of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ peak and the shape of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ curve around the peak were not yet addressed to date. In addition, guidelines needed for the fitting in the context of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ method were lacking.

In this paper, we propose a new fitting technique dedicated to the $\mathrm{dlnI}_g/\mathrm{dV}_g$ method, along with a combination of conventional C_g–V_g and I_g–V_g fittings. First of all, a calculation of gate current due to electron direct tunneling and/or F–N tunneling from an inversion layer is carried out, leading to the guidelines of the fitting. Experimental samples are presented in terms of n-channel MOSFETs (nMOSFETs) with low effective oxide thickness (EOT) (1.4 nm) TaC/HfSiON/SiON gate stacks. Underlying material parameters are assessed accordingly, followed by corroborating evidence.

II. Simulations and Guidelines

The energy band diagram of a metal-gate/high-k/IL/p-type substrate MOS system in flatband condition is schematically shown in Fig. 1. In the figure, the relevant material and process parameters are labeled as follows: Φ_m for the metal work function; t_k, ε_k, and χ_k for the physical thickness, permittivity, and electron affinity of the high-k layer, respectively; t_{IL}, $\varepsilon_{\mathrm{IL}}$, and χ_{IL} for the physical thickness, permittivity, and electron affinity of the IL, respectively; and χ_s for the silicon electron affinity. Band offsets with respect to silicon φ_k and φ_{IL} are equal to $\chi_s - \chi_k$ and $\chi_s - \chi_{\mathrm{IL}}$, respectively. In addition, labeled in Fig. 1 are those associated with tunneling conduction: the tunneling effective masses of electrons m_k^* for the high-k layer and m_{IL}^* for the IL. These parameters now serve as model parameters in the calculation of electron gate tunneling current from the inversion layer.

Manuscript received September 17, 2010; revised November 23, 2010; accepted January 2, 2011. Date of publication January 31, 2011; date of current version March 23, 2011. This work was supported by the National Science Council of Taiwan under Contract NSC 97-2221-E-009-155-MY3. The review of this paper was arranged by Editor S. Deleonibus.

C.-Y. Hsu and M.-J. Chen are with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: chenmj@faculty.nctu.edu.tw).

H.-G. Chang is with the Ministry of National Defense, Taipei 10048, Taiwan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2105270

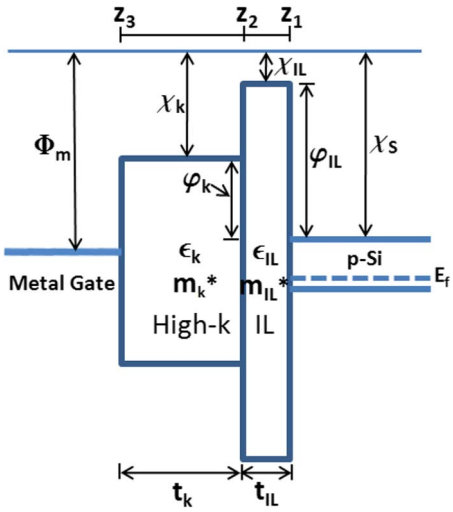


Fig. 1. Schematic of the energy band diagram of the metal-gate/high-k/IL/p-Si system biased in flatband condition. The process and material parameters involved in this paper are labeled.

Here, we slightly modified an existing triangular-potential-based quantum simulator, as already established in our previous work on polysilicon gate oxide stacks [15], [16]. This change was made primarily through the Wentzel–Kramers–Brillouin (WKB) transmission probability T_{WKB} given by

$$T_{\mathrm{WKB}} = \exp\left[-2\left(\int_{z_1}^{z_2}\kappa_1(z)dz + \int_{z_2}^{z_3}\kappa_2(z)dz\right)\right] \quad (1)$$

where z_1, z_2, and z_3 indicate the IL/Si, high-k/IL, and metal/high-k interfaces, respectively; and $\kappa_1(z)$ and $\kappa_2(z)$ are the magnitude of an imaginary wave vector in a forbidden band gap of the IL and the high-k layer, respectively. It is a straightforward task to derive analytic models for T_{WKB} according to the four tunneling criteria φ_1, φ_2, φ_3, and φ_4, as depicted in Fig. 2. Here, φ_1 and φ_2 represent the difference of high-k conduction-band sidewall edges with respect to a tunneling stream from the level E of the subband j and the valley i, and φ_3 and φ_4 represent the difference of the IL conduction-band sidewall edges with respect to the tunneling stream. In case 1 ($\varphi_1(E) > 0$, $\varphi_2(E) > 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), where direct tunneling prevails in both layers, T_{WKB} from the subband j of the valley i is the product of two direct tunneling probabilities for the layers in series as follows:

$$T_{\mathrm{WKB}} = \exp\left[\frac{4\sqrt{2m_k}\left(\varphi_1^{3/2}(E) - \varphi_2^{3/2}(E)\right)}{3q\hbar F_k}\right] \times \exp\left[\frac{4\sqrt{2m_{\mathrm{IL}}}\left(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E)\right)}{3q\hbar F_{\mathrm{IL}}}\right] \quad (2)$$

where F_k and F_{IL} are the electric field in the high-k layer and the IL, respectively. In case 2 ($\varphi_1(E) < 0$, $\varphi_2(E) > 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), the tunneling in the high-k layer is the F–N tunneling, and thus, T_{WKB} is the product of one direct tunneling probability and one F–N tunneling probability as follows:

$$T_{\mathrm{WKB}} = \exp\left[\frac{4\sqrt{2m_k}\left(-\varphi_2^{3/2}(E)\right)}{3q\hbar F_k}\right] \times \exp\left[\frac{4\sqrt{2m_{\mathrm{IL}}}\left(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E)\right)}{3q\hbar F_{\mathrm{IL}}}\right]. \quad (3)$$

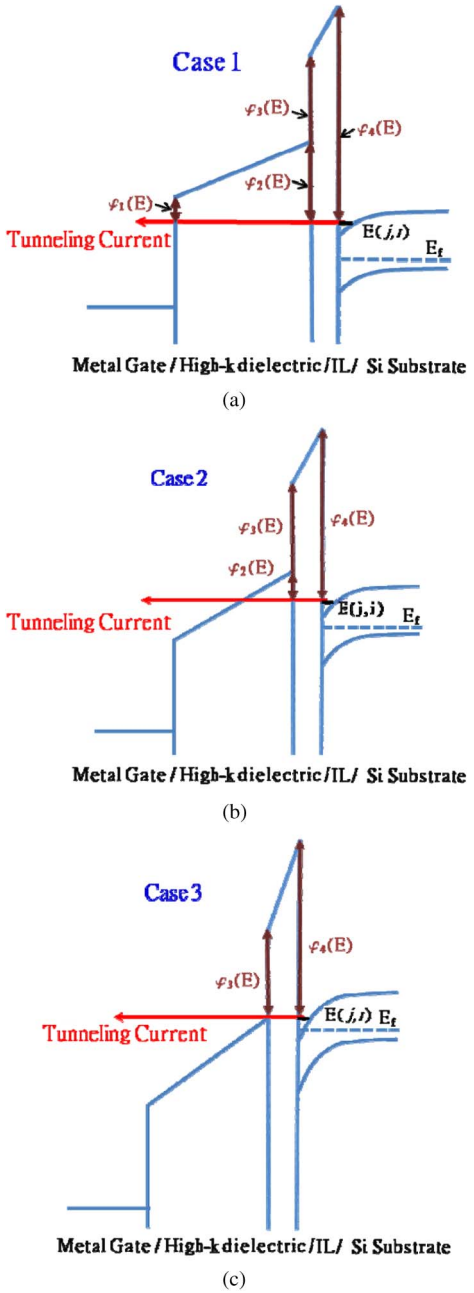


Fig. 2. Schematic description. (a) Tunneling case 1: direct tunneling through both the high-k layer and the IL. (b) Tunneling case 2: F–N tunneling occurring in the high-k layer. (c) Tunneling case 3: only direct tunneling through the IL.

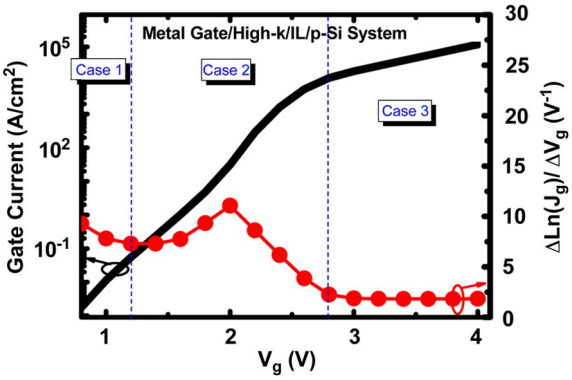


Fig. 3. Simulated gate current and $\mathrm{dlnI}_g/\mathrm{dV}_g$ in a wide range of gate voltage up to 4 V. The parameters used in the calculation are the following: $\Phi_m = 4.48$ eV, $\varphi_k = 1.65$ eV, $\varphi_{\mathrm{IL}} = 3.15$ eV, $m_k^* = 0.18$ $\mathrm{m_o}$, $m_{\mathrm{IL}}^* = 0.5$ $\mathrm{m_o}$, $t_k = 2$ nm, $t_{\mathrm{IL}} = 1$ nm, $\varepsilon_k = 12.4\,\varepsilon_0$, and $\varepsilon_{\mathrm{IL}} = 3.9\,\varepsilon_0$.

In case 3 ($\varphi_1(E) < 0$, $\varphi_2(E) < 0$, $\varphi_3(E) > 0$, $\varphi_4(E) > 0$), only the IL undergoes tunneling, and the T_{WKB} simply becomes

$$T_{\mathrm{WKB}} = \exp\left[\frac{4\sqrt{2m_{\mathrm{IL}}}\left(\varphi_3^{3/2}(E) - \varphi_4^{3/2}(E)\right)}{3q\hbar F_{\mathrm{IL}}}\right]. \quad (4)$$

Finally, the electron tunneling current from all the populations in the inversion layer can be calculated as

$$J = q\sum_{i,j} f(j,i)g_{2D}\int_{E(j,i)}^{\infty} F(E)T_{\mathrm{WKB}}(E)T_R(E)dE. \quad (5)$$

Here, formulas used to calculate the electron impact frequency f, the density of states per unit area for the 2-D electron gas g_{2D}, the Fermi–Dirac distribution function F, and the reflection correction factor T_R were the same as those in [15]. Note that in this paper, T_R was limited to the IL/Si interface. The reasons are that the reflection at the high-k/IL interface, as well as between the metal and high-k interface, is quite weak and thus is neglected in the calculation. Fig. 3 shows the calculated I_g and $\mathrm{dlnI}_g/\mathrm{dV}_g$ versus V_g values to highlight these different tunneling cases.

The calculated I_g and $\mathrm{dlnI}_g/\mathrm{dV}_g$ values are plotted in Fig. 4 versus V_g with one of the model parameters as a variable. The nominal values of the model parameters in the calculation are $\Phi_m = 4.48$ eV, $\varphi_{\mathrm{IL}} = 2.36$ eV, $\varphi_k = 1.1$ eV, $m_{\mathrm{IL}}^* = 0.95$ $\mathrm{m_o}$, $m_k^* = 0.03$ $\mathrm{m_o}$, $t_{\mathrm{IL}} = 1.3$ nm, $t_k = 2.2$ nm, $\varepsilon_{\mathrm{IL}} = 7\,\varepsilon_0$, and $\varepsilon_k = 12.4\,\varepsilon_0$. By careful observation of the calculated $\mathrm{dlnI}_g/\mathrm{dV}_g$ curves in Fig. 4, relevant guidelines can be drawn. First, m_k^*, t_k, t_{IL}, m_{IL}^*, ε_k, and $\varepsilon_{\mathrm{IL}}$ can adjust the height of the peak but with different trends. The peak is nearly vertically raised with increasing m_k^*, t_k, t_{IL}, m_{IL}^*, and ε_k, whereas the height of the peak decreases with increasing $\varepsilon_{\mathrm{IL}}$. Specifically, m_k^* is the most effective factor in changing the height of the peak. Note that m_k^*, t_k, t_{IL}, m_{IL}^*, $\varepsilon_{\mathrm{IL}}$, and ε_k are all weak in producing a horizontal shift of the peak.

Second, an increase in Φ_m or φ_k can give rise to a horizontal shift in the position of the peak toward the increasing V_g direction. Only for φ_k can a simultaneous change in the height of the peak be noticed. Relatively, Φ_m produces little change in the height of the peak. Third, the shape of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ curve around the peak can be characterized by a decay from the peak until a saturation of about 2 to 5 V^{-1} in the increasing gate voltage direction. It can be seen that all the parameters have the comparable shape of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ curve, except m_k^*, i.e., the shape of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ curve is only sensitive to m_k^*. Finally, the $\mathrm{dlnI}_g/\mathrm{dV}_g$ curve around the peak is independent of φ_{IL}.

III. Experimental and Fitting

The presented samples were nMOSFETs with TaC/HfSiON/SiON gate stacks, as fabricated in a state-of-the-art process [17]. In this process [17], nominal physical thicknesses of SiON and HfSiON were around 1.3 and 2.2 nm, respectively. The following process parameters were obtained by a C_g–V_g fitting using the Schrödinger–Poisson equation solver Schred [18], as depicted in Fig. 5: the metal work function Φ_m of 4.48 eV, the EOT of 1.4 nm, and the p-type substrate doping concentration of 3×10^{17} cm^{-3}. The channel width and length of the device were 10 and 1 μm, respectively. The threshold voltage extracted from the measured drain current at $V_d = 0.025$ V was found to be in agreement with that by Schred (not shown here). Then, we took the permittivity of the hafnium silicate HfSiON ε_k as the literature value of 12.4 ε_0 [17] and reasonably assumed the permittivity of SiON $\varepsilon_{\mathrm{IL}}$ to be 7 ε_0. The corresponding IL/Si interface barrier height φ_{IL} is 2.36 eV, as determined from the published relationship between the SiON permittivity and its electron affinity [19]. Here, we want to stress that, owing to the unknown nitrogen concentration in the IL and the possible process-induced thickness variation, the uncertainties in the values of $\varepsilon_{\mathrm{IL}}$ and φ_{IL}, as well as t_{IL} and t_k, exist, as will be addressed later.

The gate current was measured with the source, the drain, and the substrate tied to the ground. The measured results are depicted in Fig. 6 versus V_g. To confirm whether the measured I_g stems from pure (direct or F–N) tunneling, temperature-dependent measurement was conducted. The results are shown in Fig. 7. Apparently, two distinct tunneling mechanisms occur. I_g for $V_g > 1$ V slightly increases with temperature as a result of pure tunneling, whereas for $V_g < 1$ V, I_g significantly increases due to trap-assisted tunneling. Thus, in the subsequent analysis, the fitting will be devoted to the region of $V_g > 1$ V.

At this point, all the model parameters are known, except φ_k, m_k^*, and m_{IL}^*. Initially, we fit the I_g data in a gate voltage range of 1 to 2 V. By following the guidelines above, the fitting process can be straightforward as follows: 1) First, adjust φ_k to shift the fitting curve of $\mathrm{dlnI}_g/\mathrm{dV}_g$ versus V_g until the position of the peak is close to the experimental value ($\sim$1.5 V); 2) then, adjust m_k^* until the height of the $\mathrm{dlnI}_g/\mathrm{dV}_g$ peak approaches the experimental value (~ 7 V^{-1}); and 3) finally, adjust m_{IL}^* until the fitting I_g versus V_g curve matches the experimental one. The extracted results are $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ $\mathrm{m_o}$, and $m_{\mathrm{IL}}^* = 0.95$ $\mathrm{m_o}$. The fitting quality is good, as displayed in Fig. 6, for both I_g and $\mathrm{dlnI}_g/\mathrm{dV}_g$ versus V_g. The extracted φ_k value is quantitatively reasonable, as compared with the literature value [20]. In addition, it has been reported [21]–[23] that the effective mass of the electrons tunneling through a $\mathrm{SiO_2}$

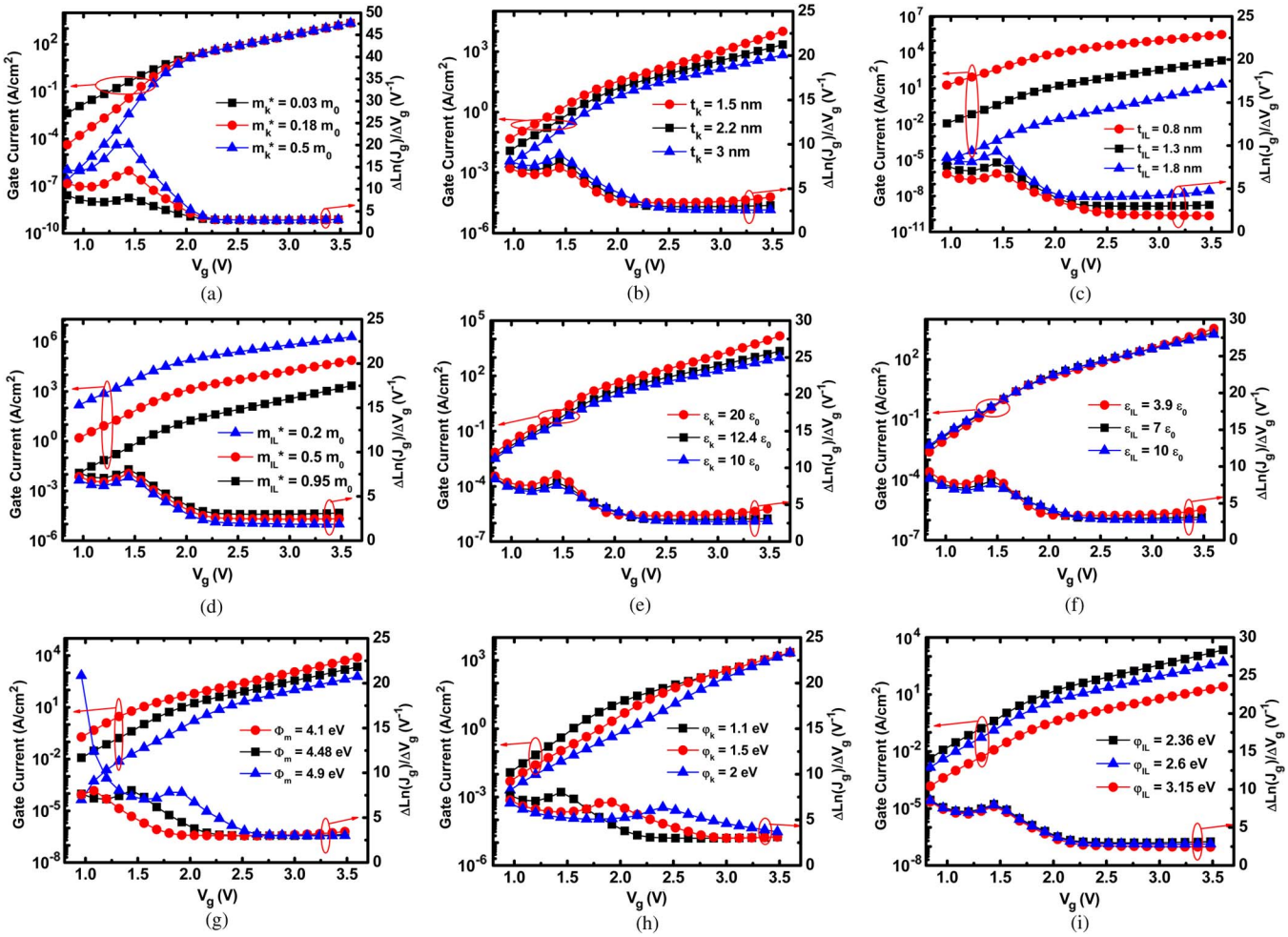


Fig. 4. Simulated gate current I_g and $\mathrm{dln}I_g/\mathrm{dV}_g$ versus V_g for (a) varying m_k^*, (b) t_k, (c) t_{IL}, (d) m_{IL}^*, (e) ε_k, (f) $\varepsilon_{\mathrm{IL}}$, (g) Φ_m, (h) φ_k, and (i) φ_{IL}.

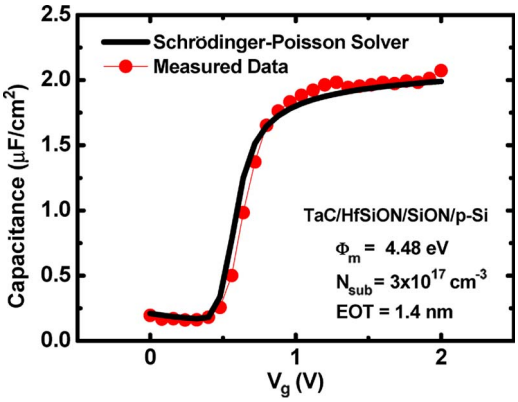


Fig. 5. Experimental (symbol) and simulated (line) C_g versus V_g.

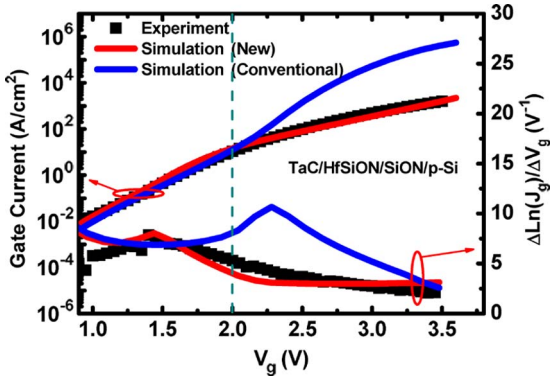
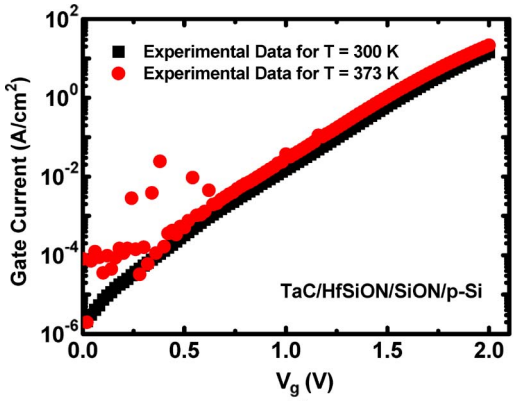


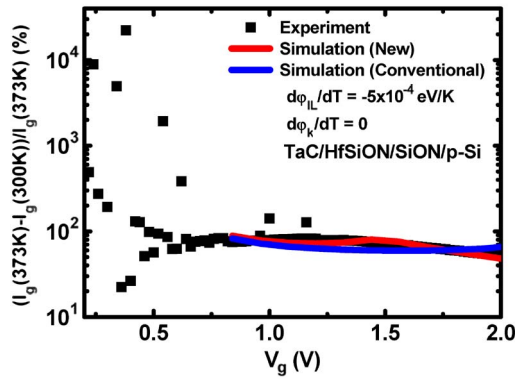
Fig. 6. Comparison of the experimental (symbols) gate current and $\mathrm{dln}I_g/\mathrm{dV}_g$ versus V_g with calculated (lines) results using two sets of parameters. Red line (new method): $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ $\mathrm{m_o}$, and $m_{\mathrm{IL}}^* = 0.95$ $\mathrm{m_o}$. Blue line (conventional method): $\varphi_k = 1.9$ eV, $m_k^* = 0.18$ $\mathrm{m_o}$, and $m_{\mathrm{IL}}^* = 0.3$ $\mathrm{m_o}$. Other parameters are $t_{\mathrm{IL}} = 1.3$ nm and $t_k = 2.2$ nm.

or a silicon oxynitride gate insulator increases significantly with decreasing gate dielectric thickness, thus supporting the very high value of the extracted m_{IL}^* in this paper.

The extracted electron tunneling effective mass m_k^* in the presented HfSiON sample appears to be rather low. This is the unconventional value relative to the published one (0.24 $\mathrm{m_o}$ [8]). To address this issue, we performed a second fitting with m_k^* fixed at a typical value of 0.18 $\mathrm{m_o}$. The best fitting can again be obtained in I_g versus V_g characteristics for gate voltage smaller than 2 V, leading to $\varphi_k = 1.9$ eV and $m_{\mathrm{IL}}^* = 0.3$ $\mathrm{m_o}$. This is the well-known conventional fitting technique. However, as shown in Fig. 6, the shape of the calculated $\mathrm{dln}I_g/\mathrm{dV}_g$ curve around the peak is exactly opposite to the measured one, particularly for the gate voltage less than 2 V. Therefore, the conventional method without the $\mathrm{dln}I_g/\mathrm{dV}_g$ fitting might lead to erroneous results. This also dictates that the tunneling



(a)



(b)

Fig. 7. (a) Measured gate current at $T = 300$ and 373 K versus gate voltage for TaC/HfSiON/SiON nMOSFETs. (b) Comparison of simulated (line) gate current change of $T = 373$ K with respect to $T = 300$ K versus V_g with measured data (symbols). The parameters used to create the red line (new method) and the blue line (conventional method) in Fig. 6 are also used here.

effective mass in the high-k layer is process dependent. The same argument was also mentioned elsewhere [24].

IV. Extra Evidence

To testify to the validity of the new fitting, extra work was done. First, the experimental I_g value was fitted with increasing V_g up to 3.5 V, as shown in Fig. 6. We found that the above extracted values of $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ m_o, and $m_{IL}^* = 0.95$ m_o remain valid in such a wide V_g range along with the same fitting quality for both I_g and $\mathrm{dln}I_g/\mathrm{d}V_g$ versus V_g. However, this is not the case for the conventional fitting technique. As clearly shown in Fig. 6, the conventional fitting fails in the whole V_g range. Thus, a wide V_g measurement range can help to justify the validity of the fitting scheme.

The second evidence concerns the reproduction of the temperature effect. The quantum simulator aforementioned was again executed with the same material and process parameters as those obtained in the new fitting technique. In this simulator, the published temperature dependence was incorporated into the IL/Si interface barrier height φ_{IL} and silicon band gap E_g as follows: $d\varphi_{IL}(T)/\mathrm{dT} = -5 \times 10^{-4}$ eV/K and $E_g(T) = E_0 - (\alpha T^2/T + \beta) + E_x$, where $E_x = 10^{-2}$ eV, $E_0 = 1.17$ eV, $\alpha = 4.73 \times 10^{-4}$ eV/K, and $\beta = 636$ K [25]. The results are given in Fig. 7(b). Good agreement with the data not only supports the extracted parameters in the context of the $\mathrm{dln}(I_g)/\mathrm{d}V_g$ method but also reconfirms the origin of tunneling for $V_g > 1$ V. In addition, shown in Fig. 7(b) is the case of the conventional method using the same temperature dependence of φ_{IL} and E_g. Clearly, the new fitting method is closer to the data than the conventional one.

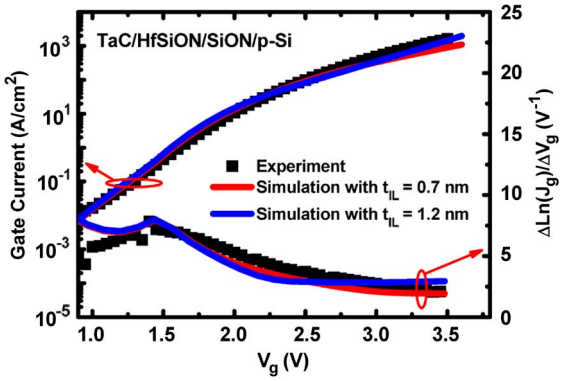


Fig. 8. Comparison of the experimental (symbols) gate current and $\mathrm{dln}I_g/\mathrm{d}V_g$ versus V_g with calculated (lines) results using two sets of t_k and t_{IL} for the same EOT (1.4 nm). Red line: $t_{IL} = 0.7$ nm, $t_k = 3.2$ nm and $m_{IL}^* = 2.8$ m_o. Blue line: $t_{IL} = 1.2$ nm, $t_k = 2.3$ nm, and $m_{IL}^* = 1.1$ m_o. Other parameters are $m_k^* = 0.03$ m_o and $\varphi_k = 1.1$ eV.

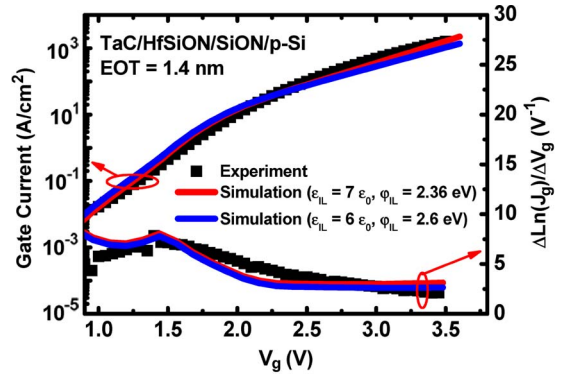


Fig. 9. Comparison of the experimental (symbols) gate current and $\mathrm{dln}I_g/\mathrm{d}V_g$ versus V_g with calculated (lines) results using two sets of ε_{IL} and φ_{IL}. The same EOT (1.4 nm) is preserved. Red line: $m_{IL}^* = 0.95$ m_o, and $t_{IL} = 1.3$ nm. Blue line: $m_{IL}^* = 1.15$ m_o, and $t_{IL} = 1.1$ nm. Other parameters are $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ m_o, and $t_k = 2.2$ nm.

Until now, we can examine the uncertainty issue. First, the uncertainty of IL thickness t_{IL} was done with two different values of t_{IL}: 0.7 and 1.2 nm. The corresponding t_k values were 3.2 and 2.3 nm such as to meet the EOT value. The fitting results are plotted in Fig. 8, leading to $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ m_o, and $m_{IL}^* = 2.8$ m_o for $t_{IL} = 0.7$ nm and $t_k = 3.2$ nm; and $\varphi_k = 1.1$ eV, $m_k^* = 0.03$ m_o, and $m_{IL}^* = 1.1$ m_o for $t_{IL} = 1.2$ nm and $t_k = 2.3$ nm. Strikingly, the extracted m_k^* value is equal to 0.03 m_o, regardless of the t_{IL} used under the same EOT. This is also the case for the uncertainty in ε_{IL} and φ_{IL}, as demonstrated in Fig. 9. Fig. 9 reveals that even with the different sets of ε_{IL} and φ_{IL}, only with m_k^* equal to 0.03 m_o can a good fitting be obtained. Finally, one might think the possible origin of the unconventional m_k^* value in this paper in terms of the potential drop in the remainder of the high-k conduction band on which the electrons propagate (not tunneling but classical conduction, as shown in cases 2 and 3 in Fig. 2). To take this into account, an additional calculation was

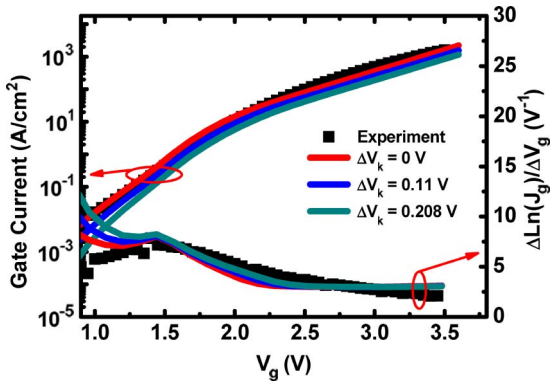


Fig. 10. Comparison of the experimental (symbols) gate current and $\mathrm{dln}\mathrm{I}_g/\mathrm{dV}_g$ versus V_g with calculated (lines) results with the potential drop in the high-k dielectric ΔV_k as a parameter. Fitting parameters: $\Phi_m = 4.48$ eV, $\varphi_k = 1.1$ eV, $\varphi_{\mathrm{IL}} = 2.36$ eV, $m_k^* = 0.03\,\mathrm{m_o}$, $m_{\mathrm{IL}}^* = 0.95\,\mathrm{m_o}$, $t_k = 2.2$ nm, $t_{\mathrm{IL}} = 1.3$ nm, $\varepsilon_k = 12.4\,\varepsilon_0$, and $\varepsilon_{\mathrm{IL}} = 7\,\varepsilon_0$.

done, and the results were given in Fig. 10 with the potential drop, denoted as ΔV_k, in the high-k region as a parameter. Obviously, good agreement with the data can be achieved with the same m_k^* value regardless of the potential drop in the high-k layer.

V. Conclusion

To accurately extract the material and process parameters in the metal-gate high-k dielectrics, we have systematically constructed a new fitting scheme over the $\mathrm{dln}\mathrm{I}_g/\mathrm{dV}_g$ versus V_g curve, along with the combination of the C_g–V_g and I_g–V_g fittings. With the guidelines created for the fitting in the experimental samples with low EOT TaC/HfSiON/SiON gate stacks, the underlying material and process parameters have been extracted. The extracted results have been verified by extra measurement at higher temperature and gate voltage. The uncertainties encountered in the determination of some process parameters have been adequately clarified. In addition, we have demonstrated that the conventional method without the $\mathrm{dln}\mathrm{I}_g/\mathrm{dV}_g$ fitting might lead to erroneous results. Thus, the $\mathrm{dln}\mathrm{I}_g/\mathrm{dV}_g$ fitting should be taken into account in the assessment of the metal-gate high-k material parameters.

References

[1] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging," in *IEDM Tech. Dig.*, Dec. 2007, pp. 247–250.

[2] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C.-H. Chang, V. Chikarmane, M. Childs, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, I. Jin, C. Kenyon, S. Klopcic, S.-H. Lee, M. Liu, S. Lodha, B. McFadden, A. Murthy, L. Neiberg, J. Neirynck, P. Packan, S. Pae, C. Parker, C. Pelto, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, K. Tone, T. Troeger, C. Weber, M. Yang, A. Yeoh, and K. Zhang, "A 32 nm logic technology featuring 2nd-generation high-k+ metal-gate transistors, enhanced channel strain and 0.171 μm^2 SRAM cell size in a 291 Mb array," in *IEDM Tech. Dig.*, Dec. 2008, pp. 941–943.

[3] M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaeghe, and M. M. Heyns, "Determination of tunneling parameters in ultra-thin oxide layer poly-Si/$\mathrm{SiO_2}$/Si structures," *Solid State Electron.*, vol. 38, no. 8, pp. 1465–1471, Aug. 1995.

[4] B. Brar, G. D. Wilk, and A. C. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin $\mathrm{SiO_2}$," *Appl. Phys. Lett.*, vol. 69, no. 18, pp. 2728–2730, Oct. 1996.

[5] W. J. Zhu, T. P. Ma, T. Tamagawa, J. Kim, and Y. Di, "Current transport in metal/hafnium oxide/silicon structure," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 97–99, Feb. 2002.

[6] Y. T. Hou, M. F. Li, H. Y. Yu, and D. L. Kwong, "Modeling of tunneling currents through $\mathrm{HfO_2}$ and $(\mathrm{HfO_2})_x(\mathrm{Al_2O_3})_{1-x}$ gate stacks," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 96–98, Feb. 2003.

[7] F. Li, S. P. Mudanai, Y. U. Fan, L. F. Register, and S. K. Banerjee, "Physically based quantum–mechanical compact model of MOS devices substrate-injected tunneling current through ultrathin (EOT $\sim$ 1 nm) $\mathrm{SiO_2}$ and high-k gate stacks," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1096–1106, May 2006.

[8] A. Campera, G. Iannaccone, and F. Crupi, "Modeling of tunneling currents in Hf-based gate stacks as a function of temperature and extraction of material parameters," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 83–89, Jan. 2007.

[9] J. Coignus, R. Clerc, C. Leroux, G. Reimbold, G. Ghibaudo, and F. Boulanger, "Analytical modeling of tunneling current through $\mathrm{SiO_2}-\mathrm{HfO_2}$ stacks in metal oxide semiconductor structures," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 27, no. 1, pp. 338–345, Jan./Feb. 2009.

[10] S. Monaghan, P. K. Hurley, K. Cherkaoui, M. A. Negara, and A. Schenk, "Determination of electron effective mass and electron affinity in $\mathrm{HfO_2}$ using MOS and MOSFET structures," *Solid State Electron.*, vol. 53, no. 4, pp. 438–444, Apr. 2009.

[11] J. Coignus, C. Leroux, R. Clerc, G. Ghibaudo, G. Reimbold, and F. Boulanger, "Experimental investigation of transport mechanisms through $\mathrm{HfO_2}$ gate stacks in nMOS transistors," in *Proc. ESSDERC*, Sep. 2009, pp. 169–172.

[12] S. Zafar, C. Cabral, R. Amos, and A. Callegari, "A method for measuring barrier heights, metal work functions and fixed charge densities in metal/$\mathrm{SiO_2}$/Si capacitors," *Appl. Phys. Lett.*, vol. 80, no. 25, pp. 4858–4860, Jun. 2002.

[13] H. C. Wen, R. Choi, G. A. Brown, T. Böscke, K. Matthews, H. R. Harris, K. Choi, H. N. Alshareef, H. Luan, G. Bersuker, P. Majhi, D. L. Kwong, and B. H. Lee, "Comparison of effective work function extraction methods using capacitance and current measurement techniques," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 598–601, Jul. 2006.

[14] J. A. Rothschild, H. Avraham, E. Lipp, and M. Eizenberg, "Tunneling of holes observed at work function measurements of metal/$\mathrm{HfO_2}$/$\mathrm{SiO_2}$/n-Si gate stacks," *Appl. Phys. Lett.*, vol. 96, no. 12, pp. 122 102-1–122 102-3, Mar. 2010.

[15] K. N. Yang, H. T. Huang, M. C. Chang, C. M. Chu, Y. S. Chen, M. J. Chen, Y. M. Lin, M. C. Yu, S. M. Jang, D. C. H. Yu, and M. S. Liang, "A physical model for hole direct tunneling current in $\mathrm{P^+}$ poly-gate PMOSFETs with ultrathin gate oxides," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2161–2166, Nov. 2000.

[16] C. Y. Hsu, C. C. Lee, Y. T. Lin, C. Y. Hsieh, and M. J. Chen, "Enhanced hole gate direct tunneling current in process-induced uniaxial compressive stress p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1667–1673, Aug. 2009.

[17] Y. T. Hou, F. Y. Yen, P. F. Hsu, V. S. Chang, P. S. Lim, C. L. Hung, L. G. Yao, J. C. Jiang, H. J. Lin, Y. Jin, S. M. Jang, H. J. Tao, S. C. Chen, and M. S. Liang, "High performance tantalum carbide metal gate stack for nMOSFET application," in *IEDM Tech. Dig.*, Dec. 2005, pp. 31–34.

[18] Schred. [Online]. Available: http://nanohub.org/resources/schred

[19] H. Yu, Y. T. Hou, M. F. Li, and D. L. Kwong, "Investigation of hole-tunneling current through ultrathin oxynitride/oxide stack gate dielectrics in p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 7, pp. 1158–1164, Jul. 2002.

[20] Y. Kamimuta, M. Koike, T. Ino, M. Suzuki, M. Koyama, Y. Tsunashima, and A. Nishiyama, "Determination of band alignment of hafnium silicon oxynitride/silicon (HfSiON/Si) structures using electron spectroscopy," *Jpn. J. Appl. Phys.*, vol. 44, no. 3, pp. 1301–1305, Mar. 2005.

[21] Khairurrijal, W. Mizubayashi, S. Miyazaki, and M. Hirose, "Unified analytic model of direct and Fowler–Nordheim tunnel currents through ultrathin oxides," *Appl. Phys. Lett.*, vol. 77, no. 22, pp. 3580–3582, Nov. 2000.

[22] Khairurrijal, W. Mizubayashi, S. Miyazaki, and M. Hirose, "Analytic model of direct tunnel current through ultrathin gate oxides," *J. Appl. Phys.*, vol. 87, no. 6, pp. 3000–3005, Mar. 2000.
[23] E. Nadimi, C. Golz, M. Trentzsch, L. Herrmann, K. Wieczorek, and C. Radehaus, "Tunneling effective mass of electrons in lightly n-doped SiO_xN_y gate insulators," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2462–2468, Sep. 2008.
[24] L. F. Mao, "Investigation of the correlation between temperature and enhancement of electron tunneling current through HfO_2 gate stacks," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 782–788, Mar. 2008.
[25] A. Hadjadj, G. Salace, and C. Petit, "Fowler–Nordheim conduction in polysilicon (n^+)-oxide-silicon (p) structures: Limit of the classical treatment in the barrier height determination," *J. Appl. Phys.*, vol. 89, no. 12, pp. 7994–8001, Jun. 2001.

Chih-Yu Hsu (S'07) received the B.S. degree in electrophysics from National Chiao Tung University, Hsinchu, Taiwan, in 2005. He is currently working toward the Ph.D. degree in electronics engineering with the Department of Electronics Engineering, National Chiao Tung University.

His research interests include the characterization and modeling of metal-gate high-k strained metal–oxide–semiconductor field-effect transistors as well as trap physics in nanoscale devices.

Hua-Gang Chang received the B.E. degree in electrical engineering from National Chung Cheng University, Chiayi, Taiwan, in 2008 and the M.S. degree in electronics engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2010.

He is currently performing the military service. His research interests include the characterization and modeling of tunneling currents in high-k gate stacks.

Ming-Jer Chen (S'78–M'79–SM'98) received the B.S. (with highest honors) degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1977 and the M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University (NCTU), Hsinchu, Taiwan, in 1979 and 1985, respectively.

In 1985, he was with the Department of Electronics Engineering, NCTU, and, in 1993, became a Full Professor. From 1987 to 1992, he was a Consultant with Taiwan Semiconductor Manufacturing Company, Hsinchu, where he led a team from NCTU and Electronics Research and Service Organization/Industrial Technology Research Institute to build up a series of process windows and design rules. From 2000 to 2001, he was a Visiting Professor with the Department of Electrical Engineering and the Center for Integrated Systems, Stanford University, Stanford, CA. He is the holder of eight U.S. patents and six Taiwanese patents in the field of high-precision analog capacitors, single-transistor memory cells, dynamic threshold metal–oxide–semiconductor, electrostatic discharge protection, and Flash memory. He has graduated 16 Ph.D. students and more than 100 M.S. students. His current research interests include device physics, trap physics, and reliability physics, all in the area of nanoelectronics.

Dr. Chen is a member of the Phi Tau Phi.