行政院國家科學委員會專題研究計畫　期中進度報告

III-V族薄膜和晶格無缺陷技術在高頻、光電元件的應用及3D矽積體電路的整合(1/3)

計畫類別：個別型計畫
計畫編號：NSC94-2215-E-009-062-
執行期間：94年08月01日至95年07月31日
執行單位：國立交通大學電子工程學系及電子研究所

計畫主持人：荊鳳德

報告類型：精簡報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 95 年 5 月 25 日

行政院國家科學委員會專題研究計畫 成果報告

III-Ⅴ族薄膜和晶格無缺陷技術在高頻、光電元件的應用及3D矽積體電路的整合(1/3)

計畫類別： 整合型計畫
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執行期間： 94 年08 月01 日至95 年07 月31 日
執行單位： 國立交通大學電子工程學系暨電子研究所

計畫主持人： 荊鳳德

報告類型： 完整報告

處理方式： 本計畫可公開查詢

中 華 民 國 95 年8 月2 日

行政院國家科學委員會補助專題研究計畫

□成果報告■期中進度報告

（計畫名稱）

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執行期間： 94 年 8 月 1 日至 95 年 7 月31 日

計畫主持人：荊鳳德

共同主持人：

計畫參與人員：

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

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執行單位：交通大學電子所

中 華 民 國 九十五 年 五 月 二十四 日

行政院國家科學委員會研究計畫成果報告

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主持人：荊鳳德 教授 執行單位：交通大學電子工程系

中文摘要

隨著 VLSI COMS 尺度的微小化，所造成的技術阻礙主要有兩方面，一方面是電晶體漏電流所造成的直流功率消耗，另一方面則為內連線寄生電容所造成的交流功率消耗。

我們在此提出一個已經證實的新式 VLSI 結構，是利用一種 3D 整合(積體)的方法來解決這些問題，3D 整合的方式是在傳統的 1P6M 內連線和 0.18um 的 Si MOSFETs 上，藉由 GOI MOSFETs 上的金屬-閘極/high-k 的閘極介電材料來加以實現。具有 IrO2 and IrO2/Hf 雙功函數閘極和 high k 材 LaAlO3 閘極介電層的新式閘極結構，比使用 SiO2 閘極介電層的閘極結構，在 1.4nm 的 EOT 下，大幅降低了近 4 個 order 的漏電流，也因此能大幅減少 p-MOSFET 閘極的直流功率消耗。

Silicon 元件上的 3D 金屬-閘極/high k GOI MOSFET 可以提供一個與高效能 RF 被動元件相整合的平台，這些較高基板損耗和較差 Q-factor 的元件，可利用由選擇性離子植入所製的高阻值的基材或轉移製程所製的半絕緣 Si 來加以克服。由傳輸線、誘導器 (inductor)、濾波器 (filters)、共振器 (resonators)和天線所組成的高效能 RF 被動元件已經完成，元件頻率在 100GHz 以上，相當接近於，在半絕緣的 GaAs 上的元件和理想 3D 電磁模擬所得的頻率。

在等效元件尺度縮小下，金屬-閘極/high k/GOI MOSFET 的頂層將具有更高的 3D 積體密度，和 2.2-2.4 倍高的驅動電流。因此能夠在量子力學極限下，等效地延伸二維 Silicon CMOS 的尺度。對於在尺度縮小所致的 fab 成本快速增加，等效的尺度縮小和 3D GOI/Si 結構的低製程成本，也是一種有潛力的解決方法。

一、簡介

The down-scaling Complementary Metal-Oxide-Semiconductor Field-Effective Transistors (CMOSFETs), shown schematically in Fig. 1(a), gives not only higher integration density but also higher transistor drive current for a faster switching speed of integrate circuit (IC). Since the drive current of sub-100 nm scale MOSFET is proportional to the gate dielectric capacitor/area ($C_{ox}=\varepsilon_0\kappa/t_{ox}$), higher drive current can be obtained by scaling down the t_{ox} to give more efficient channel charges control by gate voltage- the higher trans-conductance. Unfortunately, the down-scaling t_{ox} into recent 1.2 nm thickness generates high leakage current density from the quantum-mechanical direct tunneling, which becomes intolerable in highly integrated ICs and prohibits further scaling down due to the exponential relation with t_{ox} of $\exp(-\beta t_{ox}/V_{ox})$. Therefore, a cooling system is required to remove the heat from the gate leakage current generated DC power

consumption in advanced ICs, but becomes less effective to remove the increasing heat dispersion as increasing circuit density and shrinking transistor size.

Another difficult challenge for high density VLSI ICs is the AC power consumption in parasitic capacitance ($Cv^2f/2$) of backend interconnects. Figure 1(b) shows the schematic diagram of the 1-Poly-Si-6-Metal (1P6M) interconnects on bottom Si CMOSFETs that are the basic building blocks for modern VLSI ICs. The circuit delays in interconnect becomes the dominate factor of whole IC speed as compared with that in CMOSFETs. The interconnects also consume AC power in high density ICs, but unfortunately the higher operational frequency (f) and interconnect density are the desired technology trend for both microprocessors and communication ICs. Currently, high IC operation frequency up to 10.6 GHz is required for Ultra-Wide Band application. Although the wireless and optical interconnect [1]-[2] has been reported, these approaches mainly work for inter-chip connect rather than solving the AC power consumption in the high density interconnects. As extensively discussed in International Electron Devices Meeting (IEDM) 2003 panel section, no clear solution or approach has been proposed so far.

Finally, the ultimate challenge for VLSI technology is the gradually reaching the scaling limit of CMOSFETs (<10 nm) due to the source-drain quantum-mechanical direct tunneling [3]-[4]. This large tunneling current will also consume large DC power similar to gate dielectric tunneling current, although the scaling below 10 nm is still several technology nodes behind or about half decade long beyond the current 90 nm technology. It is important to notice that the stopping scaling means no more performance or density improvement in VLSI technology, since the higher drive current and integration density are the driven force for continuously scaling down the CMOS technology. In addition, the fast increasing fab cost with down scaling is another limitation from economic point of view, although the higher speed and integration density ICs are always needed.

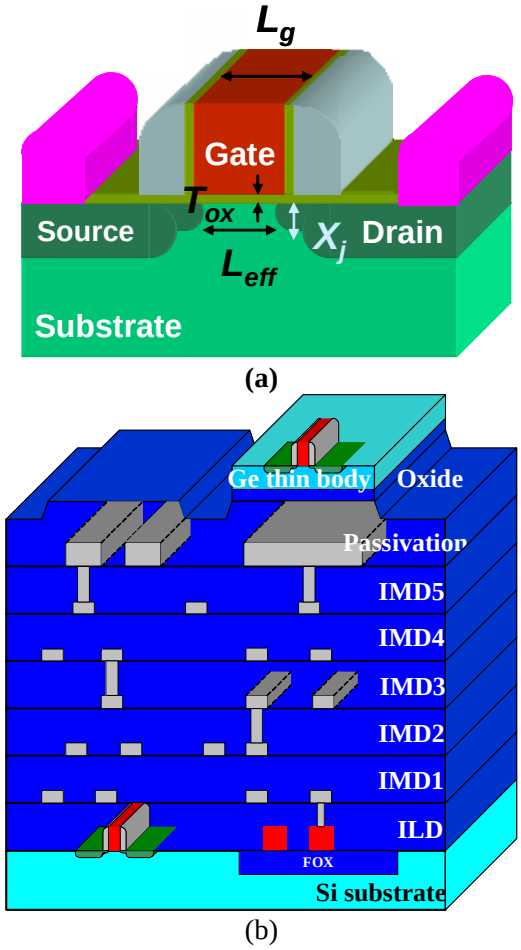

Fig. 1. The schematic diagrams of (a) a MOSFET and (b) an IC structure with lower layer Si CMOSFETs and top layers 1-Poly-Si-6-Metal interconnects. The requirements for MOSFETs are the high drive current, low leakage current and high integration density. The 3D integration of top metal-gate/high-κ/GOI CMOSFETs can equivalently solve the difficult challenges of DC power consumption in gate leakage current, AC power consumption in interconnects and scaling limit of 2D CMOSFETs

二、實驗步驟

The down-scaling Complementary

Metal-Oxide-Semiconductor Field-Effective Transistors (CMOSFETs), shown schematically in Fig. 1(a), gives not only higher integration density but also higher transistor drive current for a faster switching speed of integrate circuit (IC). Since the drive current of sub-100 nm scale MOSFET is proportional to the gate dielectric capacitor/area ($C_{ox}=\varepsilon_0\kappa/t_{ox}$), higher drive current can be obtained by scaling down the t_{ox} to give more efficient channel charges control by gate voltage- the higher trans-conductance. Unfortunately, the down-scaling t_{ox} into recent 1.2 nm thickness generates high leakage current density from the quantum-mechanical direct tunneling, which becomes intolerable in highly integrated ICs and prohibits further scaling down due to the exponential relation with t_{ox} of $\exp(-\beta t_{ox}/V_{ox})$. Therefore, a cooling system is required to remove the heat from the gate leakage current generated DC power consumption in advanced ICs, but becomes less effective to remove the increasing heat dispersion as increasing circuit density and shrinking transistor size.

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In this paper, we have shown a simple and affective method to address all these difficult challenges by using three-dimensional (3D) integration. The 3D IC architecture is similar to the logic and memory functions in neurons of our 3D brain structure, which is much advanced and cost effective as compared with man-made 2D ICs. However, the fundamental challenge is how to realize the top layer 3D CMOSFETs without degrading the lower layer multi-layers interconnects and Si MOSFETs. To overcome this problem, we have used the low temperature processed

Ge-on-Insulator (GOI) to fabricate the 3D metal-gate/high-κ dielectric/GOI CMOSFETs above the 1P6M interconnects and 0.18 μm CMOSFETs. The reducing DC power consumption is evidenced from the ~4 orders of magnitude lower leakage current in 3D GOI CMOSFETs with dual metal-gates and high-κ dielectric. The AC power consumption and maximum operation frequency of IC can also be largely improved by this new 3D architecture from Electro-Magnetic calculation. Because the higher drive current and integration density are the driven force of continuously scaling down the CMOS, the higher 3D integration density and 2.2-2.4 times larger drive current in 3D GOI transistors than Si counterparts are equivalent to device scaling. Therefore, the 3D GOI/Si integration can equivalently extend CMOS scaling beyond the 2D quantum-mechanical limit, in addition to the much improved DC and AC power consumption by using high-κ gate dielectric and lowered interconnects density respectively. The 3D GOI/Si can also provide a platform for System-on-Chip (SoC) application, where high performance and low loss RF passive devices of transmission lines, inductors, filters and antenna, up to 100 GHz have been realized on Si using the developed local semi-insulating Si process. The equivalent down-scaling and low cost process using 3D GOI/Si IC is also the potential solution to the rapidly increasing fab cost above several billions of dollars and even more as continuously scaling down..

三、結果與討論

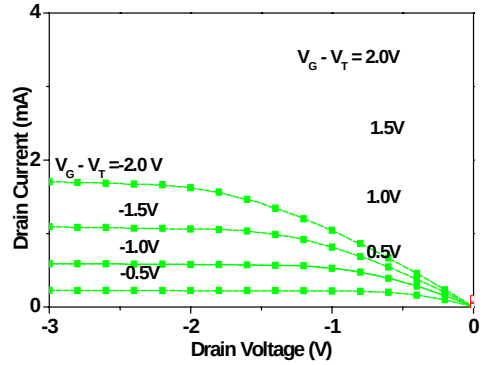
To overcome the DC power consumption and continue down-scaling the gate oxide thickness, high dielectric constant (κ) of metal-oxide [5]-[19] was proposed to reach a high C_{ox} ($\varepsilon_0\kappa/t_{ox}$) for high drive current but low leakage current due to the relatively thick t_{ox}. Equivalent-oxide thickness (EOT = $t_{ox}\times\kappa_{SiO2}/\kappa_{dieelctirc}$) below 1.0 nm [9]-[10], [18]-[19] has been reported using the high-κ dielectric with several orders of magnitude lower leakage current, indicating the successful reducing DC power consumption. Figures 2(a), 2(b) and 2(c) show I_d-V_d, I_g-V_g and C-V characteristics of the self-aligned metal-gate/high-κ/Si CMOSFETs using high-κ $LaAlO_3$ gate dielectric and novel IrO_2 and IrO_2/Hf dual metal gates respectively, which has the full process compatibility to current VLSI technology. The IrO_2 gate electrode has low resistivity metal property and also high work-function in the Periodic Table, which is an alternative metal gate in addition to the fully silicide [3], [14], [20]-[22] and metal-nitride [16]-[19] gates. Good I_d-V_d characteristics of p-MOSFETs have been obtained in Fig. 2(a) and the gate dielectric leakage current in Fig. 2(b) is ~4 orders of magnitude lower than SiO_2 at the EOT of 1.4 nm from C-V measurement shown in Fig. 2(c). This result demonstrates the successful reduction of DC power consumption from gate leakage current using high-κ gate dielectric and metal gate.

Note that the $LaAlO_3$ is one of the most advanced high-κ gate dielectrics with unique property to preserve high κ value (κ=25.1) close to La_2O_3 even by adding Al_2O_3 (κ=10), where much reduced κ value (κ~10-15) was reported in HfAlO(N) [11] or HfSiON [12] by adding the relative lower κ Al_2O_3 or SiN (κ~7) into HfO_2 (κ~22). The $LaAlO_3$ is also widely available commercially for superconductor application. The added Al, Si and N into HfO_2 are required for the transistors' Bias-Temperature Instability (BTI) improvement [11]-[12]; a non-desired phenomenon to increase the threshold voltage (V_t) of MOSFETs during continuous operation at a raised IC temperature from heat

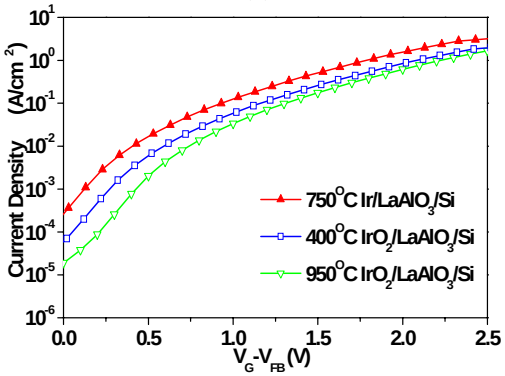
dissipation. The mechanism for BTI improvement may be due to the fact of stronger bond energy of these oxide or nitride than ionic Hf-O bond. In sharp contrast, good BTI of higher κ $LaAlO_3$ CMOSFETs was reported with 1.2 V operation voltage for 10 years lifetime at 85°C ambient [15], which meets the required 1 V operation of nanometer-scaled CMOSFETs. The unique higher κ value and good BTI suggest that the ternary $LaAlO_3$ is one of the best choices of high-κ gate dielectric.

For the metal gates study, the novel IrO_2 and IrO_2/Hf dual gate electrodes on $LaAlO_3$/Si p-MOSFETs provide not only the low leakage current (Fig. 2(b)) but also the proper work-functions. Fig. 3 shows the flat-band voltage (V_{fb}) as a function of EOT for IrO_2 and IrO_2/Hf dual gates on $LaAlO_3$/Si MOS capacitors. Note that the 5.1 eV work-function of IrO_2 gate on $LaAlO_3$/Si p-MOSFET is close to Ir and currently used p^+ poly-Si gate. The inserting low work-function Hf (3.5 eV) in IrO_2 on $LaAlO_3$/Si n-MOSFET can effectively reduce the work-function to 4.4 eV. In addition to the proper work-function, another difficult challenge for metal gate technology is the metal diffusion into the gate dielectric. It is known in the textbook that the metal contamination in SiO_2 gate dielectric on Si will increase the dielectric leakage current by generating conductive current pass and weakening the SiO_2 matrix. The low leakage current in IrO_2/$LaAlO_3$/Si devices of this work may be due to the perfect match of oxide gate electrode and oxide gate dielectric, in addition to the excellent metal diffusion barrier property of IrO_2 [26]. This is justified by the ~10 times lower leakage current in IrO_2 gate than metallic Ir gate shown in Fig. 2(b) and the 4 orders of magnitude lower gate leakage current than SiO_2 at the 1.4 nm EOT.

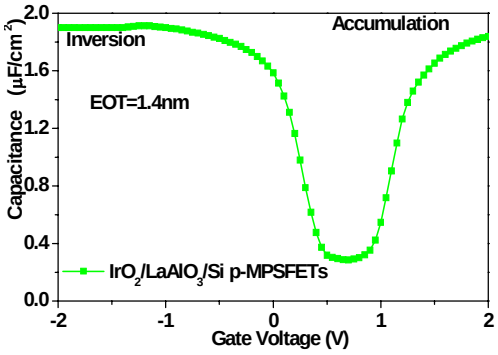
We propose the 3D integration to overcome this problem, which is similar to the neurons in our brain to provide very effective logic and memory functions beyond the man-made 2D ICs. Figures 4(a) shows the schematic of a 3D IC chip, where the interconnect distance, shown in the red lines, is reduced to half or even 1/4 by folding the 2D IC into the 3D structure by once or twice.



(a)



(b)



(c)

Fig. 2. (a) The I_d-V_d (b) I_g-V_g and (c) C-V characteristics for the [IrO_2-IrO_2/Hf]/$LaAlO_3$/Si 2D PMOSFETs. The gate length is 10 μm

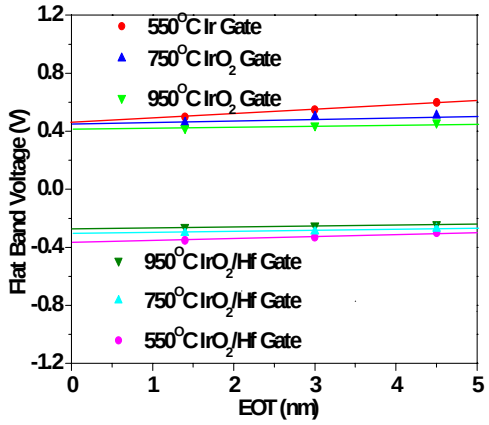


Fig. 3. The flat-band voltage and EOT plot for IrO_2 and IrO_2/Hf gate on $LaAlO_3$/Si after different RTA condition from 550 to 950°C.

We have used the Electro-Magnetic method to calculate the AC power consumption of the 3D IC structure shown in Fig. 1(b), where the additional layer of metal-gate/high-k/GOI p-MOSFETs is fabricated above the 1P6M interconnects and lower layer Si devices. Figures 4(b) shows the calculated signal coupling loss (S_{21}) and power loss ($1-|S_{21}|^2-|S_{11}|^2$) from the Scattering parameters, because no ideal open and short can be measured at high frequencies of other circuit parameters. The highest IC operation frequency is determined by the 3 dB (50%) loss of signal coupling or AC power consumption by the high density parallel lines. The operation frequency from signal coupling loss increases with increasing line spacing, which limits the interconnect density at high frequencies. We have used the 1 mm long line with a foundry provided 0.5 μm spacing technology to simulate the complicated and high-density interconnects. Under this condition, a maximum operating frequency of <20 GHz was obtained from the 3 dB signal coupling limitation. Therefore, further scaling down the interconnect spacing will become unacceptable in high density and high frequency 2D ICs due to the coupling loss and cross-talk. The maximum IC operation frequency is also limited by the AC power consumption to 20 GHz at the 1-mm long 0.5 μm spaced parallel lines, which can be increased to 40 GHz if using 3D architecture with additional IC layer. Much larger improvement of AC power consumption to ≤0.25 dB at 40 GHz is achieved using additional two layers ICs above bottom 1P6M interconnects and Si p-MOSFETs. The 3D integration is the only known technology to reduce the AC power consumption governed by fundamental physics of $CV_d^2f/2$, under the minimum operation voltage (V_d) condition for low power application.

However, the technology challenge is how to realize this 3D ICs shown in Fig. 1(b), with low thermal budget and small impact on lower-layer interconnects and Si p-MOSFETs. It is noticed that the metal-gate/high-κ/G p-MOSFETs OI p-MOSFETs [13]-[15] can meet the required low thermal budget of 500°C process and is ideal for the 3D ICs on modern Si P p-MOSFETs and multi-layer interconnects. Therefore, we have fabricated the self-aligned [IrO_2-IrO_2/Hf]/$LaAlO_3$/GOI p-MOSFETs on 1P6M interconnects and 0.18 μm Si p-MOSFETs. The measured I_d-V_d characteristics of the 3D [IrO_2-IrO_2/Hf]/$LaAlO_3$/GOI p-MOSFETs are shown in Figure 5. In addition to the good transistor characteristics, the drive currents of the 3D metal-gate/high-κ/GOI p-MOSFETs are 2.4 times higher than the Si p-MOSFETs, shown in Fig. 2(a), at the same 1.4 nm EOT metal-gate/high-κ structure. The higher drive current is especially important for achieving the desired higher switching speed ($C_{load}V_d/I_d$) of ICs. The down-scaling MOSFETs require the lower V_d for reliability consideration and low power application. Therefore, the increasing transistor's drive current is the dominate factor to increase the operation

speed of ICs, under the same capacitive load (C_{load}) condition from IC designs.

To further analyze the higher drive currents for both n- and p-MOSFETs, we have plotted the electron and hole mobility from measured I_d-V_g characteristics. Figures 6 show the hole mobility for IrO_2-IrO_2/Hf dual gates on high-κ $LaAlO_3$ dielectric and on 3D GOI or 2D Si p-MOSFETs. The hole mobilities in Si are lower than the universal mobility values, which is typical for metal-gate/high-κ p-MOSFETs [5]-[19]. The universal mobility is the interface mobility of SiO_2/Si p-MOSFETs that is universal due to the fundamental scattering mechanisms of columbic, phonon and interface roughness scatterings. Note that the oxide charge generated columbic scattering of [IrO_2-Hf-IrO_2]/$LaAlO_3$/Si p-MOSFETs is only ~ 10^{11} cm^{-2} from the slope of flat-band voltage and thickness plot in Fig. 3. This low oxide charge is comparable to the best metal-gate/HfO_2 MOSFETs [18]. Therefore, the mobility degradation is mainly due to the intrinsic property of high-κ dielectric- the soft phonon scattering [18] from the ionic nature of metal-oxide, but such ionic property also provides the required higher κ value than SiO_2 according to Solid-State Physics. To further improve both electron and hole mobilities, the strained Si is required [18]-[19], [21], [23]. The most successful strained Si can provide ~50% higher hole mobility in oxynitride gate dielectric p-MOSFET [23] and 35% higher electron mobility in high-κ HfO_2 n-MOSFET [18]. The higher both electron and hole mobilities are especially important to achieve higher operation speed and better cost ICs [23]. The higher drive current can also be obtained by conventional method of down-scaling the p-MOSFETs. Therefore, the higher mobility or the "mobility scaling" provides alternative way to improve the transistor's drive current similar to device scaling, which is already used for advanced high-speed CPU manufacture [23].

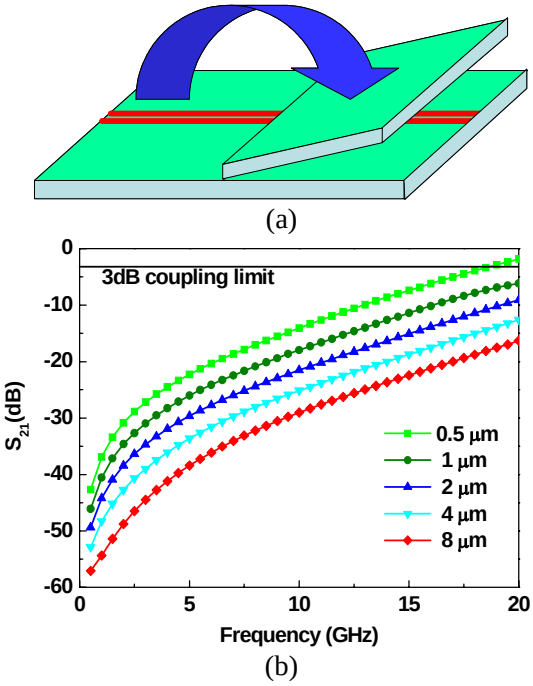


Fig. 4. (a) The schematic diagrams of a 3D IC and (b) the coupling loss by 3D Electro-Magnetic calculation of 1 mm long two parallel lines with various spacing or different lengths. The 3D integration can decrease the 1P6M interconnect distance to half and 1/4 using one and two layers GOI above bottom Si MOSFETs, respectively.

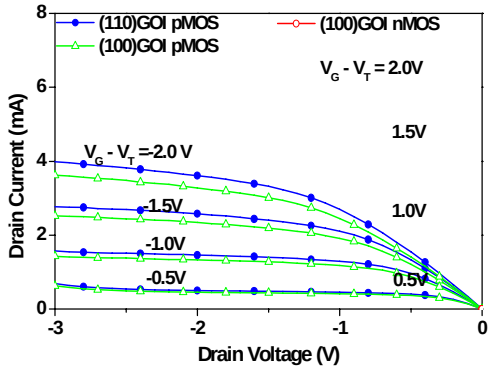


Fig. 5. The I_d -V_d characteristics of the 3D [IrO_2-IrO_2/Hf]/$LaAlO_3$/GOI p-MOSFETs with 1.4 nm EOT $LaAlO_3$ gate dielectric. The drive currents of 3D metal-gate/high-κ/GOI p-MOSFETs are higher than the 2D devices on Si shown in Fig. 2(a) using the same metal-gate/high-κ structure

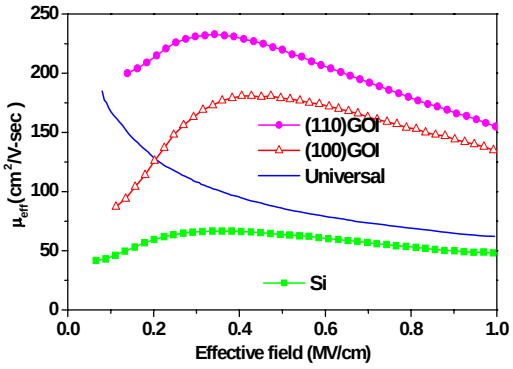


Fig. 6. The hole mobilities of $IrO_2/LaAlO_3$ p-MOSFETs on Si or GOI. The 3D GOI p-MOSFETs have 1.8X larger electron mobility and higher hole mobility of 2.7X in (100) Ge or 3.5X in (110) Ge than 2D Si counterparts.

Note that higher electron (1.8 times) and hole (2.7 times) mobilities can also obtained in 3D GOI p-MOSFETs than Si counterparts with the same metal-gate/high-κ structure, where the hole mobility can further be increased to 3.5 times higher than Si using the (110) Ge substrate similar to the hybrid-orientation technology (HOT) approach of two different substrates [24]. These are the largest reported improvement in high-κ gate dielectric p-MOSFETs among the strained Si [18]-[19], HOT [24], and strained-Si-directly-on-insulator (SSDOI) [25]. Therefore, the higher both electron and hole mobilities in GOI p-MOSFETs can also provide the "mobility scaling" to improve the switching speed and price of ICs. It is noticed that the GOI structure is mandatory rather than the bulk Ge p-MOSFETs in order to reduce the transistor's off-state leakage current due to the small energy band gap of

Ge [13]-[15]. This is similar to the lower off-state current in thin-body SOI case.

The comparison among various technologies for mobility improvement is summarized in Table 1. The HOT has higher hole mobility enhancement than strained Si and SSDOI, but without electron mobility improvement. The GOI can have both highest electron (1.8X) and hole (3.5X) mobility improvement as integrated with high-κ gate dielectric. The GOI is similar to SOI without additional epitaxy, mask step or dislocation related to lower yield as compared with other technologies. The simple and low cost GOI is also ideal to be integrated with III-V RF [27] and opto-electronic [28] devices that can be used for wireless and optical communications. Another inherent merit of GOI is the low process temperature (500-550^{o}C) that is the excellent candidate for high-κ gate dielectric integration. In sharp contrast, the much higher rapid thermal annealing (RTA) temperature (1000-1050^{o}C) for ion implantation activation in the source-drain of metal-gate/high-κ/Si p-MOSFETs will increase EOT due to residual oxygen diffusion, crystallize high-κ gate dielectric from amorphous state to increase leakage current, create Fermi-level pinning and high threshold voltage due to metal-gate and high-κ interface reaction, and cause impurity diffusion and short-channel effect in sub-100 nm channel devices. All these problems can be easily solved by low temperature processed metal-gate/high-κ/GOI p-MOSFETs.

It is important to notice that the higher 3D integration density and better transistor drive current in top layer GOI p-MOSFETs are equivalent to device down-scaling. Thus, the successful 3D integration with lowered interconnect density not only largely reduces the AC power consumption but also equivalently extends the CMOS scaling beyond quantum-mechanical limit of 2D CMOS. The low cost 3D integration, with equivalent down-scaling capability, is also the potential solution to the rapidly increasing fab cost as continuously scaling down to deep nm scale.

	Epitaxy	Mobility (IC speed & cost)	Dislocation & Defect	GaAs RF & Photonics Integration	Added Cost
SOI	none	degraded	free	unable	none
SSDOI	yes	improved	dislocation still observed	unable	Epitaxy + yield
HOT	yes	improved, only in pMOS	-	unable	Epitaxy + mask
Intel's strained Si	yes	improved, especially in pMOS (>50%)	-	unable	Epitaxy + mask
GOI	none	largely improved even with high-κ dielectric	free	ideal	none

Table 1. Comparison of GOI with SOI, SSDOI, HOT, and Intel's strained Si (local and mechanical strained Si).

The architecture of integrating 3D metal-gate/high-κ/GOI devices on Si can also be used for high performance RF SoC, where the integration of RF transceiver on CPU and chipset is the technology trend to realize the fully connected wireless network. However, the requirements of RF SoC are high performance both active MOSFETs and passive RF devices [29]-[31] that are suffered from the larger substrate loss related poor quality-factor due to the low resistivity (10 Ω-cm) VLSI-standard Si substrate than semi-insulating GaAs (~10^7 Ω-cm) [32]-[37]. The poor RF isolation of VLSI-standard Si substrate also feeds back the RF noise from power amplifier to front-end low-noise amplifier and becomes worse as increasing frequency to Ultra-Wide Band. Besides, the passive RF devices usually occupy most of the IC chip area rather than the sub-μm MOSFETs as shown in Figure 7, a typical layout of an Ultra-Wide Band low-noise amplifier. Because the 3D GOI on Si architecture can use the high resistivity Si (HRS) substrate to reduce the large substrate loss [38], high performance RF passive devices can be realized on 3D GOI/Si platform for RF SoC application with top Ge etched away.

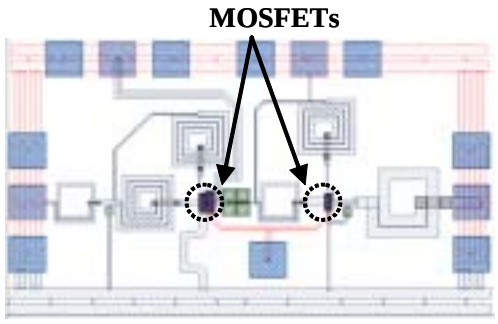


Fig. 7. The circuit layout of a low noise amplifier used for Ultra-Wide Band application. The active transistors only occupy a small portion of the whole IC.

One minor drawback is the current unavailability of 12-in HRS substrate, which can be overcome by applying ion-implant translated semi-insulating Si (10^6 Ω-cm) [32]-[37]. The mechanism is to form high density nm-scale traps by high dose ion-implant, where the free carriers in VLSI-standard Si substrate will be frozen by these traps to give the desired high resistivity. Similar charge-trapping method was also applied to form the semi-insulating GaAs and InP substrates at early days by introducing the mid-gap traps from dopants. Note that the high resistivity can be preserved to a maximum operation frequency near 1 THz

(1000 GHz) from the measured carrier lifetime of ~1 ps using optical pump-probe method [35]-[37]. This is due to the high trap density and deep trap energy in Si substrate formed by ion-implantation. Such THz limitation will ensure the continuous increasing operation frequency of Si high-speed ICs for two to three decades long beyond the Ultra-Wide Band technology.

Figures 8(a) and 8(b) show the broadband filter on 1.5 μm SiO_2 isolated Si substrate with and without the ion implant through the fabricated filter respectively, where the SiO_2 layer on VLSI-standard Si substrate is used to reduce the RF loss. The same filter is failed completely without the ion implant that is due to the 20 dB large loss as fabricated on VLSI-standard Si substrate.

For the filter with H^+ ion implant at ~4 MeV energy and 10^{16} cm^{-2} dose, high RF performance of very low 1.6 dB insertion loss at 91 GHz is measured with broad 10 GHz bandwidth, which is close to ideal filter designed by Electro-Magnetic simulation [33].

Figures 9(a) and 9(b) show the return loss and radiation pattern of an on-chip antenna on 1.5 μm SiO_2 isolated Si substrate respectively, which is important for inter-chip wireless communication [1]. Without ion implantation, the antenna fabricated on VLSI-standard Si shows only poor antenna resonance and tiny radiation power. In sharp contrast, the same on-chip antenna implanted by ~4 MeV and 10^{16} cm^{-2} H^+ ion has sharp resonance at 48 GHz and 2nd harmonic resonance at 0.1 THz. Good radiation pattern and higher antenna gain are also measured. Table 2 summarizes the comparison between the ion-implant translated semi-insulating Si, HRS [38] and RF MEMS [39]-[40] technologies for RF Si IC and SoC applications.

All three methods require additional mask, which is used for HRS to define the well depth [38].

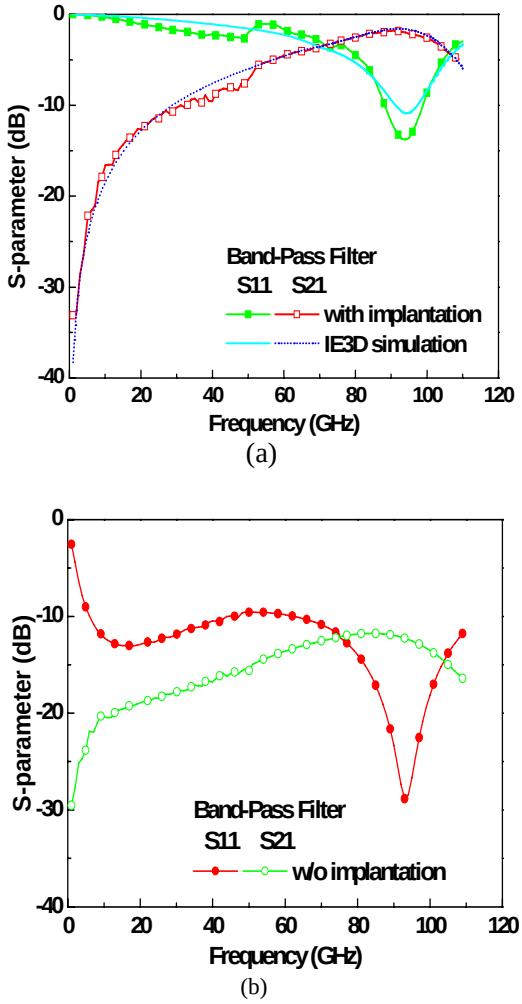


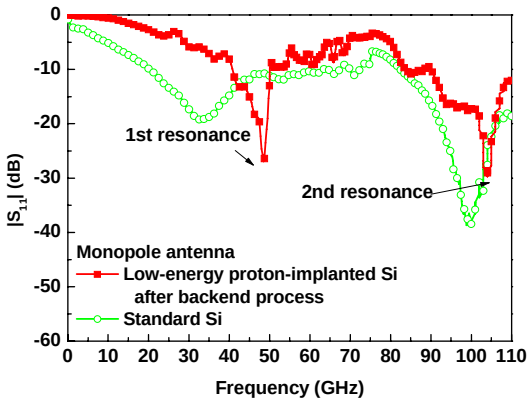
Fig. 8. The measured and Electro-Magnetic simulated S-parameters of CPW broadband filters on without the ion implantation. A 1.5 μm SiO_2 on Si substrate is used to reduce the RF loss 1.5-μm-SiO_2/VLSI-standard-Si-substrate (a) with and (b) .

The selective ion implantation formed semi-insulating Si provides the high resistivity and deep RF isolation thickness without the added package cost. These high RF performance passive devices on Si [32]-[37] suggest sub-THz devices can be realized on this new VLSI architecture using GOI/Si platform, where high performance transistors can be formed by metal-gate/high-κ/GOI

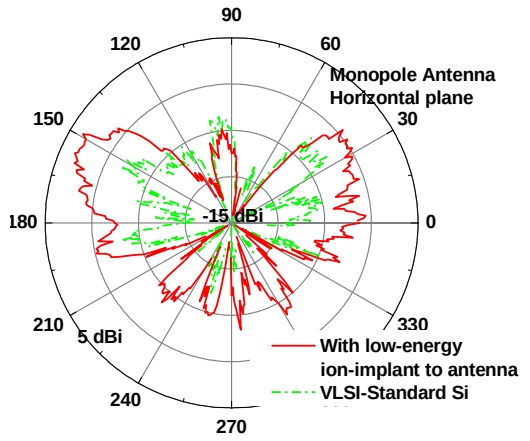
p-MOSFETs. We have shown the 3D integration of metal-gate/high-k/GOI CMOSFETs on

	ρ (Ω-cm)	Isolation depth	Added Mask	Added Process	Added Cost
Ion implant	10^6	200μm to full wafer	1	implant	Ion implant multi-layers
HRS	10^3	Full wafer	1	Implant + RTA	HRS substrate
MEMS	-	Limited to etching	1	Deep etching	Package

Table 2. The comparison of ion-implant translated semi-insulating Si with HRS, and RF MEMS technologies



(a)



(b)

Fig. 9. The measured (a) return loss and (b) horizontal polarized radiation pattern of on-chip antenna on 1.5-μm-SiO_2/VLSI-standard-Si-substrate. The antenna on VLSI-standard Si is failed due to large loss. The same antenna has sharp resonance at 48 GHz and 2nd harmonic at 103 GHz after ion implant.

四、結論

interconnect and 2D Si CMOSFETs can provide solutions for DC and AC power consumptions. The higher 3D integration density and the higher drive currents (2.2 and 2.4 times for n- and p-MOSFETs) using 3D GOI CMOSFETs are equivalent to down-scaling the 2D CMOSFETs, which gives equivalent scaling capability beyond 2D quantum-mechanical limit. The low cost 3D integration is also the potential solution to the rapidly increasing fab cost as continuously down-scaling into sub-100 nm scale. The low process temperature in 3D GOI and excellent lattice constant match to GaAs can be further integrated with III-V microwave and opto-electronic devices. This 3D architecture of GOI CMOSFETs on interconnects and Si CMOSFETs can also provide high performance RF passive devices close to these on III-V's for SoC and wireless communication applications.

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