行政院國家科學委員會專題研究計畫　成果報告

4-20GHz 超寬頻低雜訊放大器設計

計畫類別：個別型計畫
計畫編號：NSC94-2215-E-009-058-
執行期間：94 年 08 月 01 日至 95 年 07 月 31 日
執行單位：國立交通大學電子工程學系及電子研究所

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報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 95 年 9 月 18 日

Wide-Band Matched LNA Design Using Transistor's Intrinsic Gate–Drain Capacitor

Robert Hu

***Abstract*—This paper presents the development of a wide-band amplifier with matched input impedance and low noise temperature over 10–20 GHz. Here, the novel wide-band feedback mechanism provided by the transistor's intrinsic gate–drain capacitor will be analyzed in detail with both the derived input reflection coefficient and noise temperature of the resulting circuit confirmed by their simulated counterparts. It is thus clear why by fine tuning its output RC loading impedance and source inductance, a transistor's input reflection coefficient and noise temperature can be greatly improved over broad bandwidth. To demonstrate the feasibility of this novel approach, a wide-band low-noise amplifier (LNA) is designed and characterized. A bandwidth broadening mechanism using double feedback is also proposed for the future design of matched ultra-wide-band LNA.**

***Index Terms*—Input matching, low-noise amplifier (LNA), noise parameters, noise temperature, wide-band.**

I. Introduction

WIDE-BAND low-noise amplifiers (LNAs) have been a critical component in communication industry [1]–[3] and different scientific fields such as the very noise-sensitive radio-astronomy instrumentation where the typical LNA circuit has single-ended transistors in cascade [4]–[6]; LNAs with complicated input tuning circuits, which result in the inevitable incoming signal loss are, therefore, not suitable for astronomical receivers. With this type of cascade, LNAs keep reaching even higher frequency and wider bandwidth, but what is less explored is an accurate and satisfactory account, beyond the scope of simulation or speculation, of how the matched input impedance can be achieved over wide bandwidth [7]–[13].

On the Smith chart in the intended frequency range, a typical input reflection coefficient ($S_{\rm in}$) contour of the wide-band LNA is a loop surrounding the zero point where a small enclosed area is preferred; while that of the narrow-band LNA is a trajectory passing through the zero point at one specific frequency point (Fig. 1). As has been well studied, in the narrow-band design where the impact of the intrinsic feedback, i.e., the Miller effect, can be suppressed using cascode circuit configuration, it is the combination of external source and gate inductors with the transistor itself that brings in the desired matched input impedance [14]–[16]. By replacing these inductors with some more complicated LC matching circuits, such as a high-order bandpass ladder filter, wider bandwidth can indeed be achieved [17]–[19]. However, the more complicated this passive impedance matching circuit is, the higher the resulting amplifier's noise temperature will be, as the accumulated input signal loss can no longer be neglected, especially if the substrate is a lossy one like silicon.

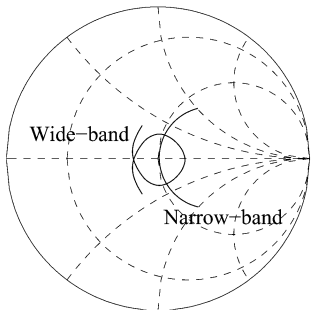

Fig. 1. Typical input reflection-coefficient contours on the Smith chart of both the wide- and narrow-band LNAs.

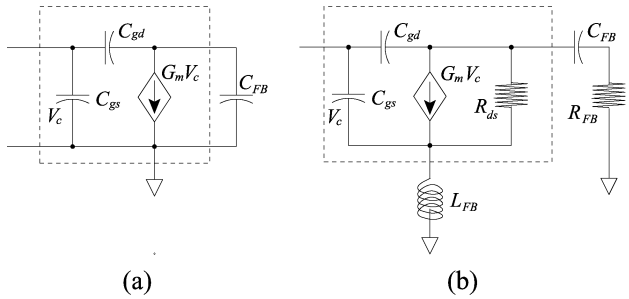

Fig. 2. Transistor circuits with matched input impedance over wide bandwidth where the dotted box contains the transistor model. (a) An output loading $C_{\rm FB}$ is sufficient for rendering wide-band matched $S_{\rm in}$ when a simplified transistor model is employed. (b) Additional $R_{\rm FB}$ and $L_{\rm FB}$ need to be added when a more sophisticated transistor model is used.

Contrary to the straightforwardness of the conventional narrow-band and its extended wide-band circuit configurations, some mathematical manoeuvring are needed in analyzing this novel wide-band input matching mechanism. A useful first step is with a simplified transistor model where only the transconductance G_m, the gate–source capacitor $C_{\rm gs}$, and the gate–drain capacitor $C_{\rm gd}$ are involved, as shown in Fig. 2(a). The output loading circuit is assumed to be a capacitor $C_{\rm FB}$, which is legitimate since the transistor, especially the first-stage one, in the LNA does not need to have its output loading impedance equal to 50 Ω. Since G_m is much larger than $\omega C_{\rm gd}$,

Manuscript received November 11, 2005. This work was supported in part by the National Aeronautics and Space Administration under Grant NAG5-9493 and by the National Science Council, R.O.C., under Contract NSC 94-2215-E-009-058.

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Digital Object Identifier 10.1109/TMTT.2006.869703

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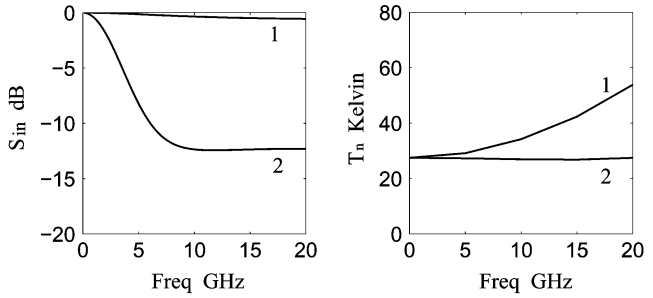

Fig. 3. Simulated input reflection coefficients and noise temperatures of the transistor and its wide-band circuit. (a) Curve 1 corresponds to $S_{\rm in}$ of the single transistor with 50-Ω output loading impedance; curve 2 is the $S_{\rm in}$ of the intended wide-band transistor circuit with external $R_{\rm FB}, C_{\rm FB}$, and $L_{\rm FB}$. (b) T_n of the single transistor and its wide-band counterpart, both with 50-Ω generator impedance.

this circuit's input admittance $Y_{\rm in}(=1/Z_{\rm in})$ can be calculated as

$$Y_{\rm in} = j\omega C_{\rm gs} + j\omega C_{\rm gd}\left[1 - \frac{j\omega C_{\rm gd} - G_m}{j\omega(C_{\rm gd}+C_{\rm FB})}\right] \approx j\omega(C_{\rm gs}+C_{\rm gd}) + \frac{C_{\rm gd}G_m}{C_{\rm gd}+C_{\rm FB}} \quad (1)$$

which is a capacitor in parallel with a resistor. An external source inductor can then be added to remove the imaginary part of $Y_{\rm in}$, thus rendering a frequency-independent matched input impedance [20].

However, the above reasoning cannot reflect the real LNA design work since it neglects the role played by the intrinsic drain resistor $R_{\rm ds}$, which has a finite value in the case of high electron-mobility transistor (HEMT) [21]–[23]. In fact, the transistor used in designing this paper's 10–20-GHz LNA has 68-Ω drain resistance. With finite-value $R_{\rm ds}$, simulation reveals that it is not simply a pure output capacitor, but an $R_{\rm FB}C_{\rm FB}$ output loading circuit plus a source inductor $L_{\rm FB}$, like that in Fig. 2(b), that brings in a matched input impedance for the transistor circuit over wide bandwidth. Here, subscript FB denotes feedback to stress these three components' respective impact on the input reflection coefficient.

In Fig. 3, the simulated $S_{\rm in}$ and matched T_n of both the transistor and its corresponding wide-band circuit are displayed. Curve 1 is from the transistor itself that has $C_{\rm gs} = 120$ fF, $C_{\rm gd} = 36$ fF, $G_m = 156$ mS, and $R_{\rm ds} = 68\ \Omega$, and the drain temperature $T_{\rm drain}$ is set to 2300 K. Curve 2 is for the wide-band circuit that has an external source inductor $L_{\rm FB} = 200$ pH connected to the transistor, and the transistor now has an RC output loading circuit with $R = 40\ \Omega$ and $C = 475$ fF. Simulation also reveals that $L_{\rm FB}$, once added, suppresses the combined effect of $C_{\rm gs}$ and $C_{\rm gd}$, and thus results in an almost constant noise temperature over wide bandwidth. Also, it is mainly $L_{\rm FB}$ and $C_{\rm FB}$ that bring upon the intended small input reflection coefficient at low frequency; as frequency increases, it is predominantly $L_{\rm FB}$ and $R_{\rm FB}$ that help in the lowering of $S_{\rm in}$. Since no external resistor appears at its input, this matched wide-band circuit tends to be low noise. Useful though the simulation is, no insight as to why it works that way can be extracted from this empirical approach.

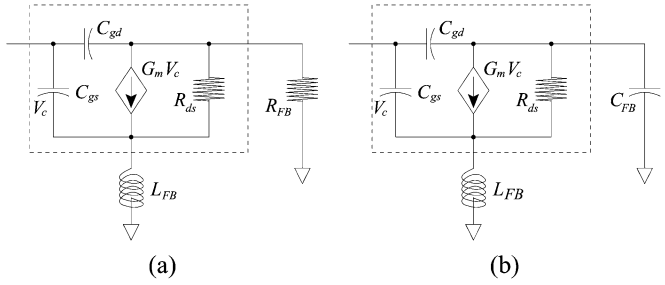

Fig. 4. Proposed wide-band circuit can be decomposed into a resistive-loading circuit at high frequency and a capacitive-loading circuit at low frequency. (a) The resistive-loading circuit with $R_{\rm FB}$ as its output loading. (b) The capacitive-loading circuit with $C_{\rm FB}$ as its output loading. The external source inductor $L_{\rm FB}$ is retained in both circuits.

Relevant equations will be developed below to explain the simulated results and how the wide-band mechanism works, followed by the implementation of a wide-band LNA. A bandwidth broadening mechanism suitable for ultra-wide-band LNA design is then proposed. Since any gain variation of the input transistor can always be compensated in the following stages of the LNA, and the impact of the transistor's gain degradation on the overall noise temperature is only secondary when compared with the transistor's directly contributed noise, gain performance will not be addressed in this paper.

II. Input Matching Analysis

To facilitate the input-matching analysis, the wide-band circuit configuration needs to be decomposed into two sub-circuits like that of Fig. 4: one is with resistive output loading $R_{\rm FB}$, which accounts for the high-frequency response of the original circuit; the other one is with capacitive output loading $C_{\rm FB}$, which is used to explain the original circuit's low-frequency behavior. The external source inductor $L_{\rm FB}$ exists in both cases.

If both $C_{\rm gd}$ and $R_{\rm ds}$ can be neglected, input impedance of the resistive-loading circuit will be

$$Z_{\rm in} = \frac{1}{j\omega C_{\rm gs}} + \frac{L_{\rm FB}(G_m + j\omega C_{\rm gs})}{C_{\rm gs}} \approx \frac{1}{j\omega C_{\rm gs}} + \frac{L_{\rm FB}G_m}{C_{\rm gs}} \quad (2)$$

where it is assumed that the impedance of $C_{\rm gs}$ is much larger than that of L_{LF}, which is usually the case in designing an amplifier circuit. This $Z_{\rm in}$ expression can be best understood as that: the induced current $G_m V_c$ flowing through inductor $L_{\rm FB}$ will generate a voltage that is in phase with the input current and, therefore, contributes a value of $L_{\rm FB}G_m/C_{\rm gs}$ to the input resistance. Conceptually this interpretation is correct, but numerically it is inaccurate because of the omission of $C_{\rm gd}$ and $R_{\rm ds}$. The impact of $C_{\rm gd}$ is that it will increase the effective input capacitance and, thus, reduces the amount of ${\rm Re}[Z_{\rm in}]$ generated by $L_{\rm FB}$; while the finite-value $R_{\rm ds}$ will degrade the transconductance G_m and, hence, lowers the induced current flowing through $L_{\rm FB}$. A better approximation for the input impedance is

$$Z_{\rm in} \approx \left(\frac{1}{j\omega C_{\rm gs}} + \frac{L_{\rm FB}\gamma G_m}{C_{\rm gs}}\right)\left[1 + \frac{C_{\rm gd}}{C_{\rm gs}}(1+\gamma G_m R_{\rm FB})\right]^{-1} \quad (3)$$

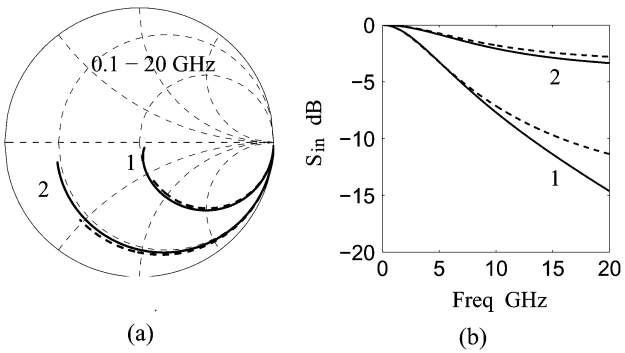

Fig. 5. Input reflection coefficient of the resistive-loading transistor circuit. (a) On the Smith chart, curves 1 and 2 correspond to the circuit with $L_{\rm FB} = 200$ and 38 pH, respectively. The solid curves are the simulated results; the dashed curves are the calculated ones using (3). (b) The same $S_{\rm in}$ expressed in decibels versus gigahertz.

with the degradation factor γ defined as

$$\gamma = \frac{R_{\rm ds}}{R_{\rm ds} + R_{\rm FB} + j\omega L_{\rm FB}}. \tag{4}$$

In deriving (3), it is assumed

$$\omega L_{\rm FB} \ll \frac{1}{\omega C_{\rm gs}} \quad \omega L_{\rm FB} \ll R_{\rm FB} \tag{5}$$

and the leakage current flowing through $C_{\rm gd}$ is much smaller than the induced drain current. Of course, the matching frequency for $Z_{\rm in} = 50\,\Omega$, i.e., Z_0, is very high if not infinite. For the transistor under discussion, the required $L_{\rm FB}$ for matching only the real part of the input impedance will be a mere 38 pH using (2), and 200 pH if (3) is adopted. As expected, simulated results justify the choice of the latter one. Fig. 5 shows the input reflection coefficient from 0.1 to 20 GHz of the resistive-loading transistor circuit: the solid curves are the simulated results where curve 1 has $R_{\rm FB} = 60\,\Omega$ and $L_{\rm FB} = 200$ pH and curve 2 has $R_{\rm FB} = 60\,\Omega$ and $L_{\rm FB} = 38$ pH; the dashed curves are the calculated counterparts using (3). The high-frequency discrepancy between the solid and dashed curves is due to the assumption, i.e., (5), used in deriving the close-form expression for input impedance. If an external inductor is inserted to the input of the transistor circuit, a matched input impedance can be obtained at some finite-value frequency point; in this paper's proposed wide-band circuit, however, this input inductor has been taken away.

To facilitate the analysis of the capacitive-loading circuit, the induced current source needs to be converted into the induced voltage source $G_m R_{\rm ds} V_c$, as in Fig. 6(a). Here, Y_α is the admittance looking into the $C_{\rm gd}$ branch and Z_β is the impedance looking into the $C_{\rm gs}$ branch. If the induced current $G_m V_c$ is much larger than the current flowing through either $C_{\rm gd}$ or $C_{\rm gs}$, the loop current $I_{\rm loop}$ can be approximated as

$$I_{\rm loop} = G_m R_{\rm ds} V_c \left[R_{\rm ds} + \frac{1}{j\omega C_{\rm FB}} + j\omega L_{\rm FB} \right]^{-1}. \tag{6}$$

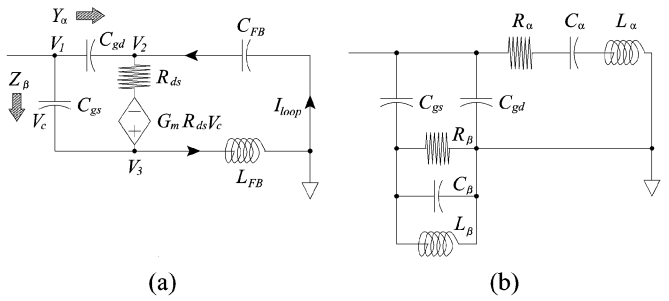

Fig. 6. Variations of the capacitive-loading circuit used to facilitate the derivation of $Z_{\rm in}$. (a) To find out the circuit's input impedance, values of Y_α and Z_β, which are indicated by the arrows, need to be derived first. (b) The equivalent circuit from the input impedance's point-of-view where $R_\alpha, C_\alpha, L_\alpha$ come from Y_α, while $R_\beta, C_\beta, L_\beta$ are from Z_β.

Thus, the admittance looking into the $C_{\rm gd}$ branch is

$$\begin{aligned} Y_\alpha &= j\omega C_{\rm gd} \frac{V_1 - V_2}{V_1} \\ &= j\omega C_{\rm gd} + \left(R_\alpha + \frac{1}{j\omega C_\alpha} + j\omega L_\alpha \right)^{-1} \end{aligned} \tag{7}$$

with

$$\begin{aligned} R_\alpha &= \frac{C_{\rm FB}}{G_m C_{\rm gd}} \\ C_\alpha &= G_m R_{\rm ds} C_{\rm gd} \\ L_\alpha &= \frac{L_{\rm FB} C_{\rm FB}}{G_m R_{\rm ds} C_{\rm gd}} (1 + G_m R_{\rm ds}). \end{aligned} \tag{8}$$

Likewise, the impedance into the $C_{\rm gs}$ branch is

$$\begin{aligned} Z_\beta &= \frac{1}{j\omega C_{\rm gs}} \frac{V_1}{V_1 - V_3} \\ &= \frac{1}{j\omega C_{\rm gs}} + \left(\frac{1}{R_\beta} + j\omega C_\beta + \frac{1}{j\omega L_\beta} \right)^{-1} \end{aligned} \tag{9}$$

with

$$\begin{aligned} R_\beta &= \frac{G_m L_{\rm FB}}{C_{\rm gs}} \\ C_\beta &= \frac{C_{\rm gs}}{G_m R_{\rm ds}} \\ L_\beta &= \frac{L_{\rm FB} G_m R_{\rm ds} C_{\rm FB}}{C_{\rm gs}}. \end{aligned} \tag{10}$$

With knowledge of Y_α and Z_β, input impedance of the capacitive-loading circuit can be easily found out as follows:

$$Z_{\rm in} = \left(Y_\alpha + \frac{1}{Z_\beta} \right)^{-1}. \tag{11}$$

From the input point-of-view, the capacitive-loading circuit can be rearranged such as that of Fig. 6(b). The critical components are those on the $R_\alpha C_\alpha L_\alpha$ branch, while the other two shunt branches offer some modifications, as can be verified through simulation. In Fig. 7, the solid curve is the simulated result with

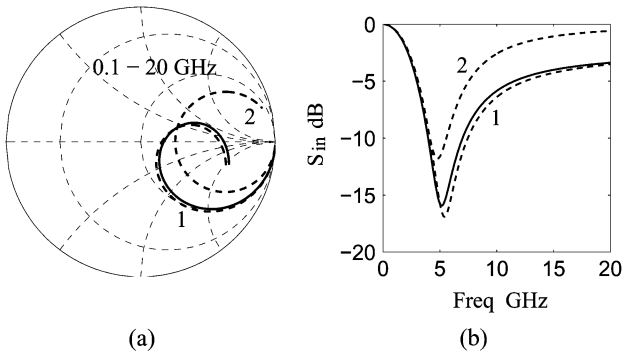

Fig. 7. Calculated and simulated input reflection coefficient for the capacitive-loading circuit. (a) On the Smith chart, dashed curve 1 is the calculated result using (11), solid curve 1 is its simulated counterpart, and dashed curve 2 is the calculated one using $R_\alpha, L_\alpha, C_\alpha$ of (8) only. (b) The same results expressed in decibels versus gigahertz.

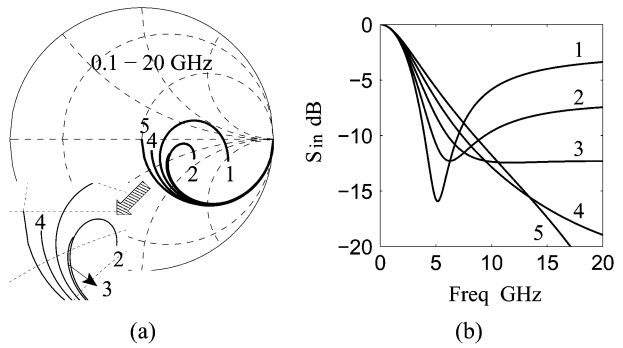

Fig. 8. Simulated input reflection coefficient of the transistor circuit with different values of $R_{\rm FB}$. (a) On the Smith chart, curves 1–5 correspond to $R_{\rm FB} = 0, 20, 40, 60$, and $80\ \Omega$, respectively, while $C_{\rm FB}$ and $L_{\rm FB}$ are held constant at 475 fF and 200 pH. (b) The same simulated results in decibels versus gigahertz.

$C_{\rm FB} = 475$ fF and $L_{\rm FB} = 200$ pH, dashed curve 1 is the calculated counterpart using (11), dashed curve 2 is the calculated result using only R_α, C_α, and L_α while all the other circuit components are neglected. The matching frequency can thus be approximated as [24]

$$f_0 = \frac{1}{2\pi\sqrt{L_\alpha C_\alpha}} = \frac{1}{2\pi\sqrt{L_{\rm FB}C_{\rm FB}(1+G_m R_{\rm ds})}}. \qquad (12)$$

With the discussed component values, the calculated frequency using (12) is 4.79 GHz and is very close to the simulated one. The 3-dB bandwidth can also be calculated accordingly.

Since the resistive-loading circuit is matched at high frequency while the capacitive-loading circuit is matched at comparatively low frequency, the composite $R_{\rm FB}C_{\rm FB}$-loaded circuit is deemed to be matched over a wide bandwidth: it degenerates into the $C_{\rm FB}$-loaded circuit at low frequency, thus matched, and becomes the $R_{\rm FB}$-loaded circuit at high frequency and matched again. Now the wide-band input matching mechanism can be soundly explained. With a series $R_{\rm FB}C_{\rm FB}$ used as the transistor's output loading circuit while an inductor $L_{\rm FB}$ is connecting its source to ground, Fig. 8 shows the simulated input reflection coefficient of this transistor circuit. Here, curves 1–5 have $R_{\rm FB} = 0, 20, 40, 60$ and $80\ \Omega$, respectively,

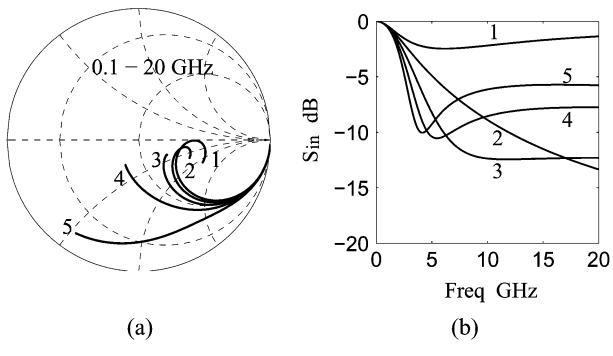

Fig. 9. Simulated input reflection coefficient of the wide-band transistor circuit with different values of $L_{\rm FB}$. (a) On the Smith chart, curves 1–5 correspond to $L_{\rm FB} = 0, 100, 200, 300$, and 400 fF, respectively, while $C_{\rm FB}$ and $R_{\rm FB}$ are held constant at 475 fF and 40 Ω. (b) The same simulated results in decibels versus gigahertz.

and all five curves are with $C_{\rm FB} = 475$ fF and $L_{\rm FB} = 200$ pH. Clearly, curve 3 presents the most desired wide-band characteristic. As for curve 2, its hook-shaped $S_{\rm in}$ on the Smith chart resembles the circled input reflection coefficient contour of a typical wide-band LNA.

Fig. 9 concerns the impact on $S_{\rm in}$ of the source inductor $L_{\rm FB}$: curves 1–5 are with $L_{\rm FB} = 0, 100, 200, 300, 400$ pH, respectively, and all have $C_{\rm FB} = 475$ fF and $R_{\rm FB} = 40\ \Omega$. Though it is curve 3 that is most coveted, other values of $L_{\rm FB}$ retain, to a certain degree, the wide-band characteristic, as $S_{\rm in}$ tends to be running flat at high frequency. This suggests that what is most critical to a wide-band transistor circuit is the value of its output loading impedance.

III. Noise Temperature Analysis

For a transistor with $C_{\rm gs}, C_{\rm gd}, G_m$, and $R_{\rm ds}$ at temperature $T_{\rm drain}$, its noise temperature can be expressed in terms of the generator impedance $Z_g = R_g + jX_g$ or the generator admittance $Y_g = G_g + jB_g$ as

$$\begin{aligned} T_n &= \frac{T_{\rm drain}}{G_m^2 R_{\rm ds} R_g}|1 + j\omega(C_{\rm gs}+C_{\rm gd})Z_g|^2 \\ &= \frac{T_{\rm drain}}{G_m^2\, R_{\rm ds} G_g}|Y_g + j\omega(C_{\rm gs}+C_{\rm gd})|^2. \end{aligned} \qquad (13)$$

Thus, the increase with frequency of the noise temperature comes mainly from $C_{\rm gs}$ and, to a lesser extent, from $C_{\rm gd}$. By using an input inductor to mitigate the capacitive effect, noise temperature of a narrow-band transistor circuit can be greatly reduced at one frequency point.

To derive the noise-temperature expression for the wide-band circuit, its output loading $R_{\rm FB}C_{\rm FB}$ needs to be replaced by a short circuit. Since the input noise temperature of a two-port circuit is a function of its generator impedance, but not its output loading impedance, this short-circuit arrangement is legitimate with the additional advantage of simplifying the derivation procedure. To avoid the mathematical entanglement while retain the underlying physics, capacitor $C_{\rm gd}$ will be omitted here.

First, the relationship between the output current $I_{\rm short}$ and noise current I_R, which is generated by $R_{\rm ds}$ at temperature $T_{\rm drain}$, has to be constructed, as indicated in Fig. 10(a). Since

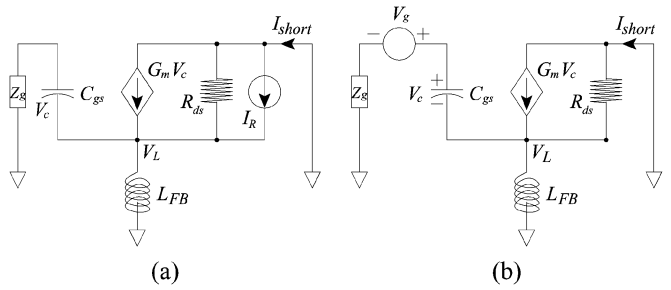

Fig. 10. Schematics used for noise-temperature derivation. (a) Schematic used to derive the output short-circuit $I_{\rm short}$ from the $R_{\rm ds}$-accompanying noise current I_R. (b) Schematic used to obtain the equivalent generator noise voltage V_g from $I_{\rm short}$.

the voltage V_c on $C_{\rm gs}$, which is the gate voltage minus the source voltage, is

$$V_c = \frac{-Z_C V_L}{Z_g + Z_C} = \frac{-Z_{LR} Z_C I_R}{Z_g + Z_C + Z_{LR} + G_m Z_{LR} Z_C} \tag{14}$$

with

$$Z_{LR} = \left(\frac{1}{j\omega L_{\rm FB}} + \frac{1}{R_{\rm ds}}\right)^{-1}$$
$$Z_C = \frac{1}{j\omega C_{\rm gs}}. \tag{15}$$

Thus,

$$I_{\rm short} = I_R + G_m V_c - \frac{V_L}{R_{\rm ds}}$$
$$= I_R \frac{Z_g + Z_C + Z_{LR} - (Z_C + Z_g) Z_{LR}/R_{\rm ds}}{Z_g + Z_C + Z_{LR} + G_m Z_{LR} Z_C}. \tag{16}$$

Now this $I_{\rm short}$ has to be transformed to its equivalent input noise voltage V_g, which is generated by Z_g at temperature T_n, as shown in Fig. 10(b). Since

$$V_c = \frac{Z_c V_L}{(1 + G_m Z_C) Z_{LR}} = \frac{Z_c V_g}{Z_g + Z_C + Z_{LR} + G_m Z_{LR} Z_C} \tag{17}$$

then

$$I_{\rm short} = G_m V_c - \frac{V_L}{R_{\rm ds}}$$
$$= V_g \frac{G_m Z_C - (1 + G_m Z_C) Z_{LR}/R_{\rm ds}}{Z_g + Z_C + Z_{LR} + G_m Z_C Z_{LR}}. \tag{18}$$

Following the thermodynamic definition, the noise voltage V_g and noise current I_R per unit bandwidth will be [25]

$$\overline{|V_g|^2} = 4KR_gT_n \quad \overline{|I_R|^2} = 4KT_{\rm drain}R_{\rm ds} \tag{19}$$

where K is the Boltzmann's constant. Thus,

$$T_n = \frac{T_{\rm drain}}{G_m^2 R_{\rm ds} R_g} \left|\frac{A}{B}\right|^2 \tag{20}$$

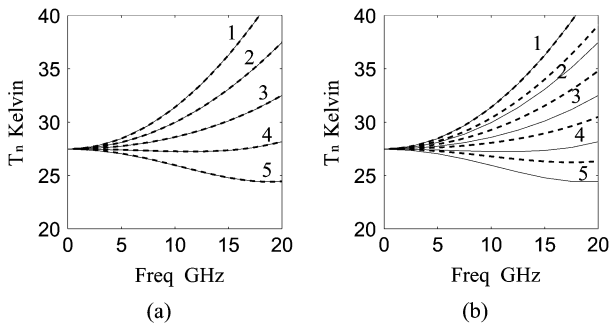

Fig. 11. Simulated and calculated noise temperatures of the wide-band transistor circuit with 50-Ω generator impedance. (a) The solid curves are the simulated T_n with curves 1–5 corresponding to circuit with external source inductor $L_{\rm FB} = 0, 50, 100, 150$, and 200 fF, respectively; the overlapping dashed curves are the calculated counterparts using (20). (b) The solid curves are the same simulated T_n; the dashed curves are the calculated results using (22), which is itself a rough approximation.

with

$$A = 1 + \frac{Z_g}{Z_C} - \frac{Z_{LR}}{R_{\rm ds}} + \frac{Z_{LR}}{Z_C} - \frac{Z_g Z_{LR}}{Z_C R_{\rm ds}}$$
$$B = 1 - \frac{Z_{LR}}{Z_C R_{\rm ds}} \left(\frac{1}{G_m} + Z_C\right). \tag{21}$$

When the generator impedance is 50 Ω, i.e., Z_0, a rough yet informative approximation is retaining the first three items of A while setting B to one; therefore,

$$T_n \approx \frac{T_{\rm drain}}{G_m^2 R_{\rm ds} Z_0} \left|1 + j\omega C_{\rm gs} Z_0 - \frac{Z_{LR}}{R_{\rm ds}}\right|^2. \tag{22}$$

It is now clear that the inclusion of the source inductor $L_{\rm FB}$, even of small value, brings in the inductive Z_{LR}, thus leveling the noise-temperature curve. Fig. 11(a) shows the simulated and calculated noise temperatures with 50-Ω generator impedance: solid curves 1–5 correspond to the simulated results with $L_{\rm FB} = 0, 50, 100, 150$, and 200 pH, respectively; the dashed curves are their calculated counterparts using (20). Validity of the rough approximation is confirmed in Fig. 11(b) where the solid curves are again the simulated results; the dashed curves are the calculated ones using (22). The reason why a large $L_{\rm FB}$ at high frequency tends to pull T_n down to 0 K is because, in this extreme case, the lower end of the drain resistor becomes floating; thus, noise current I_R can no longer reach the output loading circuit and be counted as effective noise.

IV. Wide-Band LNA Design and Characterization

As a demonstration of the newly proposed input-matching method, a wide-band LNA using Raytheon's metamorphic HEMT fabrication process is designed and measured. The constituting transistor is displayed in Fig. 12(a) and has its gate split into four fingers, each 0.1-μm wide and 50-μm long. Its S-parameters, as measured on-wafer at room temperature, are shown in Fig. 12(b) where the solid curves have bias condition of $V_d = 1.0$ V and $I_d = 12$ mA and the dashed curves have $V_d = 0.6$ V and $I_d = 12$ mA. The gate currents in both cases

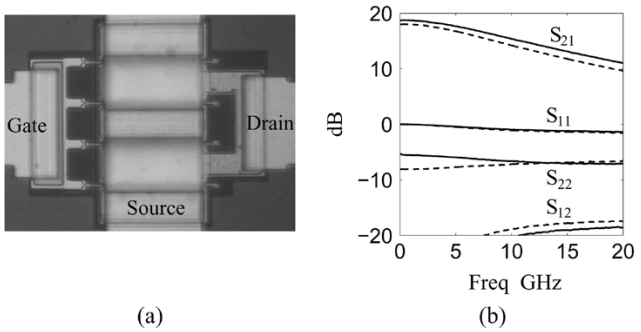

Fig. 12. Raytheon transistor and its S-parameters measured on-wafer. (a) In this photograph, the wide air-bridges are connecting the source to the ground on top and bottom. (b) In the measured S-parameters, the solid curves correspond to $V_d = 1.0$ V and $I_d = 12$ mA; the dashed curves are with $V_d = 0.6$ V and $I_d = 12$ mA.

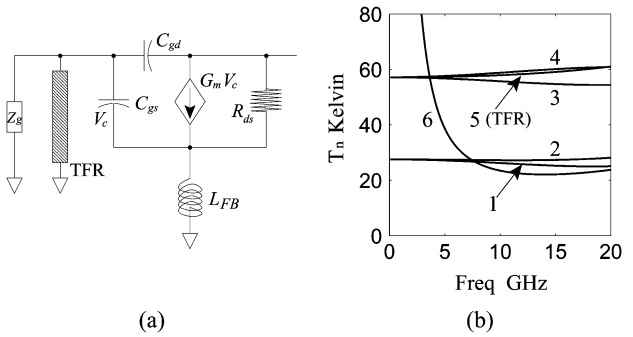

Fig. 13. Impact of the gate bias resistor on the circuit's noise temperature. (a) A thin-film resistor (TFR) can be used for the transistor's gate bias. (b) Noise temperature of the transistor circuit with different gate bias schemes employed.

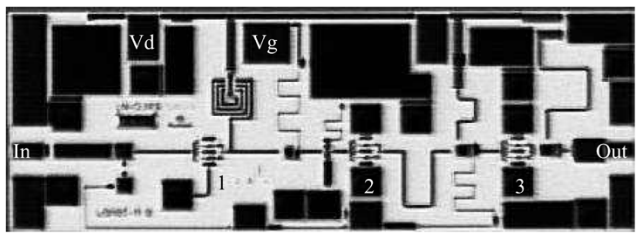

Fig. 14. Layout of the 10–20-GHz matched LNA. This three-stage circuit, with transistors numbered 1–3, has dimension of $2000 \times 750 \times 100\ \mu\text{m}^3$ and is fabricated by Raytheon.

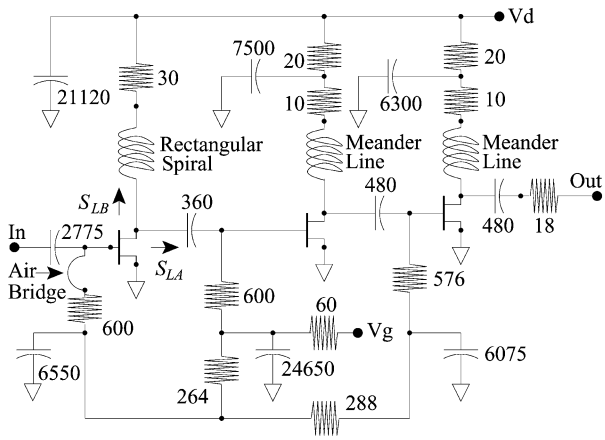

Fig. 15. Schematic of the 10–20-GHz matched LNA. The resistance is in ohms and the capacitance is in femtofarads. Here, S_{LA} and S_{LB} are the input reflection coefficients into circuits indicated by their respective arrows. The air bridge indicated can be removed using a needle probe, thus allows the gate of the first-stage transistor to be separately biased.

are less than 1 μA. Once extracted [26], parameters corresponding to the solid curves are used in this paper's discussion of wide-band input matching.

One concern in designing the wide-band LNA is about the implementation of the gate bias circuit, especially that of the first-stage transistor since it will directly affect the circuit's noise performance. For a narrow-band LNA operating at the millimeter-wave frequency range, a grounded quarter-wave transmission line can be used since it behaves like an open circuit for the incoming signal [27]. However, the required quarter-wave line is too large to be implemented into the intended 10–20-GHz circuit chip; one viable option is using a large resistor, which is intrinsically wide-band and can be low loss. For a gate bias resistor R_{bias}, the increased noise temperature due to its thermal noise is $\Delta T_n = T_{\text{amb}}/(G_g R_{\text{bias}})$, where T_{amb} is the ambient temperature. With 50-Ω generator impedance, a 600-Ω gate bias resistor contributes at least 24 K, to say nothing of the incoming signal loss.

Since in the real circuit a lumped resistor has to be realized as a thin-film resistor, as in Fig. 13(a), its parasitic shunt capacitance will inevitably deteriorate the LNA's noise performance. Fig. 13(b) compares the noise impact of different gate bias schemes: curve 1 is without any gate bias and C_{gd} is omitted; curve 2 now has C_{gd} included, but still has no gate bias circuit; curve 3 has C_{gd}, and an ideal lumped 600-Ω resistor is used for gate bias; curve 4 adds an additional 40-fF parasitic capacitor in parallel with this 600-Ω lumped resistor; curve 5 replaces the lumped resistor and its parasitic capacitor with a 600-Ω thin-film resistor that is 5-μm wide and 500-μm long with 6-Ω/square sheet resistivity; curve 6 takes a different approach by using an ideal 2000-μm bond wire for gate bias. With the goal of minimizing the bias circuit's noise impact, the off-chip scheme offers the best result. If out-of-band low-frequency S_{in} is also desired to be small, this long bond wire's other end can be connected to a 50-Ω resistor without increasing much in-band noise.

The 10–20-GHz LNA is a three-stage amplifier with common drain and gate biases, and is fabricated by Raytheon. It has dimensions of $2000 \times 750 \times 100\ \mu\text{m}^3$, as in Fig. 14, where color shading have been inverted to highlight the constituting components. Fig. 15 shows the schematic of this LNA where the capacitance is in femtofarads and the resistance is in ohms. The indicated air bridge on the gate of the first stage can be removed using a needle probe, thus allows the first-stage transistor to be biased off-chip. S_{LA} and S_{LB} are the input reflection coefficients looking into the indicated direction. Compared with the 100-Ω/square thin-film resistivity provided by TRW (now NGST), the 6-Ω/square resistivity in this Raytheon fabrication process, though suitable for applications preferring a small temperature coefficient, tends to arouse more noise.

The drain bias circuit of the first-stage transistor is composed of a rectangular spiral inductor and a 30-Ω resistor; drain bias circuits of the second and third stages have their respective inductors realized using narrow transmission lines. This approach not

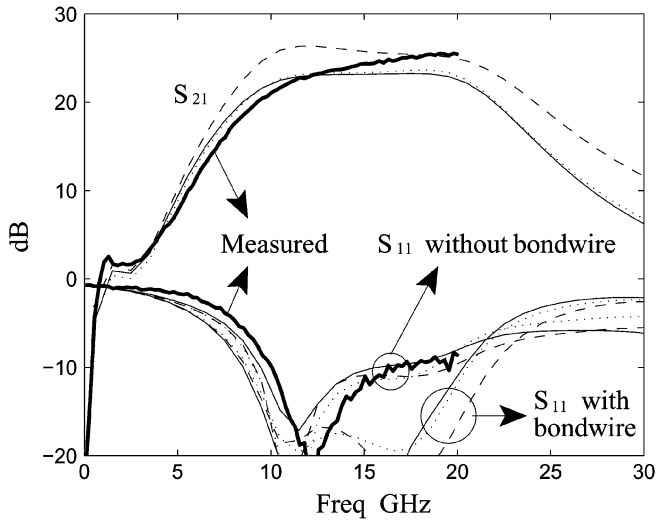

Fig. 16. Measured and simulated S_{21} and S_{11} of the LNA on-wafer at room temperature. The two darkened solid curves are the measured results; the other curves, as solid, dashed, and dotted, are the simulated ones. Another set of simulated S_{11}, where the input bond wire is taken into account, has also been included in this figure.

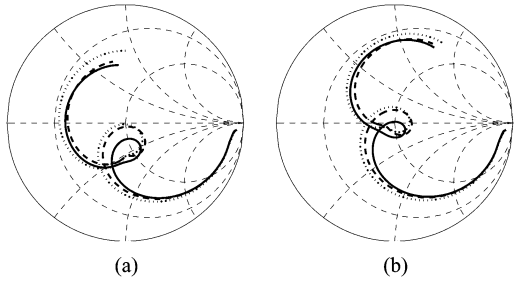

Fig. 17. Simulated S_{11} of the LNA from 0.1 to 30 GHz. (a) There is no input bond wire in front of the circuit. (b) When input bond wire is included, the simulated S_{11} contour will rotate clockwise.

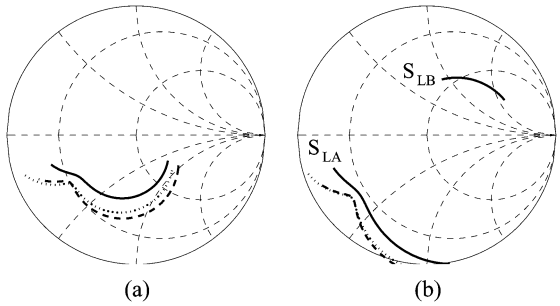

Fig. 18. Simulated output loading reflection coefficient for the first-stage transistor from 10 to 20 GHz. (a) Total output loading reflection coefficient. (b) Two constituting reflection coefficients S_{LA} and S_{LB}, which are defined in the LNA's schematic.

only tapers the gain curve, but also renders an output impedance less reactive. The inclusion of the 30-Ω resistor on each drain branch, though slightly increasing the circuit's power dissipation and noise temperature, ensures a negative S_{11} (in decibels) at very low frequency and, therefore, unconditional stability. The 30-Ω drain resistors on the second and third stages are further split into 10- and 20-Ω ones, which, when combined with large bypass capacitors, form low-pass filters and shore up the signal isolation along the common drain bus.

The first-stage transistor has it source connected to ground, i.e., the $100 \times 100\ \mu\text{m}^2$ via pad, by way of a 110-μm-long transmission line, which can be viewed as the aforementioned L_{FB} inductor. The source of the second (and also the third) transistor is directly connected to its two adjacent ground pads so the via's inductive effect can be reduced and, thus, boosts the circuit's gain response at high frequency. To have a matched output impedance, an 18-Ω resistor is added. Since the LNA already has a large S_{21}, this resistor-caused gain loss can be tolerated and its noise contribution is also small.

The simulated and measured results of this circuit on-wafer at room temperature are presented in Fig. 16. Here, the darkened solid curves are the results measured on-wafer with $V_d = 1.1$ V, $I_d = 36$ mA, $V_g = -0.49$ V, and $I_g = -0.52\ \mu$A, and the testing power of the vector network analyzer is -40 dBm; the other curves are the simulated results where three transistor models, extracted from different wafers and under different bias conditions, are employed. Since during packaging bond wire 200–300-μm long has to be included at the input (and also output), its impact on S_{11} has to be taken into account. Fig. 17(a) shows the simulated S_{11} of the LNA from 0.1 to 30 GHz without the input bond wire. Once input bond wire is added, as in Fig. 17(b), this LNA becomes perfectly wide-band matched.

As discussed in Section III, appropriate RC output loading impedance for the LNA's first-stage transistor is crucial in achieving matched input impedance over wide bandwidth. Fig. 18(a) thus shows the simulated 10–20-GHz output loading reflection coefficient for the first-stage transistor and, again, three different transistor models are employed. Being on the lower half of the Smith chart, they resemble that of an RC circuit. A further decomposition is presented in Fig. 18(b), where S_{LA} is the input reflection coefficient looking specifically into the second-stage transistor and resembles S_{in} of a one-port RC circuit; S_{LB} is the input reflection coefficient looking into the drain bias branch and is similar to S_{in} of an RL circuit.

After carrying out the S-parameter measurement, this circuit is ready to be characterized in terms of noise. As known, noise temperature of a two-port circuit can be expressed as a function of its noise parameters: minimum noise temperature $T_{\min}$, noise ratio N, and optimum reflection coefficient $\Gamma_{\text{opt}} (= \gamma_{\text{opt}} \exp(j\theta_{\text{opt}}))$, which is a complex number, i.e.,

$$T_n = T_{\min} + 4T_0 N \frac{|\Gamma_g - \Gamma_{\text{opt}}|^2}{(1 - |\Gamma_g|^2)(1 - |\Gamma_{\text{opt}}|^2)} \tag{23}$$

where T_0 is 290 K and $\Gamma_g (= \gamma_g \exp(j\theta_g))$ is the generator reflection coefficient. The reason why noise ratio N rather than the conventional noise resistance R_n has been adopted is because N is invariant to lossless transformation [28]. The relationship between N and R_n is

$$N = R_n \cdot \text{Re}[Y_{\text{opt}}] \tag{24}$$

where Y_{opt} is the optimum generator admittance. For a physical two-port circuit, there is one more constraint, i.e., the value of $4T_0N/T_{\min}$ must be larger than one, which implies the correlation coefficient between the two noise waves out of ports 1 and 2 cannot be larger than one [29], [30].

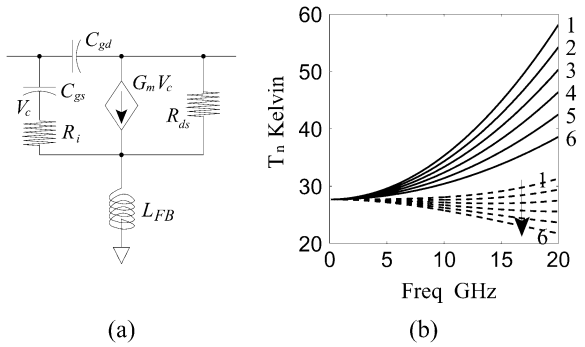

Fig. 19. Schematic of the transistor circuit and its simulated noise temperature with 50-Ω generator impedance. (a) In the schematic, R_i is assumed to be at ambient temperature, while $R_{\rm ds}$ is at temperature $T_{\rm drain}$. (b) In the simulated T_n, solid curves 1–6 correspond to the transistor circuit with no $L_{\rm FB}$ and the correlation coefficient between R_i-induced noise voltage and $R_{\rm ds}$-induced noise current is 0, 0.2, 0.4, 0.6, 0.8, and 1.0, respectively. The six dashed curves are for the transistor circuit with 200-pH $L_{\rm FB}$ and the noise correlation coefficient is changing from 0 to 1 again.

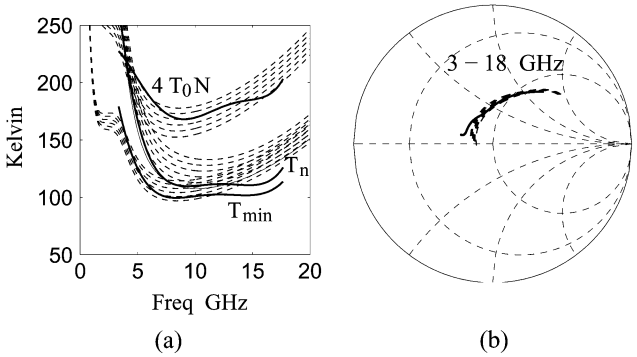

Fig. 20. Measured and simulated noise characteristics of the LNA on-wafer at room temperature. (a) The solid curves are the measured $4T_0N$, T_n and $T_{\rm min}$; the accompanying dashed curves are their simulated counterparts with noise correlation coefficient changing from 0 to 1. (b) The measured and simulated $\Gamma_{\rm opt}$.

When a small gate resistor R_i is included for better transistor modeling [31], [32], noise temperature of the transistor circuit, like that of Fig. 19(a), will now be a function of the correlation coefficient between the noise voltage from R_i at temperature $T_{\rm amb}$ and the noise current from $R_{\rm ds}$ at temperature $T_{\rm drain}$. The simulated results are presented in Fig. 19(b) where the solid curves are without any $L_{\rm FB}$, while dashed curves have a 200-pH source inductor $L_{\rm FB}$ added to the transistor. Curves 1–6 correspond to correlation value of 0, 0.2, 0.4, 0.6, 0.8, and 1.0, respectively. Here, R_i is set to 1 Ω and $T_{\rm drain}$ is assumed to be 2300 K. Due to the difficulty in carrying out noise-parameter measurement accurately down to the transistor level [33], different (rather than one specific) values of the correlation coefficient are used in the LNA's noise simulation.

Fig. 20 shows both the measured and simulated noise characteristics of the LNA on-wafer at room temperature with $T_{\rm drain}$ set to 2300 K. The solid curves are the measured results with LNA biased at 36 mA and 1.1 V, and the dashed curves are the simulated counterparts with the noise correlation coefficient changing from 0 to 1, with step size equal to 0.2. It is the LNA's small S_{21} and large T_n at 3 GHz that set the low-frequency limit in the noise measurement; the 18-GHz high-frequency measurement limit is imposed by the available frequency range of the

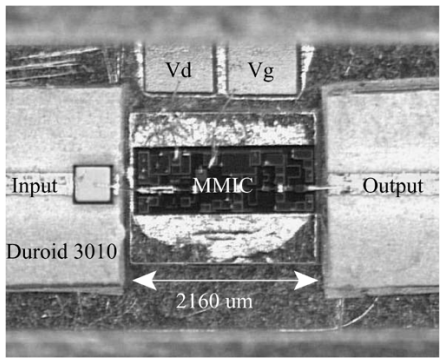

Fig. 21. Packaged LNA with the integrated circuit inside. The input and output 50-Ω transmission lines are on the Duroid 3010 substrate. In addition to the two capacitors for drain and gate biases, a third capacitor is added at the input of the circuit for dc-blocking purpose.

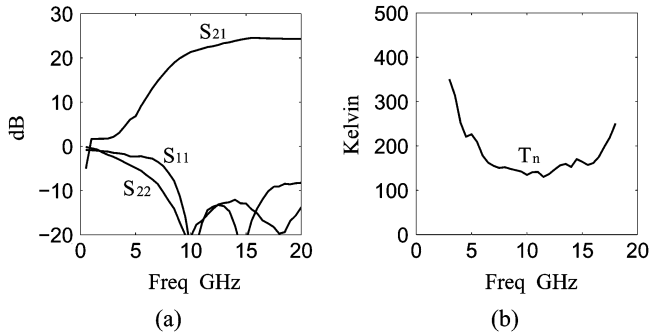

Fig. 22. S-parameters and noise temperature of the packaged LNA at room temperature. (a) Measured S-parameters of this packaged LNA. S_{12} is below −20 dB and not displayed here. (b) Measured noise temperature with 50-Ω generator impedance.

noise source itself. The LNA's noise parameters, as measured on-wafer using a wide-band frequency-variation method [34], has its in-band $4T_0N/T_{\rm min}$ ratio equal to 1.7, which is a reasonable number. The high-frequency discrepancy between the simulated and measured curves can be accounted for in terms of the slightly smaller S_{21} in the simulation at high frequency. Revised modeling of the constituting components should result in more agreeing S_{21} curves, thus minimizes the noise temperature difference. Simulated $\Gamma_{\rm opt}$, nevertheless, shows little dependency on the noise correlation coefficient and is close to the measured one.

The packaged LNA is shown in Fig. 21. Both the input and output 50-Ω microstrip lines are on a 10-mil Duroid 3010 substrate, which has a large dielectric constant and is easy to handle, but tends to be lossy at high frequency. The circuit is attached using silver epoxy to the gold-plated copper chassis, which is designed to have isolation better than 40 dB at 20 GHz when the amplifier circuit is not biased. Since the on-chip input capacitor has been short circuited accidentally, an external chip capacitor for dc blocking has to be added. Due to the unleveled top surfaces of this chip capacitor and the amplifier circuit, a longer 1-mil input bond wire has to be used, and that causes the LNA's S_{11} to be matched at the slightly lower 10 and 15 GHz. A more agreeable S_{11} should be obtained by using a connector-type dc-blocking capacitor at the input. Fig. 22 shows the measured S-parameters and noise temperature of this packaged LNA. The

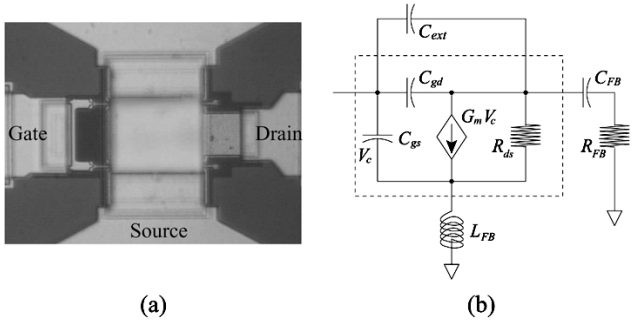

Fig. 23. 100-μm transistor and its corresponding double-feedback circuit configuration for ultra-wide-band application. (a) Photograph of this 100-μm transistor, which has its gate split into two fingers. (b) In the double-feedback circuit configuration, an external $C_{\rm ext}$ is added to increase the equivalent gate–drain capacitance, thus allowing a smaller transistor (such as this 100-μm one) to be used.

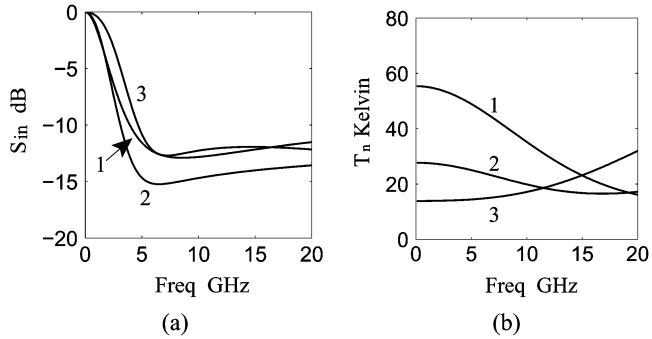

Fig. 24. Simulated input reflection coefficients and noise temperatures of three ultra-wide-band transistor circuits, as specified in Table I. (a) $S_{\rm in}$ in decibels versus gigahertz. (b) The corresponding T_n with 50-Ω generator impedance.

TABLE I
THREE DIFFERENT ULTRA-WIDE-BAND TRANSISTOR CIRCUITS

.	C_{gs}	C_{gd}	G_m	R_{ds}	L_{FB}	C_{FB}	R_{RB}	C_{ext}
1	60	18	78	120	600	400	100	54
2	120	36	156	60	500	600	80	36
3	240	72	312	30	400	300	60	0

flat -9-dB S_{11} curve toward 20 GHz exhibits the typical wide-band characteristic. This LNA can be cooled down in cryostat to have ultra-low noise temperature suitable for radio-astronomy and atmospheric applications [35]–[37].

V. BANDWIDTH BROADENING FOR POTENTIAL ULTRA-WIDE-BAND LNA DESIGN

Thus far in this paper, we have analyzed and demonstrated the feasibility of designing a matched 10–20-GHz LNA using the novel wide-band approach. Compared with the 20-GHz high end where further design iterations ensure an even smaller input reflection coefficient, much of the design challenge lies in achieving a good S_{11} at 10 GHz, which is indeed the limiting factor in determining the circuit's relative bandwidth. One may wonder whether this 10-GHz frequency point can be halved to have an ultra-wide-band 5–20-GHz LNA. Granted, the most straightforward way is using a larger transistor, probably twice the original size. Based on the wide-band theory contrived, the second approach is keeping the transistor unchanged while adding an external capacitor $C_{\rm ext}$ in parallel with the intrinsic capacitor $C_{\rm gd}$, thus boosting the intended feedback response at low frequency. Naturally, the third approach is having a small 100-μm transistor in combination with a large $C_{\rm ext}$. Fig. 23(a) shows the 100-μm transistor, which has a layout that resembles the 200-μm transistor, but has the number of fingers halved from 4 to 2. It is, therefore, reasonable to assume that its intrinsic parameters can be linearly scaled from that of the 200-μm one. Fig. 23(b) shows the ultra-wide-band circuit configuration with double feedback formed by $C_{\rm gd}$ and $C_{\rm ext}$.

The simulated $S_{\rm in}$ and T_n of these ultra-wide-band circuits, with $T_{\rm drain} = 2300$ K, are presented in Fig. 24 where curve 1 is with a 100-μm transistor and a large $C_{\rm ext}$; curve 2 is with a 200-μm transistor and a small $C_{\rm ext}$, and curve 3 is with a 400-μm transistor and has no $C_{\rm ext}$. Though roughly in par with curve 2, it is the double power dissipation that runs against curve 3. The reason why curve 1 has a much larger noise temperature at low frequency is because T_n is inversely proportional to $G_m^2 R_{\rm ds}$ [see (13)] and, thus, is inversely proportional to the size of the transistor. Parameters used in the simulation are tabulated in Table I where row 1 is for the 100-μm transistor circuit, row 2 is for the 200-μm one, and row 3 is for the 400-μm one. Here the resistance is in ohms, capacitance is in femtofarads, and inductance is in picohenrys. Of course, if we want to design an LNA with even wider bandwidth, a slightly larger transistor with some moderate value of $C_{\rm ext}$ has to be contemplated given that the transistor's parameters are difficult to manipulate separately through process techniques.

VI. CONCLUSION

In this paper, a novel feedback approach for wide-band LNA design has been suggested and analyzed in detail. Agreements between the mathematical expressions and their simulated counterparts have confirmed this approach's validity. A 10–20-GHz wide-band LNA was then designed and characterized. This is the first time an accurate and thorough account of how wide-band LNA works has been carried out has been presented. The methodology proposed here will be useful for the future design of ultra-wide-band LNAs.

ACKNOWLEDGMENT

The author thanks S. Weinreb, J. Zmuidzinas, D. Miller, M. Edgar, J. Kooi, and N. Wadefalk, all with the California Institute of Technology, Pasadena, J. Ward and G. Chattopadhyay, both with the Jet Propulsion Laboratory (JPL), Pasadena, CA, S. I. Tsai, L. Yang and T. H. Sang, all with the National Chiao Tung University (NCTU), Hsin-Chu, Taiwan, R.O.C., F. K. Y. Lo, with the National Radio Astronomy Observatory (NRAO), Charlottesville, VA, and the anonymous reviewers of this TRANSACTIONS for suggestions and encouragement.

REFERENCES

[1] R. C. Mott, "A GaAs monolithic 6 GHz low-noise amplifier for satellite receivers," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 3, pp. 565–570, Mar. 1989.

[2] F. Seguin, B. Godara, F. Alicalapa, and A. Fabre, "A gain-controllable wide-band low-noise amplifier in low-cost 0.8-μm Si BiCMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 1, pp. 154–160, Jan. 2004.

[3] D. Barras, F. Ellinger, H. Jackel, and W. Hirt, "A low supply voltage SiGe LNA for ultra-wideband front ends," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 10, pp. 469–471, Oct. 2004.
[4] S. Weinreb, D. L. Fenstermacher, and R. W. Harris, "Ultra-low-noise 1.2–1.7-GHz cooled GaAsFET amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-82, no. 6, pp. 849–853, Jun. 1982.
[5] N. R. Erickson, R. M. Grosslein, R. B. Erickson, and S. Weinreb, "A cryogenic focal plane array for 85–115 GHz using MMIC preamplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 12, pp. 2212–2219, Dec. 1999.
[6] N. Wadefalk, A. Melberg, I. Angelov, M. E. Barsky, S. Bui, E. Choumas, R. W. Grundbacher, E. L. Kollberg, R. Lai, N. Rorsman, P. Starski, J. Stenarson, D. C. Streit, and H. Zirath, "Cryogenic wide-band ultra-low-noise IF amplifiers operating at ultra-low DC power," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 6, pp. 1705–1711, Jun. 2003.
[7] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*. Englewood Cliffs, NJ: Prentice-Hall, 1984.
[8] R. Goyal, *High-Frequency Analog Integrated Circuit Design*. New York: Wiley, 1995.
[9] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New York: Wiley, 1990.
[10] Y. J. Jeon, M. Y. Jeon, J. M. Kim, Y. H. Jeon, D. H. Jeon, and D. M. Kim, "Monolithic feedback low noise X-band amplifiers using 0.5-μm GaAs MESFET's: Comparative theoretical study and experimental characterization," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 275–279, Feb. 1998.
[11] C. P. Chang and H. R. Chuang, "0.18 μm 3–6 GHz CMOS broad-band LNA for UWB radio," *Electron. Lett.*, vol. 41, pp. 696–697, Jun. 2005.
[12] C. H. Liao and H. R. Chuang, "A 5.7-GHz 0.18-μm CMOS gain-controlled differential LNA with current reuse for WLNA receiver," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 12, pp. 526–528, Dec. 2003.
[13] F. Bruccoleri, E. Klumperink, and B. Nauta, "Generating all two-MOS-transistor amplifiers leads to new wide-band LNA," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1032–1040, Jul. 2001.
[14] J. S. Goo, H. T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee, and R. W. Dutton, "A noise optimization technique for integrated low-noise amplifiers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 994–1002, Aug. 2002.
[15] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee, "COMS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 8, pp. 1079–1085, Aug. 1990.
[16] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004.
[17] W. L. Jung and J. S. Wu, "Stable broad-band microwave amplifier design," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 8, pp. 1079–1085, Aug. 1990.
[18] H. J. Carlin and P. P. Civalleri, "An algorithm for wide-band matching using Weiner–Lee transforms," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 39, no. 7, pp. 497–505, Jul. 1992.
[19] A. Ismail and A. A. Abidi, "A 3–10-GHz low-noise amplifier with wide-band LC-ladder matching network," *IEEE J. Soild-State Circuits*, vol. 39, no. 12, pp. 2269–2277, Dec. 2004.
[20] R. Hu and M. S. Yang, "Investigation of different input-matching mechanisms used in wide-band LNA design," *Int. J. Infrared Millim. Waves*, vol. 26, pp. 221–245, Feb. 2005.
[21] K. H. Duh, M. W. Pospieszalski, W. F. Kopp, P. Ho, A. A. Jabra, P. C. Chao, P. M. Smith, L. F. Lester, J. M. Ballingall, and S. Weinreb, "Ultra-low-noise cryogenic high-electron-mobility transistors," *IEEE Trans. Electron Devices*, vol. 35, no. 3, pp. 249–256, Mar. 1988.
[22] P. C. Chao, S. C. Palmateer, P. M. Smith, U. K. Mishra, K. H. Duh, and J. C. M. Huang, "Millimeter-wave low-noise high electron mobility transistor," *IEEE Electron Device Lett.*, vol. EDL-6, no. 10, pp. 531–533, Oct. 1985.
[23] P. R. Jay *et al.*, "Design of TEGFET device for optimum low-noise high-frequency operation," *IEEE Trans. Electron Devices*, vol. ED-33, no. 5, pp. 590–594, May 1986.
[24] R. Hu, "An 8–20 GHz wide-band LNA design and the analysis of its input matching mechanism," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 11, pp. 528–530, Nov. 2004.
[25] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.
[26] A. Eskandarian and S. Weinreb, "A note on experimental determination of small-signal equivalent circuit of millimeter-wave FETs," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 1, pp. 159–162, Jan. 1993.
[27] M. Morgan, "Millimeter-wave MMIC's and application," Ph.D. dissertation, Dept. Elect. Eng., California Inst. Technol., Pasadena, CA, 2003.
[28] J. Lange, "Noise characterization of linear two ports in terms of invariant parameters," *IEEE J. Solid-State Circuits*, vol. SC-2, no. 6, pp. 37–40, Jun. 1967.
[29] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 9, pp. 1340–1350, Sep. 1989.
[30] M. W. Pospieszalski and W. Wiatr, "Comments on 'Design of microwave GaAs MESFET's for broad-band low-noise amplifier'," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-34, no. 1, pp. 194–194, Jan. 1986.
[31] K. H. Duh, P. C. Chao, P. M. Smith, L. F. Lester, B. R. Lee, J. M. Ballingall, and M. Y. Kao, "High-performance Ka-band and V-band HEMT low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 12, pp. 1598–1603, Dec. 1988.
[32] J. Chen and B. Shi, "Impact of intrinsic channel resistance on noise performance of CMOS LNA," *IEEE Electron Device Lett.*, vol. 23, pp. 34–36, Jan. 2002.
[33] R. Hu and T. Z. Sang, "On-wafer noise parameter measurements using wide-band frequency-variation method," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 7, pp. 2398–2402, Jul. 2005.
[34] R. Hu and S. Weinreb, "A novel wide-band noise-parameter measurement method and its cryogenic application," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1498–1507, May 2004.
[35] R. Hu, "Analysis of the input noise contribution in the noise temperature measurements," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 3, pp. 141–143, Mar. 2005.
[36] F. Rice, M. Sumner, J. Zmuidzinas, R. Hu, H. G. Leduc, A. I. Harris, and D. Miller, "SIS mixer design for a broad-band millimeter spectrometer suitable for rapid line surveys and redshift determinations," *Proc. SPIE–Int. Soc. Opt. Eng.*, vol. 4855, pp. 301–311, Feb. 2003.
[37] I. L. Fernandiz, J. D. Gallego, C. Diez, A. Barcia, and J. M. Pintado, "Wide-band ultra low noise cryogenic InP IF amplifiers for the Hershel mission radiometers," *Proc. SPIE–Int. Soc. Opt. Eng.*, vol. 4855, pp. 489–500, Feb. 2003.

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