Higher Gate Capacitance Ge n-MOSFETs Using Laser Annealing

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***Abstract*—By applying laser annealing (LA) on both gate dielectrics and source/drain activation, the $TaN/ZrO_2/La_2O_3/SiO_2$ on Ge n-MOSFETs shows a high gate capacitance density, a small n^+/p-junction ideality factor of 1.10, a small subthreshold swing (SS) of 106 mV/dec, and a good high-field mobility of 285 or 340 $cm^2/V \cdot s$ after gate leakage correction at 1 MV/cm, at a small 0.95-nm equivalent oxide thickness (EOT). To the best of our knowledge, this is the first demonstration of significantly high gate capacitance in MOSFETs by LA. This is also the highest 1-MV/cm mobility at the smallest EOT of Ge n-MOSFETs and better than the SiO_2/Si universal mobility.**

***Index Terms*—Annealing, gate dielectric, Ge, high-κ, laser.**

I. Introduction

GERMANIUM has attracted much attention due to its features of both higher electron and hole mobilities than Si [1]–[15]. Furthermore, Ge has $\sim 50\times$ higher density of state than InGaAs to deliver high transistor current. The integration of Ge on Si can be realized by using a Ge-on-insulator (GOI or GeOI) structure [1], where defect-free Ge has been realized. This GeOI structure can also suppress the leakage current of small-energy-bandgap Ge and is useful for device-level 3-D ICs [16]. The Ge p-MOSFET also shows $2.5\times$ better high-field hole mobility at 1 MV/cm than the SiO_2/Si universal mobility at a small 1.4-nm equivalent oxide thickness (EOT) [16]. Nevertheless, achievement of good high-field electron mobility for Ge n-MOSFETs at a small EOT is still under development, but the small EOT of $\sim$0.95 nm is needed to compete with metal-gate/high-κ/strained-Si n-MOSFETs at 32-nm nodes. The poor Ge n-MOSFET is due to the low source–drain doping activation by RTA and poor high-κ/Ge interface property.

In this letter, we have used laser annealing (LA) [7], [17]–[21] to improve both gate capacitance and n^+/p junction of Ge n-MOSFET [15], [16]. Application of LA on a gate dielectric lowers the EOT from 1.6 to 0.95 nm. Using LA, $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ n-MOSFET shows excellent high-field mobility at 1 MV/cm and 0.95-nm EOT. Such good high-field mobility is necessary for highly scaled MOSFETs at a small EOT, operated at a high effective electric field ($E_{\rm eff}$).

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II. Experimental Procedure

We used 2-in p-type Ge (100) wafers with 10-$\Omega \cdot$cm resistivity in the experiments. After standard cleaning, isolation oxides were formed by plasma-enhanced chemical vapor deposition. After the source and drain were defined with the SiO_2 dummy gate, phosphorus ion was implanted at the source–drain region at 35 keV and 5×10^{15} cm^{-2}, followed by KrF LA (248 nm, $\sim$30-ns pulse) for source–drain activation [16]. After pregate cleaning in cyclic diluted HF (1:50) and rinsing in DI water, ultrathin 0.8-nm SiO_2, 1-nm high-κ La_2O_3, and 3-nm high-κ ZrO_2 were deposited by physical vapor deposition [15], followed by postdeposition anneal (PDA) under oxygen ambient. Then, the second LA was applied to increase the gate capacitance density. The LA was performed under air ambient. The laser spot sizes were 0.3 cm^2 after focus and 0.9 cm^2 without focus for n^+/p junction and high-κ dielectric annealing, respectively, where continuous stepping in the X- and Y-directions was used for the whole sample. Finally, the TaN gate electrode and source–drain Al contacts were deposited to form the Ge n-MOSFET. The contact window on the source–drain was formed using BOE to remove the gate dielectric.

III. Results and Discussion

Fig. 1(a) and (b) shows the C–V and J–V characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ MOS capacitors formed by PDA, followed by LA and control 550 °C RTA. The LA significantly increases the gate capacitance to 2.7 μF/cm^2 that gives a capacitance equivalent thickness of 1.27 nm. A sharp gate-stack/Ge interface after LA was also observed by TEM. In addition, only a small *flatband* ($V_{\rm fb}$) shift and an increasing gate current were found by LA. The necessary negative $V_{\rm fb}$ value for a low-threshold-voltage (V_t) n-MOSFET is due to the unique property of the La_2O_3 gate dielectric [22] that is related to the positively charged oxygen vacancies [23]. The good high-κ quality after LA is evident from the small C–V hysteresis of only 21 mV, from -3 to 1 V sweep, and better than the 73 mV in control RTA device. An EOT of 0.95 nm was obtained from Berkeley's quantum–mechanical C–V simulator with Ge material parameters [7], [15], [24].

LA can also improve the source–drain junction characteristics. Fig. 2 shows the n^+/p-junction characteristics of P^+-implanted p-Ge after LA. At a laser fluence of 0.25 J/cm^2, a small junction ideality factor (n) of 1.10 and the largest forward current were obtained while still maintaining a low reverse leakage current. These results were better than those of control 550 °C RTA devices. In addition, a low sheet resistance (R_s) of 73 Ω/sq was measured after LA and better than the 105 Ω/sq

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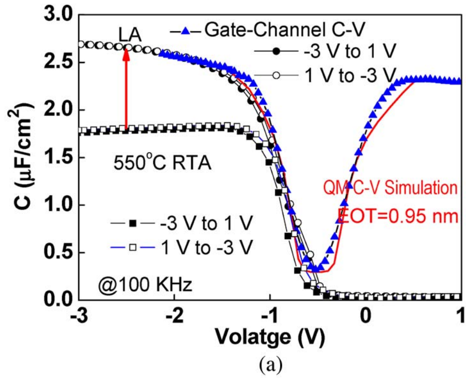
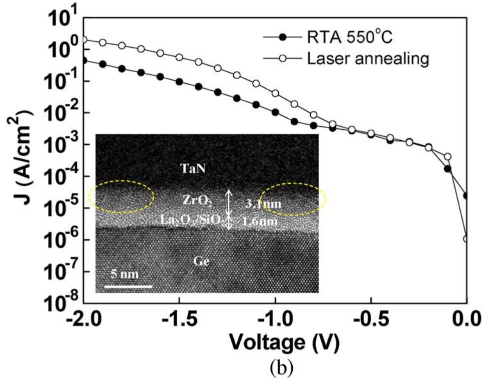


(a)



(b)

Fig. 1. (a) C–V and (b) J–V characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ n-MOS capacitors after 550 °C RTA and LA. The insert figure shows the cross-sectional TEM image after LA.

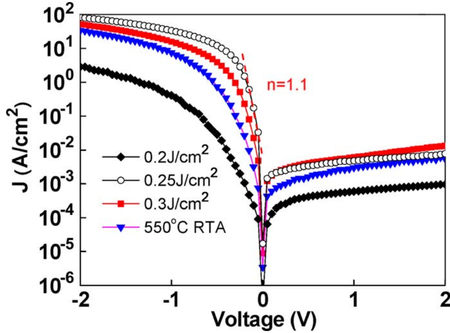


Fig. 2. n^+/p-junction characteristics of P^+-implanted Ge after LA.

using 550 °C RTA. This LA fluence is lower than the previous 0.36 J/cm^2 to activate the ion-implanted Si MOSFET [18], which is due to the lower melting temperature of Ge than Si.

Fig. 3(a) and (b) shows the I_d–V_d and I_d–V_g characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/Ge$ n-MOSFETs using LA. Well-behaved transistor characteristics were reached with a good subthreshold swing of 106 mV/dec that leads to an interface trap density of 1.3×10^{13} eV$^{-1} \cdot$ cm^{-2} [25]. A small threshold voltage (V_t) of 0.18 V is due to the negative V_{fb} measured from the C–V characteristics shown in Fig. 1(a).

Fig. 4 shows the mobility as a function of E_{eff} over a wide range, which was obtained with and without gate leakage current correction [26]. Standard split C–V at 100 kHz was used for mobility extraction without gate leakage correction. A very high 1-MV/cm mobility of 285 or 340 cm^2/V $\cdot$ s after gate leakage correction was reached for the metal-gate/high-κ/Ge n-MOSFETs, using LA at a small 0.95-nm EOT. It is important to note that the electron mobility was higher than the Si universal mobility at 1-MV/cm E_{eff}, which is also the best high-field mobility data of electron mobility of Ge n-MOSFETs at the smallest EOT [1]–[15]. The slightly smaller low-field mobility with gate leakage current correction is due to device variation. The good high-field mobility using LA is attributed to the concentrated 5.0-eV laser energy absorbed near the Ge surface, which, in turn, heats up the gate dielectrics and thereby improves the interface. The ultrafast ~30-ns LA can also reduce the interface reaction [27] and improve the mobility. These are supported from the much better C–V hysteresis and mobility shown in Figs. 1 and 4, respectively, to improve both dielectric and dielectric/Ge interface.

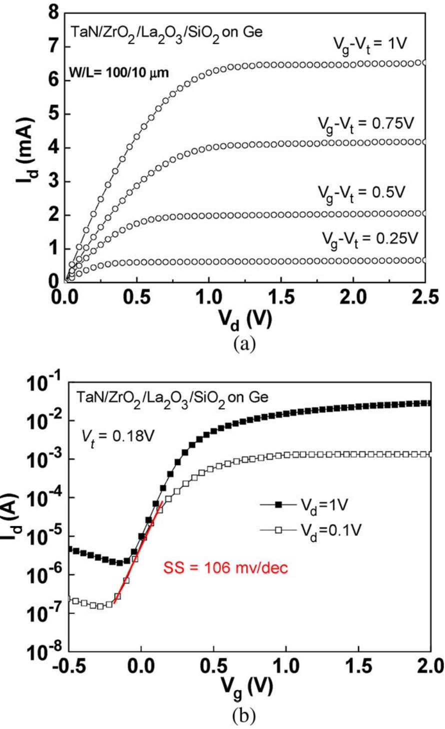


Fig. 3. (a) I_d–V_d and (b) I_d–V_g characteristics of $TaN/ZrO_2/La_2O_3/SiO_2/$ Ge n-MOS using LA.

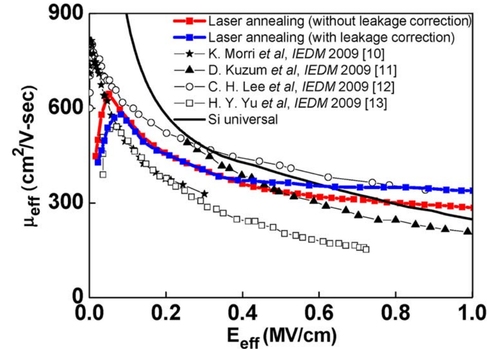


Fig. 4. Electron mobility as a function of the effective electric field of $TaN/ZrO_2/La_2O_3/SiO_2$ on Ge n-MOSFET using LA.

IV. Conclusion

By applying low-energy LA on $TaN/La_2O_3/SiO_2/Ge$ n-MOSFETs, a small junction n factor of 1.10, a small

106-mV/dec SS, and a good 1-MV/cm high field mobility were reached simultaneously at a small EOT of 0.95 nm.

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