行政院國家科學委員會專題研究計畫　成果報告

覆晶銲錫接點之熱電效應及其抗電遷移之研究

計畫類別：整合型計畫
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計畫主持人：陳智

計畫參與人員：邱聖翔 梁世緯 張元蔚 陳俊宏

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報告附件：出席國際會議研究心得報告及發表論文
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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
□期中進度報告

電子產品軟焊焊點及界面之研究－
覆晶銲錫接點之熱電效應及其抗電遷移之研究

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摘要

本研究主要針對共晶錫鉛(SnPb)與無鉛銲錫，錫銀(SnAg3.5)覆晶銲錫接點在電遷移現象中電流與溫度的兩種現象來做探討，研究中主要利用紅外線熱像儀(IR)來量測電子元件裡的溫度變化，更以此來探討覆晶結構在高電流密度底下所產生的電熱效應以及不同尺寸的鋁導線對於電遷移效應底下破壞時間的影響。。最後再配合電腦模擬來解出銲錫接點內的電流密度分佈及溫度分佈，再研究如何提升銲錫接點的抗電遷移能力，提升他們的使用壽命。

本研究主要針對共晶錫鉛之覆晶結構在高電流密度下進行電遷移現像研究。本研究使用兩種不同結構的銲錫之覆晶封裝試片，第一種試片所使用之UBM爲Ti/Cr-Cu/Cu(晶片端)與Cu/Ni(P)/Au(基板端)；第二種試片所使用之UBM爲Ni/Cu(晶片端)與Cu/Ni(基板端)。研究顯示在通電過程中，鋁導線是最主要的發熱源，是產生焦耳熱效應的最主要因素之一。經由電腦模擬結果發現，在通電過程中，在鋁導線與銲錫接點入口處會有一熱點(hot spot)產生，熱點的溫度更會隨著外加電流的增加而提升，這個熱點的存在對於覆晶結構有加速破壞的影響。特別是在陰極端產生加速產生氣孔導致覆晶結構沿著界面破壞。

鋁導線的尺寸也會對覆晶銲錫接點的電遷移破壞時間也有很大的影響，實驗結果顯示，加寬與縮短鋁導線的長度可以延長整個覆晶銲錫接點的電遷移破壞時間。

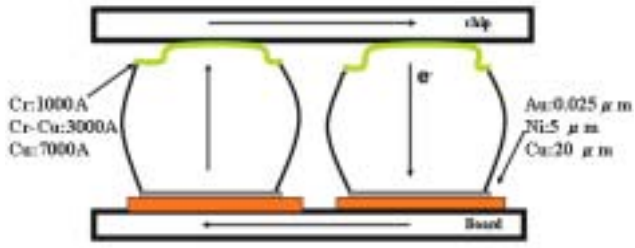
前言

在電子元件輕薄短小與功能日新月異的趨勢下，覆晶封裝(Flip chip packaging)已然成爲高階電子元件產品之主要封裝方式。現今電路設計的要求下，每個銲錫球將傳輸約 0.2A之電流，在不久的將來將會高至 0.4A，以 50μm直徑的銲錫球來計算其電流密度將高達 10^4A/cm^2，在元件操作溫度 100℃下(已超過銲錫球熔點絕對溫度之一半以上)，電子遷移將對銲錫球之可靠度造成危害。最早在 1960 年代就開始有鋁、銀金屬的電遷移（electromigration, EM）研究等等[1,2,3]。Pro. Tu察覺到此問題可能的嚴重性而開始著手研究*含鉛銲錫* Electromigration[4-8]。對於無鉛銲錫的Electromigration，目前已陸續有相關論文發表[9-10]。而在美國工業界則有Intel, IBM, 以及Flip Chip Technology三家公司開始重視此問題並各自有研究部門在探討此問題。

本研究針對覆晶封裝中電子遷移對銲錫球之可靠度所造成之危害進行研究並提出解決之道，同時找出銲錫材料有關之電遷移參數如材料的選擇、線路的設計…等，來提供工業界之參考。

實驗步驟

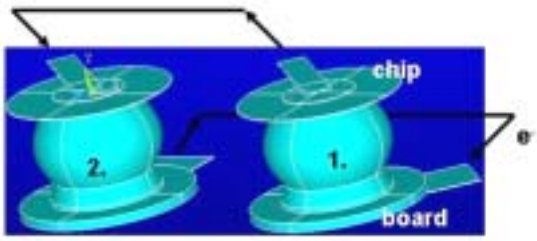
圖一爲本研究之覆晶試片結構圖，晶片端之 UBM 分別爲 Cr，phase-in Cr-Cu，與 Cu，其厚度分別爲 1000A，3000A 與 7000A。基板端之 UBM 分別爲 Cu：20μm ，Ni: 5μm ，Au : 0.25μm。



圖一、 覆晶試片結構圖。

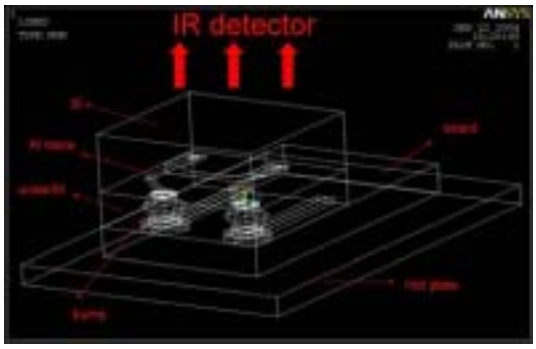
銲錫則在高於其熔點 30 度下首先與晶片端接合(reflow)，接著再與基板端對準進行第二次接合(reflow)。

圖二爲本研究之試片 3D結構圖，電子流從二號bump之晶片端 45^0角進入，再由基板端之後方流出，接著由一號bump晶片端 45^0角進入，再由基板端後方 45^0角流出。



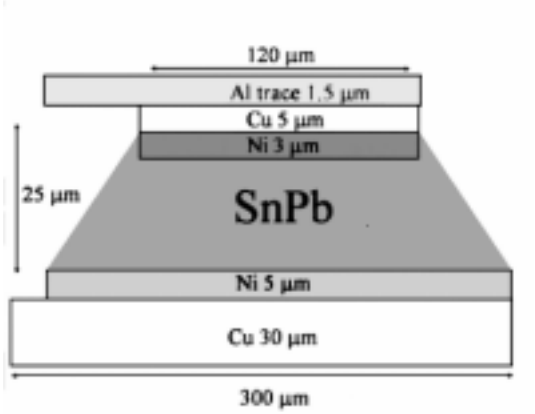
圖二、試片 3D 結構圖。

圖三爲將覆晶試片晶片端朝向 IR 偵測器，IR 可以穿透矽晶片，所以可以透過矽晶片觀察到晶片底下之鋁導線線路結構與通電過程中溫度的分佈。



圖三、 IR 透過矽晶片量測到鋁導線溫度之示意圖。

圖四爲另一組不同結構的銲錫試片，晶片端之 UBM 分別爲 Ni 與 Cu，其厚度分別爲 3μm，5μm 。基板端之 UBM 分別爲 Cu : 30μm ，Ni: 5μm。

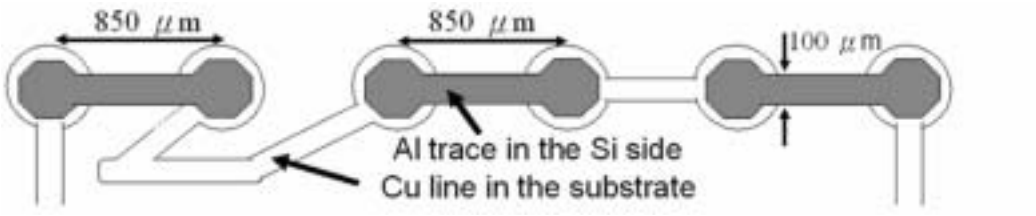


圖四、另一組不同結構的銲錫試片。

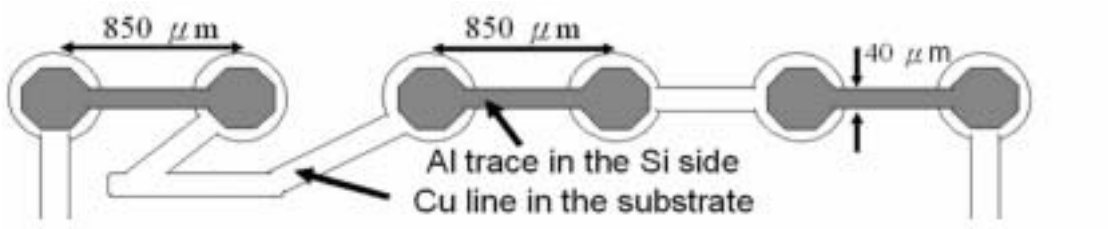
爲了要探討鋁導線尺寸對於覆晶銲錫接點在電遷移效應下破壞時間的影響。本研究設計了三種不同尺寸的鋁導線再做分析。每段導線長度都爲 850um，圖五、六爲 daisy-chain 的結構並且連接有 6 顆銲錫凸塊，鋁導線的總長度爲 2550 μm，寬度分別爲 100μm 與 40μm，厚度皆爲 1.5 μm，利用這兩種結構來探討鋁導線寬度的效應。

第三種結構則如圖七所示，是由三段鋁導線連接在一起，寬度爲 100μm，並且底下有 4

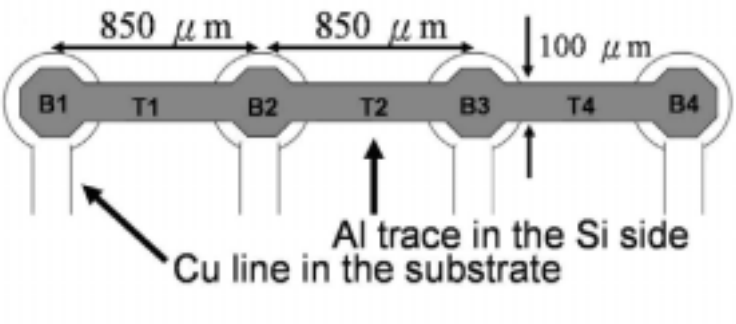
顆銲錫凸塊，3 段鋁導線分別標記爲 T1、T2、T3；四顆銲錫凸塊標記爲 B1~B4。我們可以藉由基板端不同位置的電流，可以來探討不同鋁導線長度對於在電遷移效應下破壞時間的影響。



圖五、daisy-chain 結構，寬度爲 100μm。



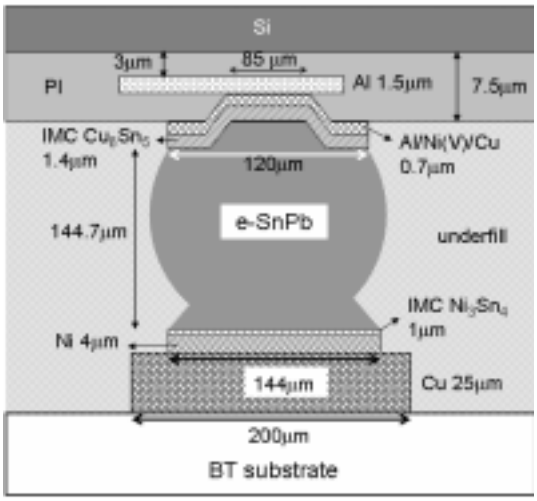
圖六、daisy-chain 結構，寬度爲 40μm。



圖七、不同長度鋁導線結構示意圖。

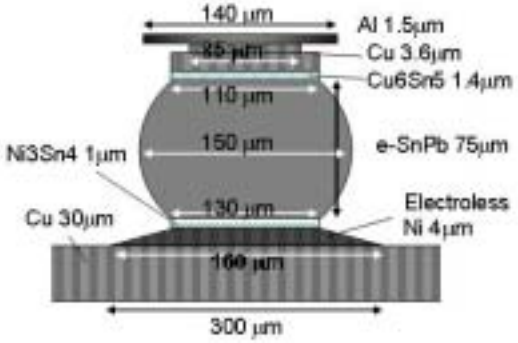
3-D 電腦模擬分析

覆晶封裝試片採用薄膜底部金屬層的模型，見圖九，是選用共晶錫鉛(eutectic SnPb)銲錫，晶片端採用鋁導線，鋁導線的尺寸爲寬 34μm與厚 1.5μm，基板使用銅導線，銅導線的尺寸爲寬 80μm與厚 25μm。晶片端的底部金屬層(UBM)是Al/Ni(V)/Cu 0.7μm，板端採用Ni 4μm。同時考慮介金屬化合物(IMC)的生成，在晶片端爲Cu_6Sn_5 1.4μm，基板則是Ni_3Sn_4 1μm。晶片端的接觸開口(contact opening)直徑爲 85μm，底部金屬層開口(UBM opening)爲 120μm。銲錫的高度爲 144.7μm。



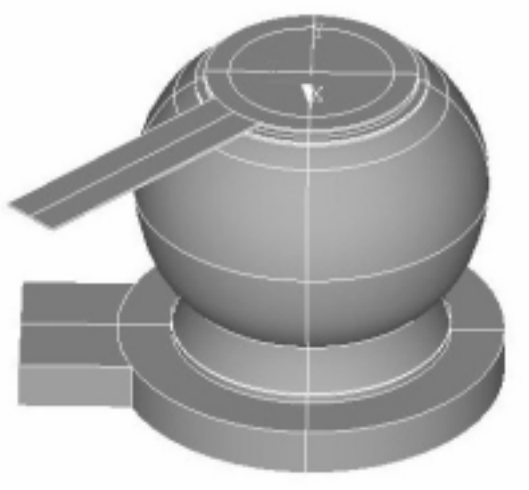
圖九、 覆晶封裝試片在晶片端採用薄膜底部金屬層 Al/Ni(V)/Cu 之結構圖。

另外，用來計算銲錫接點的電阻在量測上的幾何效應，所採用的模型如圖十，一樣選用共晶錫鉛(eutectic SnPb)銲錫，晶片端採用鋁導線，鋁導線的尺寸爲寬 100μm與厚 1.5μm，基板使用銅導線，銅導線的尺寸爲寬 100μm與厚 30μm。晶片端的底部金屬層(UBM)是Cu 3.6μm，板端採無電鍍Ni 4μm。同時考慮介金屬化合物(IMC)的生成，在晶片端爲Cu_6Sn_5 1.4μm，基板則是Ni_3Sn_4 1μm。晶片端的接觸開口(contact opening)直徑爲 85μm，底部金屬層開口(UBM opening)爲 110μm。銲錫的高度爲 75μm。此一銲錫結構會搭配實際量測迴路，將會在結果與討論中提出。

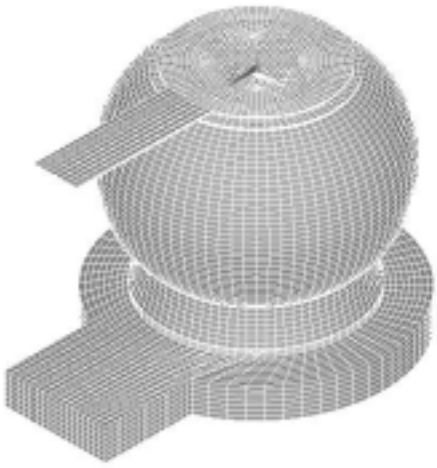


圖十、 覆晶封裝試片在晶片端採用厚膜底部金屬層 Cu 之結構圖。

模型建立是利用國家高速電腦中心提供的ANSYS軟體，這是一個被廣泛使用且方程式健全的科學計算軟體，使用元素的種類爲SOLID69，這是一種八節點式的六面熱電耦合元素。模型建立的步驟使採用由下往上的方式(Bottom-up)，先畫出銲錫的半剖面面積，旋轉360^{o}形成球體，如圖十一。再繪出導線部份，接著將體積網格化(圖十二)，施加邊界條件。此部分即可做電性模擬分析。

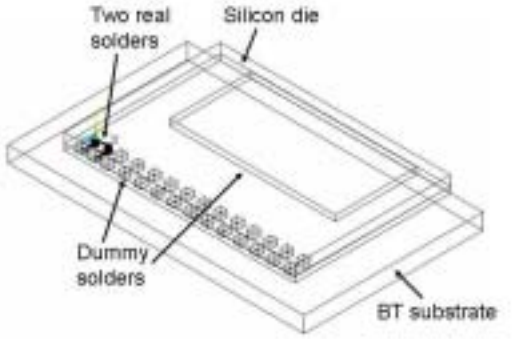


圖十一、 銲錫接點模擬體積圖。



圖十二、 銲錫接點模擬網格化圖。

若是要分析熱電耦合系統，討論溫度分佈情形，爲了配合實際散熱情形與運算的極限，在實際試片中，除了兩顆實際可以電遷移試驗的銲錫球外，對應其他銲錫的部份採用了六面體的取代銲錫(dummy solder)。再將周圍封裝起來，上方加上矽(Si)晶片，下方爲 BT 基板，最後的模型如同圖十三。



圖十三、 封裝試片模擬體積圖。

表一爲模擬所使用的材料的熱電性質，包含熱傳導係數(Thermal conductivity)與電阻率(Resistivity)，其中因爲電阻會隨著溫度上升而上升，TCR 的效應是不可以省去的，也因此增加了模擬計算時的困難度。

Materials	Thermal conductivity (W/m-°C)	Resistivity (μΩ-cm)	TCR ($10^{-3}K^{-1}$)
Silicon	147.0	--	--
Al	238.0	3.2	4.2
Al/Vi(V)/Cu	166.6	29.54	5.6
Cu_6Sn_5	34.1	17.5	4.5
e-SnPb	50.0	14.6	4.4
Ni_3Sn_4	19.6	28.5	5.5
Ni	76.0	6.8	6.8
Cu	403.0	1.7	4.3
Electroless Ni	9.32	70.0	6.8
BT	0.70	--	--
Underfill	0.55	--	--
Passivation	0.34	--	--

表一、模擬所使用的材料參數。

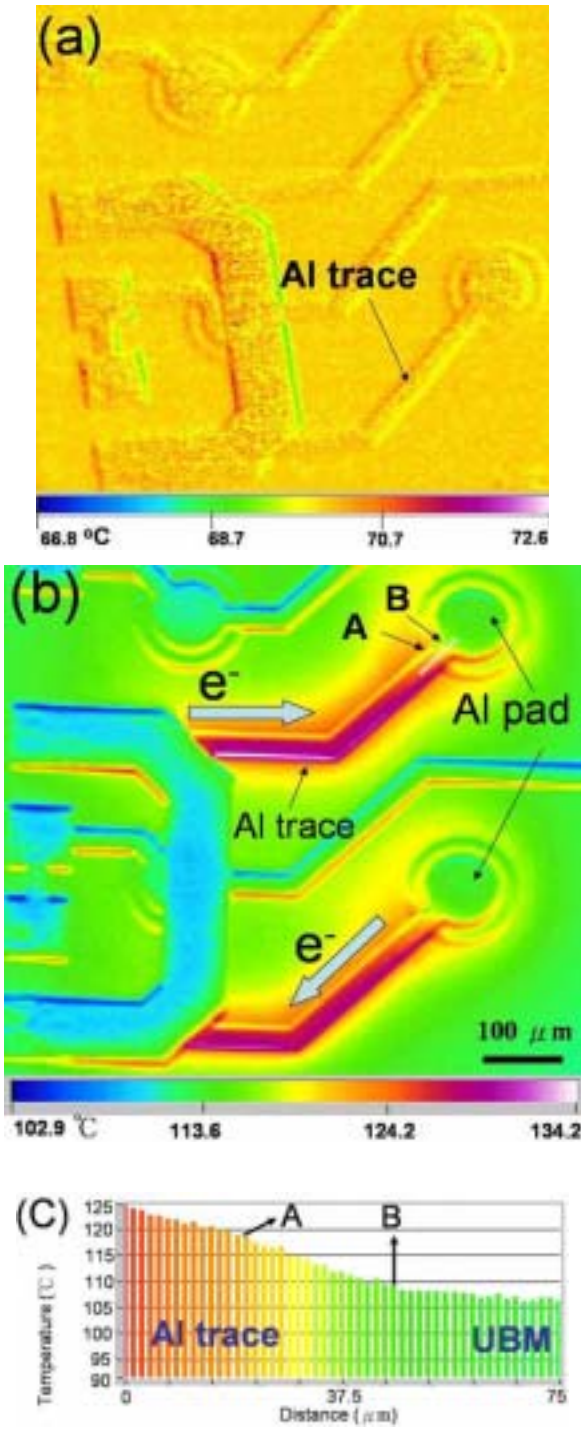
結果與討論

銲錫之電熱效應研究

通電前，IR 先在 70 度作溫度的校正，由圖十四(a)可以看到穿透矽晶片的鋁導線溫度分佈相當的均勻，並且鋁導線的線路外觀可以很清楚的呈現。對整個覆晶結構在 70 度底下施予 0.59 安培的電流，如圖十四(b)所示，電流方向就如圖中箭頭所指示，鋁導線與鋁 Pad 可以很清楚的觀察到，兩顆銲錫凸塊位於圖中鋁 Pad 的正下方，所以由 IR 的結果顯示鋁導線在通電過程中會比鋁 Pad 有比較高的溫昇，因爲整個銲錫金屬是熱的良導體並且幫助導線將熱傳導出去；圖中最高溫發生在鋁導線的中央約 134 度，而鋁 Pad 由於銲錫在下方的關係只有約 105 度。圖中鋁 Pad 內圈是 passivation opening，外圈則是 UBM opening。我們在鋁 Pad 附近取一條長度爲 75um 的虛線，此虛線會通過鋁導線與鋁 Pad ，並在 passivation opening 和 UBM opening 的邊界標記 A、B。圖十四(c)爲 75m 虛線的溫度分佈曲線，並且

觀察到 passivation opening 和 UBM opening 的邊界 A、B 溫度分別爲 118.2 ℃與 109.7 ℃。值得一提的是我們取整個鋁 Pad 內圈 passivation opening 的平均溫度只有 105.2 ℃，單只有在水平端鋁導線與 UBM 的接口處到鋁 Pad 另一端就有 1700℃/cm 的溫度梯度，這是一個相當嚴重的影響。

而在通電的過程中，銲錫內部的溫度一直是我們所感興趣的，本研究更建立 3D 的電腦模擬結果，並發現到在通電過程中，在鋁導線與銲錫接點入口處會有一熱點(hot spot)產生，在後續會有完整的銲錫接點內部的電與熱系統的分析。



圖十四、(a)通電前，溫度校正示意圖，(b)0.59 A/100℃之 IR 溫度分佈圖 (c)在圖(b)虛線之溫度曲線。

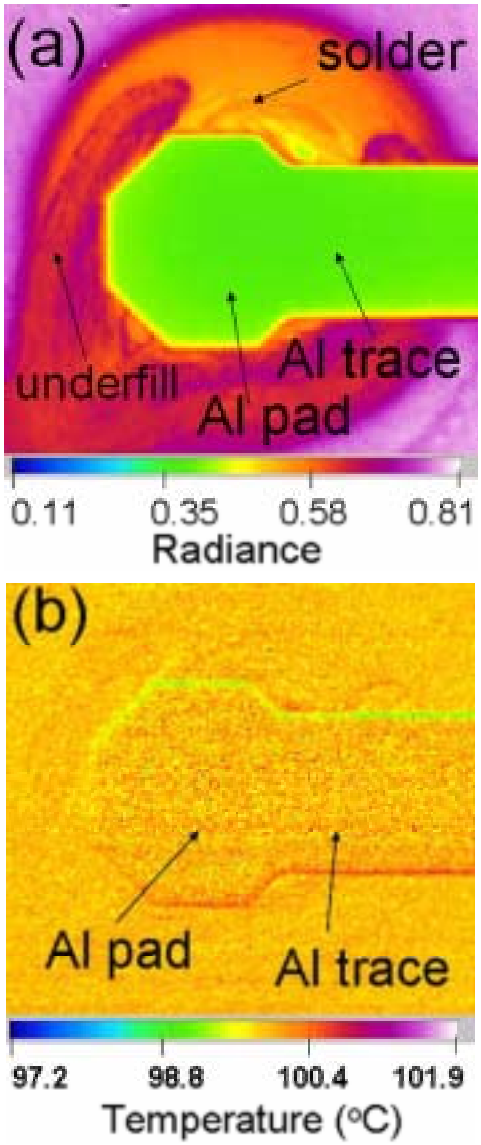
鋁導線尺寸對於電遷移現象之研究

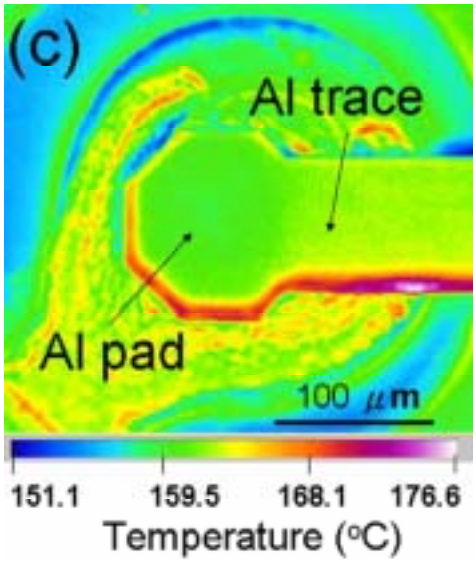
鋁導線寬度的影響

通電前，IR 先在 100 度作溫度的校正，由圖十五 (a)可以看到穿透矽晶片的鋁導線的線路

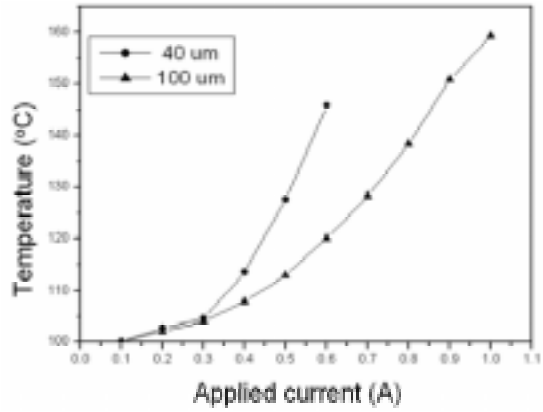
外觀可以很清楚的呈現。如圖十五 (b)所示，通電前，看到穿透矽晶片的鋁導線溫度分佈相當的均勻，鋁導線與鋁 Pad 可以很清楚的觀察到，對整個覆晶結構在 100 度底下施予 0.6 安培的電流，如圖十五 (c)所示，及可觀察到試片在通電後之溫度分佈。

我們對於圖五、六這兩種結構施予 100 度 0.6 安培的電流，通電後結果顯示，寬度爲 40 的鋁導線在一瞬間和錫接點就遭到破壞，然而寬度爲 100 的鋁導線則在 18 個小時後才破壞。爲了要探討這個破壞時間不同的原因，我們利用 IR 來量測鋁導線 Pad 上 40μm x 40μm 的溫度，由圖十六 結果顯示，40μm 線寬的鋁導線結構相對於 100μm 寬度的結構會有比較高的溫昇，相對的焦耳熱效應也比較嚴重。





圖十五、(a)通電前，圖五之 B1 輻射校正示意圖，(b) 通電前，圖五之 B1 溫度校正示意圖 (c) 0.8 A/100℃之 IR 溫度分佈圖。



圖十六、寬度 40μm 與 100μm 之鋁導線電遷移破壞時間(daisy-chain)。

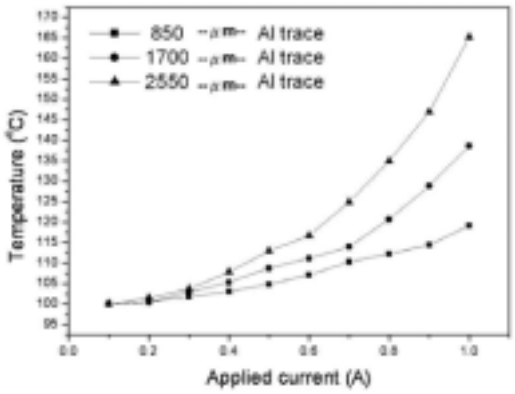
鋁導線長度的影響

我們對於圖七結構進行鋁導線長度效應影響的分析，通電模式分別爲(1).電流流經 3 段導線 4 顆銲錫凸塊(B1+T1+B2+T2+B3+T3+B4). (2) 電流流經 2 段導線 3 顆銲錫凸塊 (B1+T1+B2+T2+B3). (3) 電流流經 1 段導線 2 顆銲錫凸塊(B1+T1+B2).對於這 3 種模式施予 100 度 1 安培的電流，電流密度爲 7.1×10^3 A/cm^2。結果顯示電流通過 3 段導線的破壞時間爲 35 小時、電流通過 2 段導線的破壞時間爲 1700 小時、電流通過 1 段導線的破壞時間爲超過 3000 小時。由此結果可以知道鋁導線長度影響破壞時間甚鉅，由於這 3 種不同長度的鋁導線結構之電流密度皆相同，之所以會造成破壞時間有如此大的差異因素在於焦耳熱效應。經由IR的結果顯示，如圖十七所示，在通電的過程當中，這 3 種不同長度的鋁導線溫昇分別爲 65.1 ℃、38.6 ℃、19.1 ℃，而這溫昇的差異就是造成破壞時間有這麼大不同的主要原因。

在焦耳熱效應的公式中:

$$P = I^2 R$$

P 爲 Joule heating power， I 是電流， R 是電阻。在 3 段鋁導線長度通電的過程中，總電阻爲 1210 mΩ，鋁導線電阻佔整個迴路的 81%，銲錫凸塊只有 5 mΩ，其餘的電阻是有基板端的銅導線所提供，由此可得知鋁導線是在通電過程中最主要的發熱源。

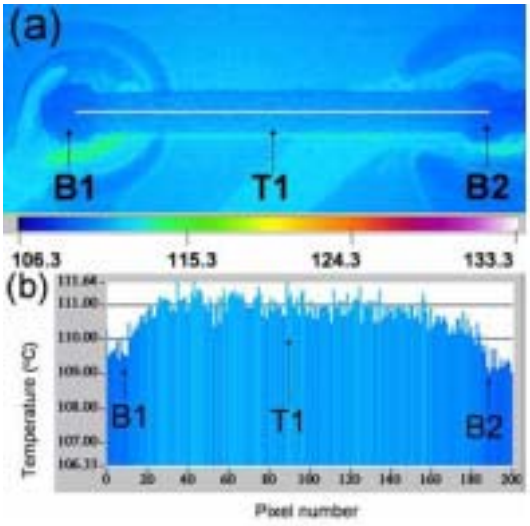


圖十七、3 段不同鋁導線長度 850-μm、1700-μm、2550-μm，電流與溫度之關係圖。

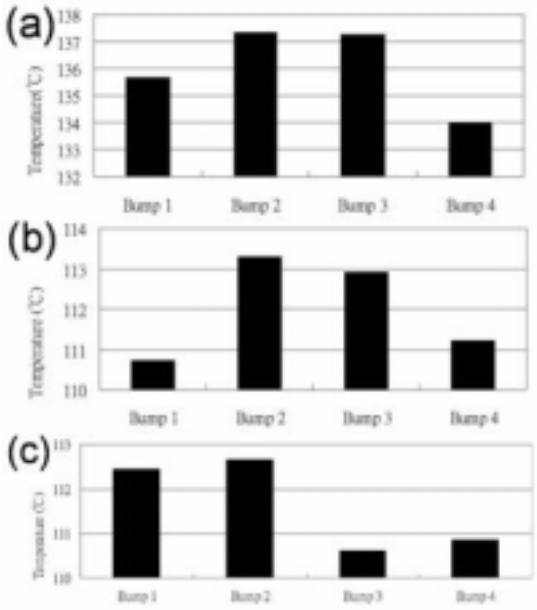
熱遷移現象之研究

我們在對於電遷移效應中熱遷移現象來做討論，我們對圖七的結構在 100 度下施予 0.8 安培的電流，電流只流經 B1、B2 與一條導線。由圖十八結果顯示，鋁導線中央(111.5 ℃)由於散熱比較不易，相對的會比兩端(109.7 ℃) 有較高的溫昇，並且兩顆銲錫凸塊位於圖中鋁 Pad 的正下方，可能也是造成此現象的另一個因素。

我們再這一組通電參數中發現一個有趣的現象，在通電的過程當中，沒有電流流經的鄰近位置也會有產生溫度上升的現象，如圖十九(a)所示，電流流經 B1~B4 與 3 段鋁導線，中間的 2 顆銲錫凸塊會比 2 兩端有比較高一點的溫昇，並且只有 2.7 度左右的溫差。當施予相同的電流 0.8 安培，電流流經 B2、B3 與一條鋁導線，如圖十九(b)所示，B2、B3 的溫度約爲 113.0 °C，有趣的是，旁邊沒有電流通過的 B1、B4，竟然也量測到 111.0 °C 的溫度。這現象使我們得知鄰近位置即使沒有電流經過，還是一樣會有溫昇的現象產生。圖十九(c)電流流經 B1、B2 與一條鋁導線，B1、B2 溫度爲 112.5 °C，旁邊沒有電流通過的 B3、B4，相同的也量測到 110.7 °C 的溫度。



圖十八、(a) 電流流經 B1、B2，0.8 安培之 IR 溫度分佈圖 (b) 圖(a)白線之溫度分佈圖。

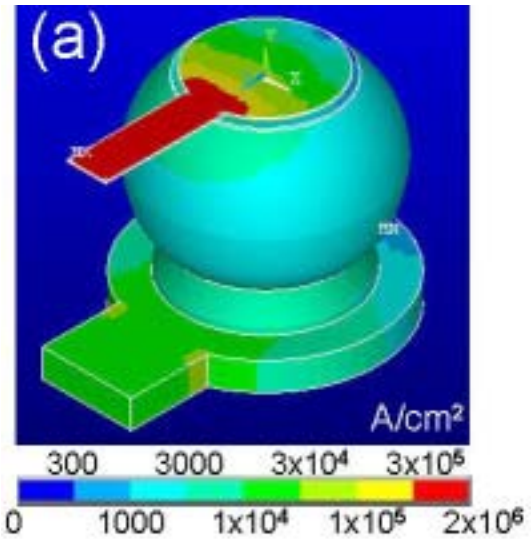


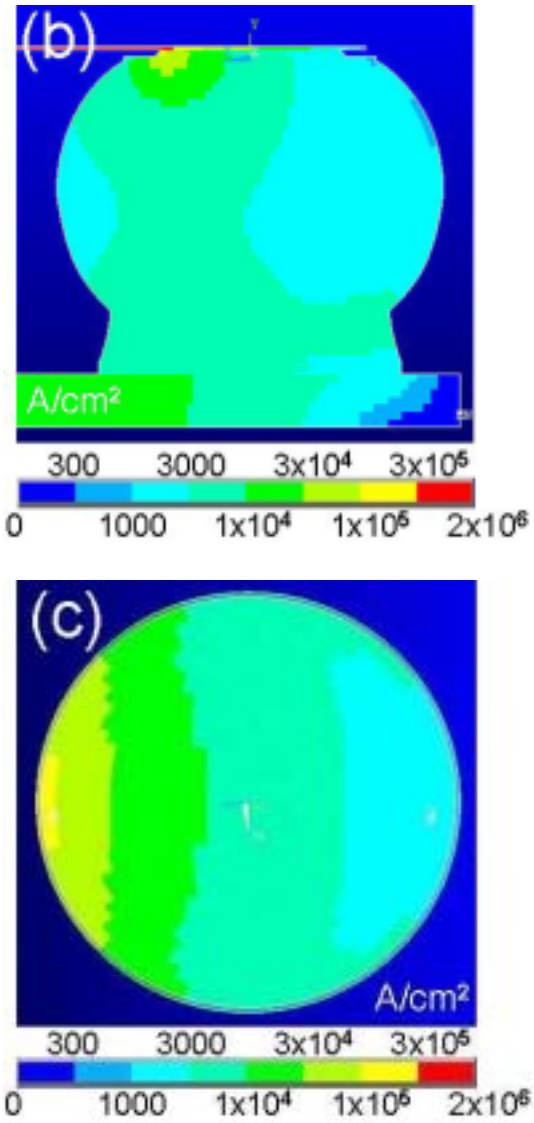
圖十九、電流(0.8 A)、流經不同長度鋁導線之鋁 Pad 溫度 (a)電流流經 B1 到 B4(b) 電流流經 B2 到(c) 電流流經 B1 到 B2。

電流密度結果分析

I. 標準模型

單一顆覆晶銲錫接點的電流密度分布圖如圖二十三(a)，電流條件是 0.567 安培，所對應的平均電流密度是 5000 安培/平方公分。可以發現圖二十三(a)中的紅色部分是高電流密度區，分布在鋁導線，其平均值約爲 1.11×10^6安培/平方公分。爲了方便比較電流集中效應，將其效應的程度量化，因此我們定義"聚集率"(crowding ratio)爲銲錫內部的電流密度最大值除以平均電流密度。所以當集中率值越大時，就表示電流分布的不均勻，方便做比較分析。由圖二十三(a)(b)，我們可以發現電流集中效應發生在鋁導線的入口處。取標準模型中，銲錫靠近鋁導線入口處的電流密度最大值爲 1.11×10^5安培/平方公分，其對應的聚集率爲 22.2。接下來藉由改變結構或是材料性質來觀察其改變對減緩電流集中效應的效果。

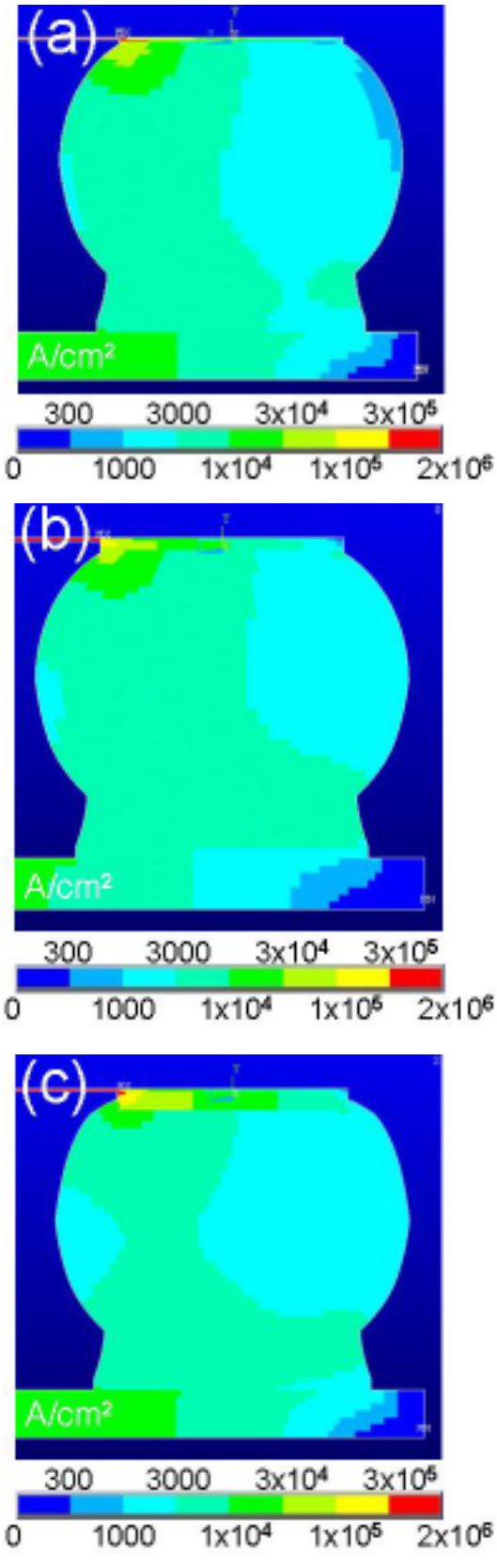


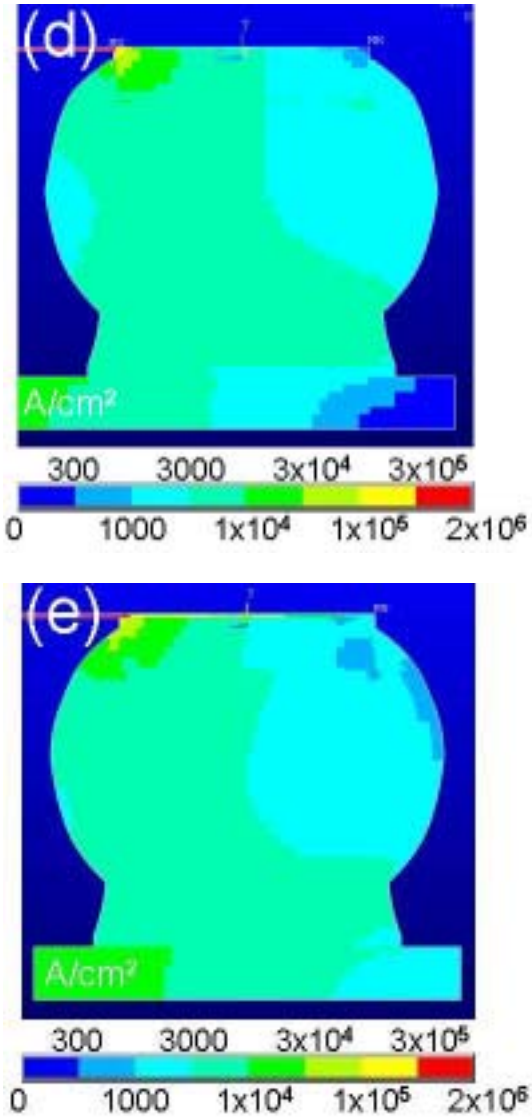


圖二十三、(a)標準模型的三度空間電流密度分布圖;(b)沿鋁導線取橫截面之電流密度分布圖;(c)銲錫接點最頂端之電流密度分布圖。

III.改變底部金屬層厚度

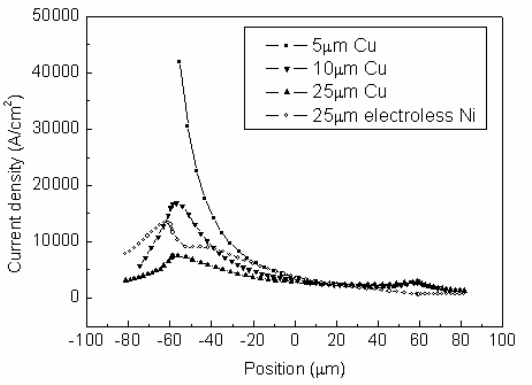
爲了比較出底部金屬層厚度的關係，我們採用了不同厚度的底部金屬層來模擬，包刮 0.5-μm Cu、5-μm Cu、10-μm Cu、20-μm Cu以及 20-μm electroless Ni，分別依次由圖二十五(a)到(e)。從圖八的結果我們可以發現嚴重的電流集中效應依然都發生在鋁導線進到銲錫的入口處。但是厚度較後的底部金屬層結構可以有效的使銲錫的部份遠離電流集中效應，定使其在電遷移的條件下有均勻的電流密度分布。各別對應的電流密度最大值分別爲：1.17×10^5、1.69×10^4、4.37×10^4、7.54×10^3、與 1.34×10^4安培/平方公分，對應到的叢集率爲：23.4、8.7、3.4、1.5 與 2.7。結果我們可以發現底部金屬層的厚度越厚，銲錫裡面的電流密度最大值越小，增加底部金屬層厚度而減緩電流密度最大值其原因在於使電流集中的現象遠離銲錫接點，因爲底部金屬層有良好的抗電遷移性質。


(a)
A/cm²
300
3000
3x10⁴
3x10⁵
0
1000
1x10⁴
1x10⁵
2x10⁶
(b)
A/cm²
300
3000
3x10⁴
3x10⁵
0
1000
1x10⁴
1x10⁵
2x10⁶
(c)
A/cm²
300
3000
3x10⁴
3x10⁵
0
1000
1x10⁴
1x10⁵
2x10⁶

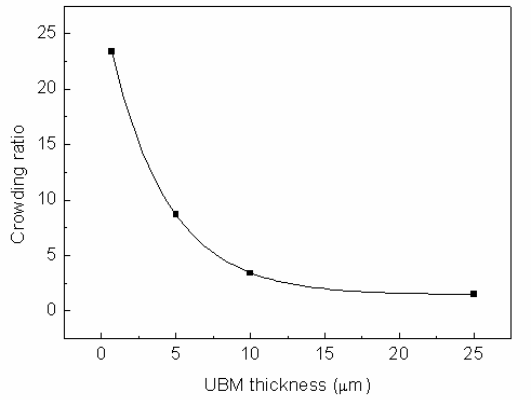


圖二十五、(a)底部金屬層改爲 0.7-μm Cu 時，沿鋁導線取橫截面之電流密度分布圖;(b)底部金屬層改爲 5-μm Cu 時，沿鋁導線取橫截面之電流密度分布圖; (c) 底部金屬層改爲 10-μm Cu 時，沿鋁導線取橫截面之電流密度分布圖;(d) 底部金屬層改爲 20-μm Cu 時，沿鋁導線取橫截面之電流密度分布圖;(e) 底部金屬層改爲 20-μm electroless Ni 時，沿鋁導線取橫截面之電流密度分布圖。

當我們取出銲錫最上端沿鋁導線位置的電流密度值對相對位置座標作圖，如圖二十六，我們可以發現電流密度最大值明顯下降，因爲底部金屬層的厚度效應，而最大值的位置約略在-55μm 處，此即爲鋁導線入口的位置。另外我們也可以發現一樣厚度的時候無電鍍鎳效果不如銅要來的好，主要是來自於低電阻率的 Cu 可以更有效的分散電流。而電流密度對底部金屬層的關係圖中(圖二十七)，我們可以發現其關係約爲指數下降。



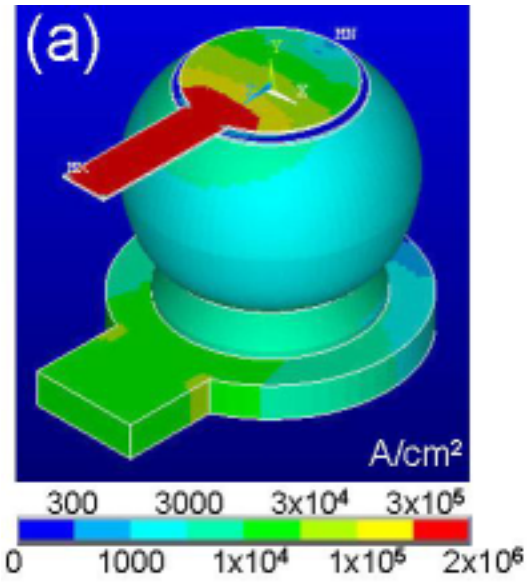
圖二十六、不同底部金屬層厚度之電流密度沿鋁導線對應座標分布圖。

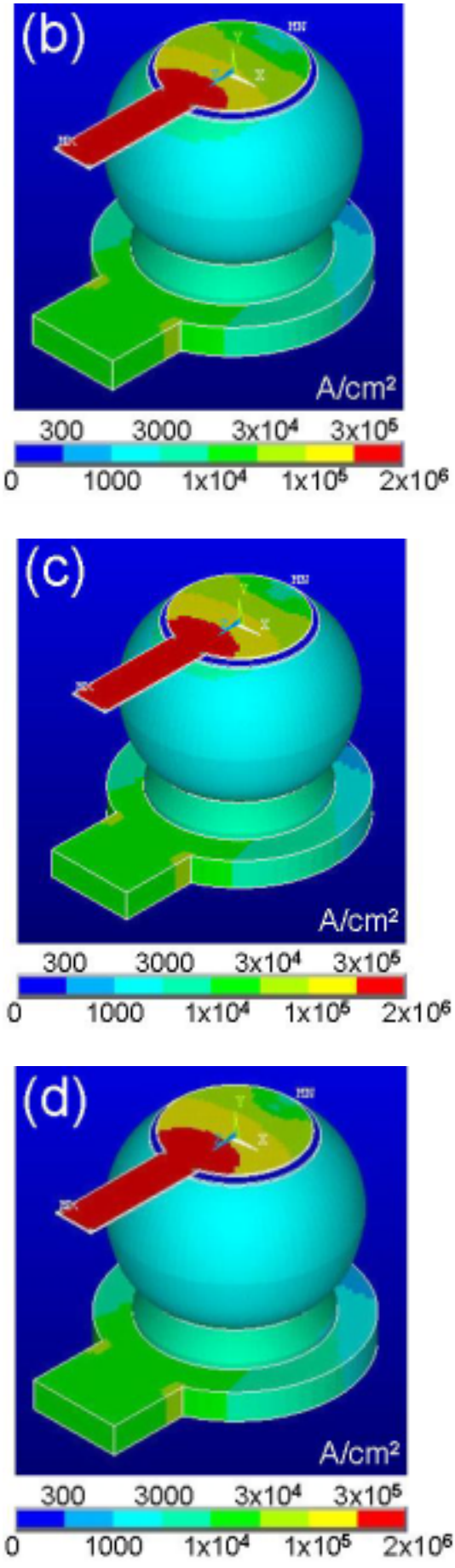


圖二十七、叢集率對底部金屬層銅厚度關係圖。

IV.改變底部金屬層電阻率

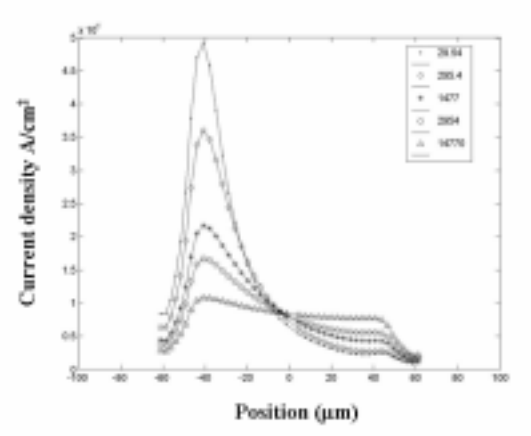
爲了探討底部金屬層電阻率的效應，我們選用了以標準模型中底部金屬層的10倍、50倍、100倍與500倍來作比較。其對應的電阻率分別爲：295、1477、2954與14770 μΩ-cm，從圖二十八可以看出來兩個趨勢，第一：鋁導線部份紅色的大電流區往鋁金屬盤延伸，表示電流路徑因爲底下大電阻的底部金屬層而改變，因爲電流無法順利直接流穿過底部金屬層，所以在鋁金屬盤流經足夠路徑後才均勻的往銲錫接點分散；第二：銲錫接點部份原本的電流密部分布由1000到10000安培/平方公分，再大電阻率的底部金屬層的改善下，電流密部分布下降至由1000到3000安培/平方公分。





圖二十八、(a)電阻率改爲 295 μΩ-cm 的三度空間電流密度分布圖;(b)電阻率改爲 1477 μΩ-cm 的三度空間電流密度分布圖;(c)電阻率改爲 2954 μΩ-cm 的三度空間電流密度分布圖;(d) 電阻率改爲 14770 μΩ-cm 的三度空間電流密度分布圖。

當我們一樣取出銲錫最上端沿鋁導線位置的電流密度值對相對位置座標作圖，如圖二十九，我們可以發現電流密度分佈明顯變的均勻，可以再次說明電流路徑因爲底下大電阻的底部金屬層而改變，因爲電流無法順利直接流穿過底部金屬層，所以在鋁金屬盤流經足夠路徑後才均勻的往銲錫接點分散。

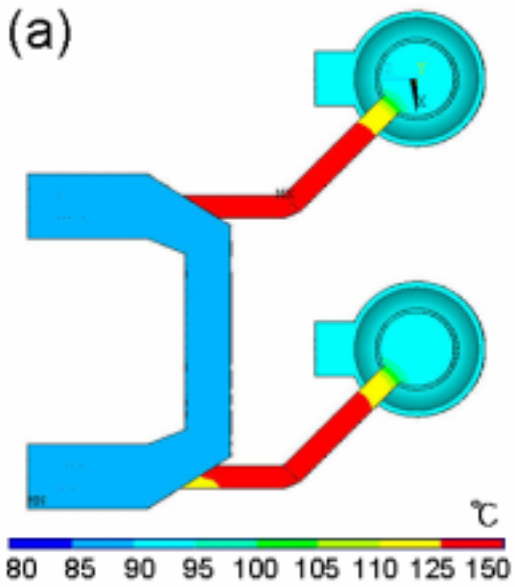


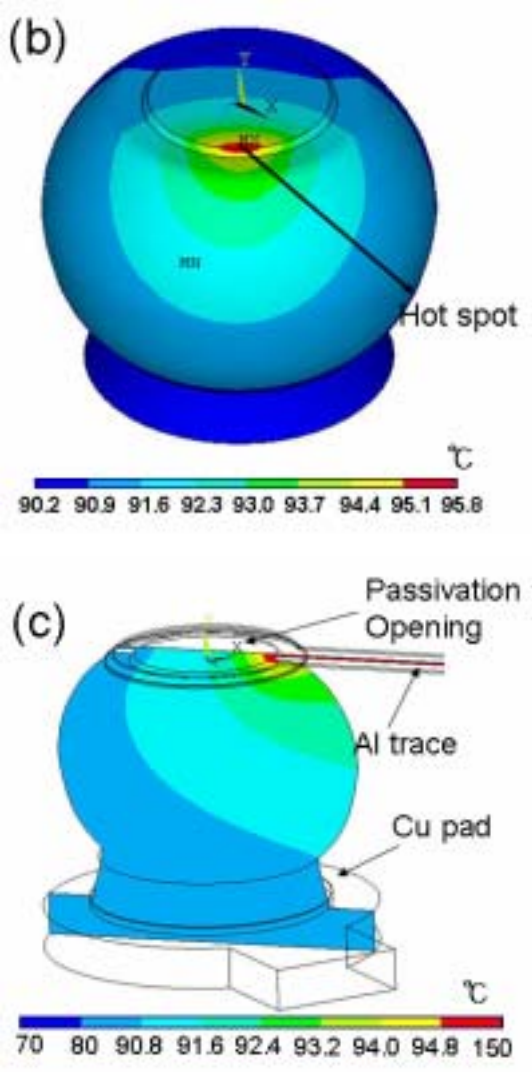
圖二十九、不同底部金屬層厚度之電流密度沿鋁導線對應座標分布圖。

溫度分布結果分析

I..標準模型

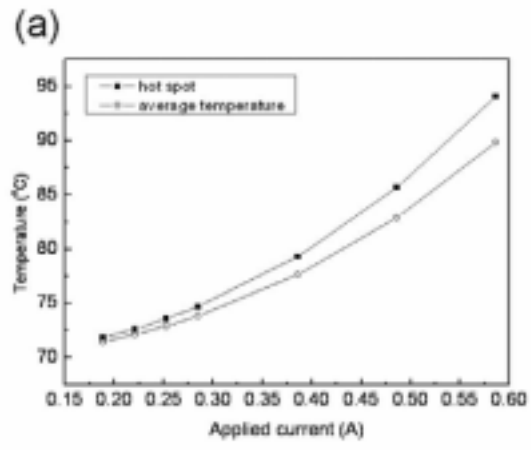
由於有紅外線熱像儀可以分析銲錫上方鋁導線的溫度分布情形，因此，我們採用實驗對照模擬的方式來修正我們的熱邊界條件，最後我們以BT基板爲等溫面 70°C，試片周圍與室溫(25°C)對流，對流係數爲 10W/cm^2-K，電流條件爲 0.15 安培到 0.6 安培。在此條件下，我們可以得到實驗與模擬最接近的結果。圖三十(a)，首先我們就可以看到鋁導線是主要的發熱源，因爲鋁導線是薄膜結構，有相當大的電阻，也就對應到公式：$P=I^2R=j^2$ V，所以會產生很大的發熱量，所以系統的最高溫發生在鋁導線，熱由發熱的鋁導線往矽晶片與銲錫散熱，使得銲錫內部會產生一個熱點，可以由圖三十(a)(b)觀察到，熱點溫度爲 95.6°C，比銲錫接點平均溫度高約 4.5°C，因爲有溫度高低溫的不同衍生出溫度梯度的問題，近來發現溫度梯度會導致熱遷移的行爲使得接點加速破壞，因此我們將會討論溫度梯度與電流之關係。

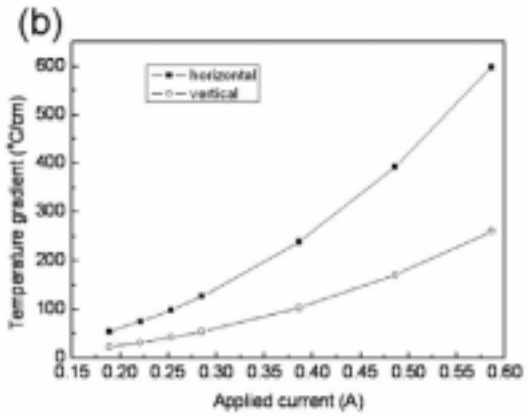




圖三十、在基板 70°C，0.6 安培下: (a)兩顆實際迴路銲錫接點之溫度分布;(b)單取一顆銲錫接點之溫度分布圖;(c)銲錫接點沿鋁導線取橫截面之溫度分布圖。

我們可以從圖三十發現，雖著電流越大，溫度也隨之上升，而熱點與平均溫度也越差越多，在 0.6 安培差到 4.5°C。也因此溫度梯度，無論是水平向或是垂直向，也都是電流越大梯度越大的趨勢，可以顯現越高電流時，因爲鋁導線發熱越嚴重，並且因爲電流集中效應，不均勻的電流分布造成銲錫接點溫度也分布不均。爾後將會設法改善熱電效應，使銲點壽命提升，當然就得從減緩電流集中效應與減少發熱著手。

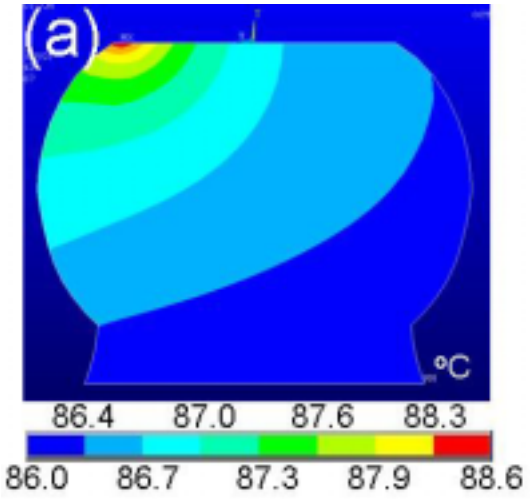


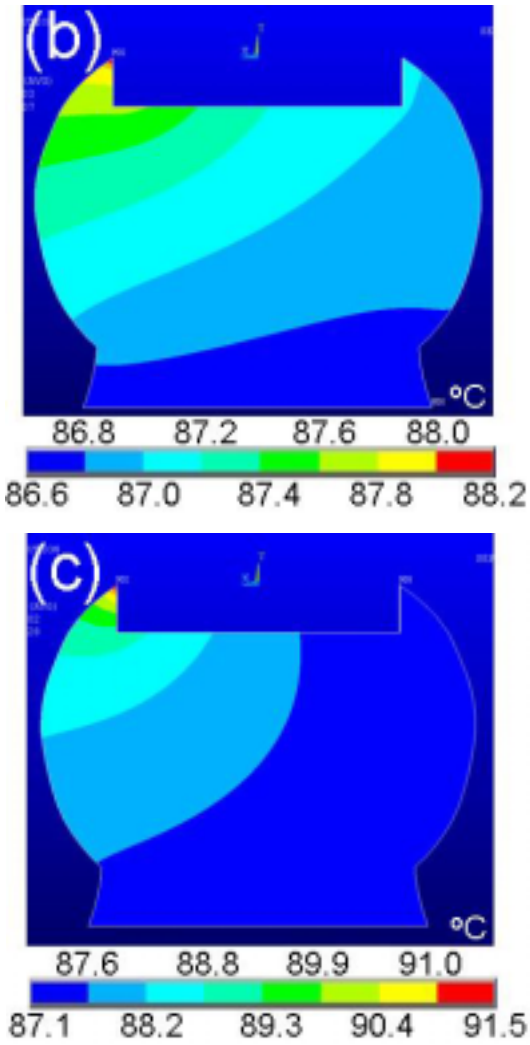


圖三十、(a)銲錫接點熱點與平均溫度隨電流大小之關係圖;(b)銲錫接點水平方向熱梯度與垂直方向熱梯度隨電流大小之關係圖。

II.改變底部金屬層厚度

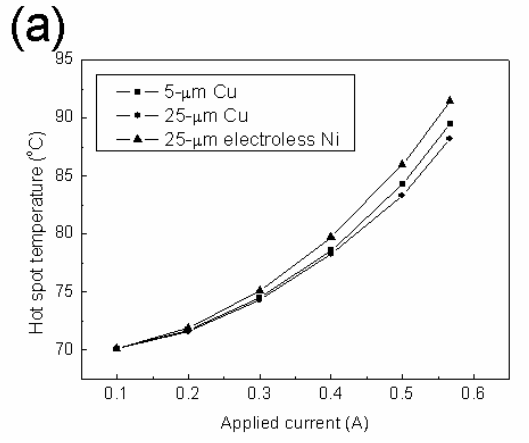
5-μm Cu，在基板 70°C與電流 0.6 安培下的條件下，溫度分布情形如圖三十一(a)，其熱點溫度爲 89.5°C，平均溫度爲 87.3°C，差 2.3°C。計算一下溫度梯度約爲 157.4°C/公分。而改成 25-μm Cu，在基板 70°C與電流 0.6 安培下的條件下，溫度分布情形如圖三十一(b)，其熱點溫度爲 88.2°C，平均溫度爲 87.0°C，對應溫度梯度約爲 105.8°C/公分，減低銲錫接點溫度的效果是最好的。若是換成 25-μm 無電鍍鎳，在基板 70°C與電流 0.6 安培下的條件下，溫度分布情形如圖三十一(c)，其熱點溫度爲 91.5°C，平均溫度爲 87.6°C，對應溫度梯度約爲 290°C/公分，即是厚度比銅 5μm厚上許多，可是因爲電阻率很差，熱傳也很差的緣故，所以沒有達到很好降低操作溫度的效果。

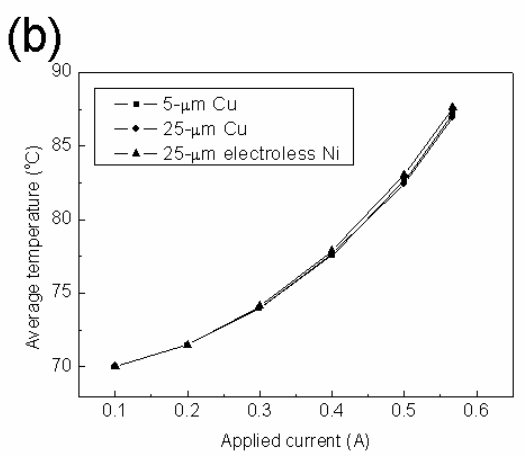




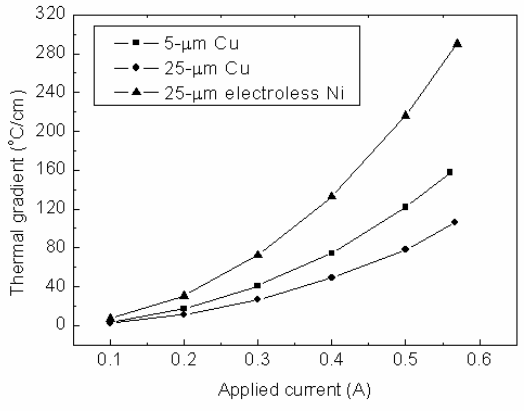
圖三十一、在基板 70°C，0.6 安培下: (a)底部金屬層改爲 5μm Cu時，沿鋁導線取橫截面之溫度圖;(b)底部金屬層改爲 20-μm Cu時，沿鋁導線取橫截面之溫度分布圖;　(c)底部金屬層改爲 20-μm electroless Ni時，沿鋁導線取橫截面之溫度分布圖。

圖三十二與圖三十三，代表溫度與電流的三個關係。首先熱點溫度，因爲鋁導線是主要發熱源，雖然我們使用了厚膜結構，但對於減緩溫度的效果仍然有限，甚至平均溫度其實都差不了多少。但是溫度梯度卻會差異很大，主要還是因爲無電鍍鎳的熱傳效果不好，導致溫度差異很大，有較大的溫度梯度。





圖三十二、(a)不同底部金屬厚度與材質，銲錫中熱點與電流之關係圖;(b) 不同底部金屬厚度與材質，銲錫中平均溫度與電流之關係圖。



圖三十三、不同底部金屬厚度與材質，銲錫中熱梯度與電流之關係圖

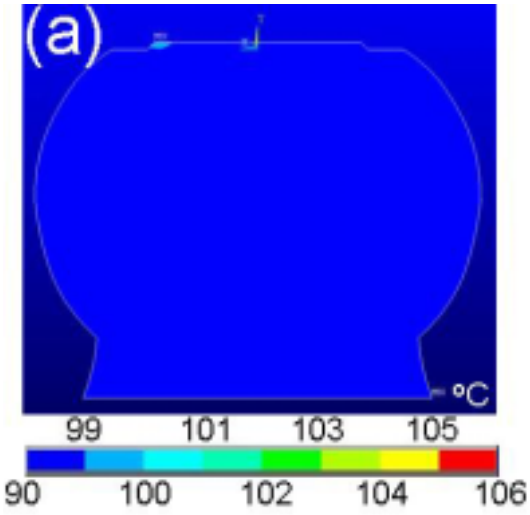
通常大家會利用 Black's 方程式來計算電子產品的使用壽命，其方程式如下：

$$MTTF = A\frac{1}{j^n}\exp\left(\frac{Q}{kT}\right)$$

其中 A 是常數，j 電流密度，n 電流密度的指數，Q 爲活化能，k 視波茲曼常數，而 T 爲絕對溫度。藉由此公式，我們可以發現到經由改變底部金屬層的厚度應該可以有效的提昇銲點壽命，因爲增加底部金屬層厚度不僅使銲點裡的最大電流密度減緩，也使得操作溫度降低，因爲 Cu 良好的電性與熱傳。

III.改變底部金屬層電阻率

先前提到另一個減緩電流集中效應的方法就是改變底部金屬層的電阻率，也由於銲點壽命與溫度跟電流密度息息相關。爲了以防提高薄膜電阻率造成很大升溫，藉此我們就來看其溫度影響，我們可以發現除非電阻率提高很多，否則其實對溫度的增加是沒有很大的差別，在 0.6 安培的時候，與標準模型只差約 6.7^{o}C，然而一般操作條件僅在 0.2 安培，對升溫影響更小。


(a)
°C
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101
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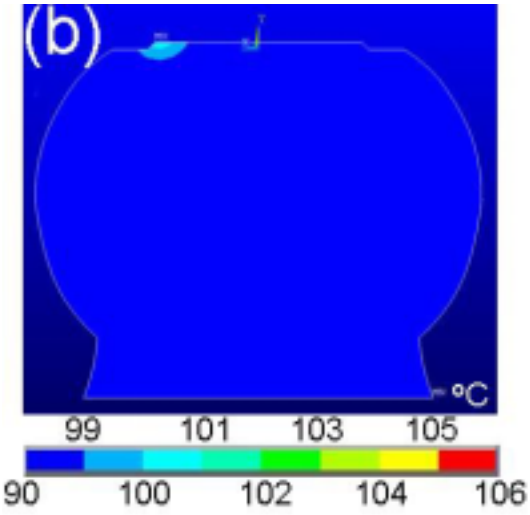
104
106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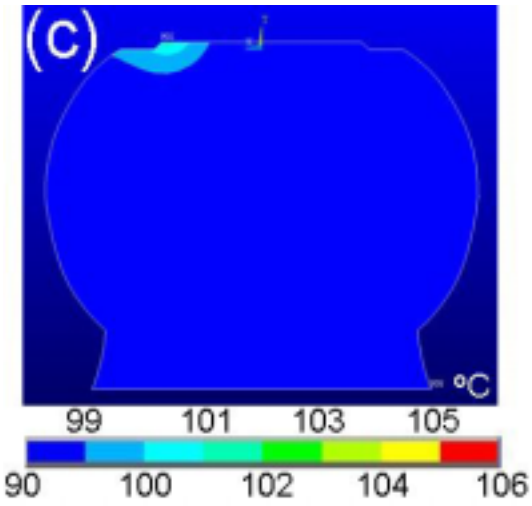
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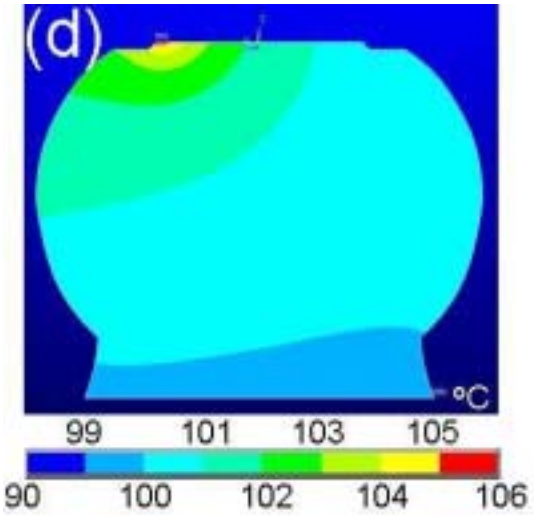
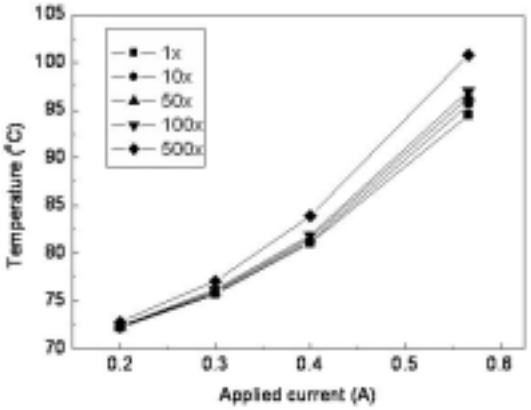


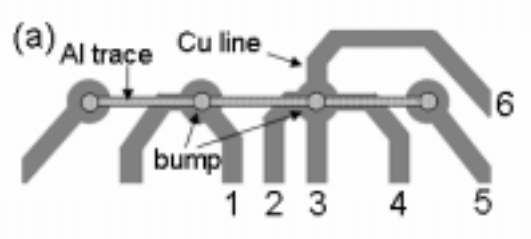
圖三十四、在基板 70°C，0.6 安培下:(a)電阻率改爲 295 μΩ-cm的三度空間電流密度分布圖;(b)電阻率改爲 1477 μΩ-cm的三度空間電流密度分布圖;(c)電阻率改爲 2954 μΩ-cm的三度空間電流密度分布圖;(d) 電阻率改爲 14770 μΩ-cm的三度空間電流密度分布圖。

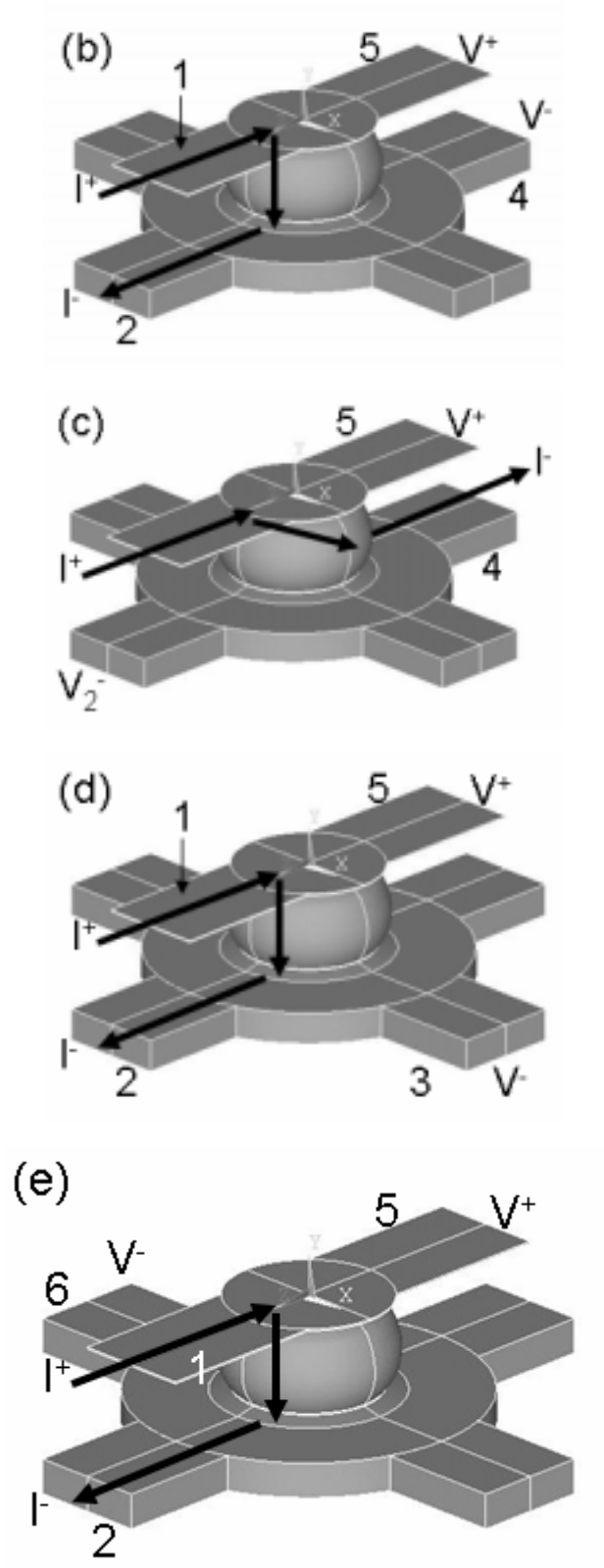


圖三十五、不同底部金屬電阻率度與材質，銲錫中熱點與電流之關係圖。

銲錫接點量測電阻之幾何效應

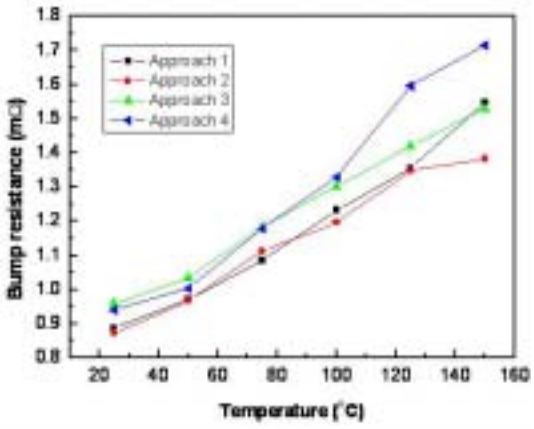
爲了觀察銲錫接點在量測電阻時的幾何效應，特地採用一種線路，如圖三十六(a)所示。上面有四顆銲錫接點，外接數個線路，其中量測的六個線路標註在圖上以便說明量測方式。第一個方法(圖三十六(b))，電流經由 1 號與 2 號線路，量測 4 號與 5 號的電位差，再計算出電阻。方法二(圖十九(c))，電流經由 1 號與 4 號線路，量測 2 號與 5 號的電位差，再計算出電阻。方法三(圖三十六(d))，電流經由 1 號與 2 號線路，量測 3 號與 5 號的電位差，再計算出電阻。第四個方法(圖三十六(e))，電流經由 1 號與 2 號線路，量測 5 號與 6 號的電位差，再計算出電阻。





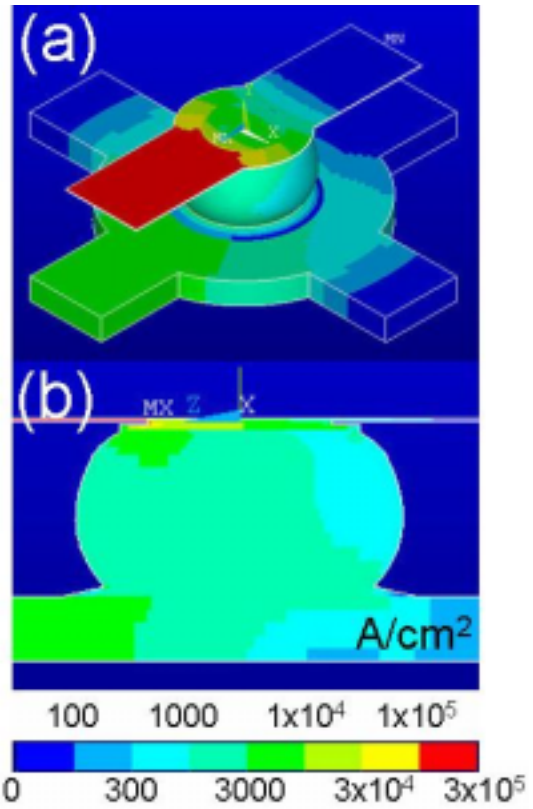
圖三十六、(a)線路的平面示意圖;銲錫與線路的立體圖，配合量測路徑表示圖:(b)方法一;(c)方法二; (d)方法三; (e)方法四。

量測是利用電源供應器Keithley 2400，施加 0.2 安培，隨著加熱板供給基板不同溫度，從 25^{o}C到 150^{o}C，量測四種方式，其結果如下圖三十七，可以發現其電阻隨溫度上升的關係相當良好，四個不同方式的電阻隨溫度上升的係數爲：5.1×10^{-3}、4.4×10^{-3}、4.3×10^{-3}、4.9×10^{-3} K^{-1}，因爲我們量測到的是數種金屬的總和，所以其結果是相當接近預期。當在室溫的時候，方法一量測到的電阻爲 0.89 m　，接下來依序爲 0.87、0.96 與 0.94 m



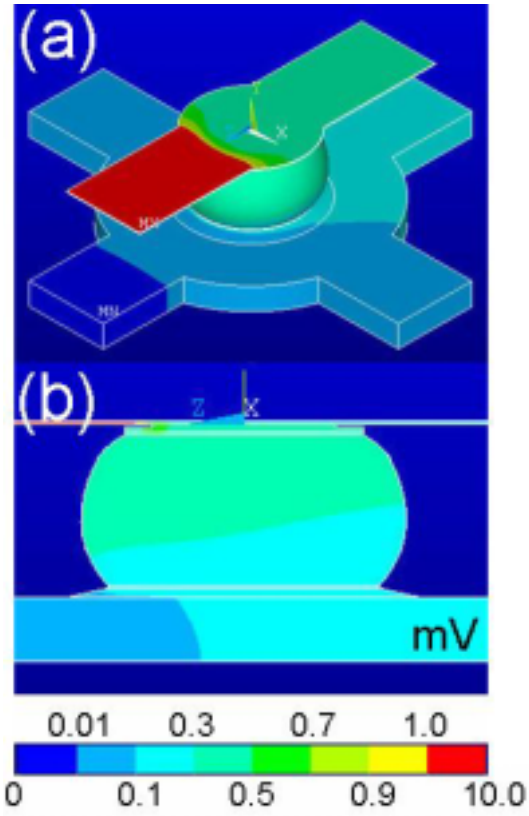
圖三十七、電阻爲溫度的關係圖。

誠如之前提出的，由於覆晶銲錫是一個線到凸塊(line-to-bump)的結構，因此在銲錫內部靠近鋁導線的入口會有電流集中效應，，因此電流密度的不均勻分布一定會影響電位與電阻的關係。圖三十八，即爲當電流爲 0.2 安培時的電流密度分布，配合我們量測結果作後續分析。



圖三十八、(a)單一顆銲錫的電流密度分佈;(b)沿鋁導線取橫截面之電流密度分佈圖。

將電流密度分布轉換爲電位分布情形，圖三十九(a)，可以發現電位變化都發生在鋁導線的部份，而且從圖三十九(b)的橫截面電位分布可以發現左邊的電位差是右邊的 9 倍，這樣會造成量測上的差異，也就是不同位置的量測點會有不同的電位差值，得到不同的電阻值。依照根實驗量測一樣的方法，取出模擬的電阻值，各別爲 0.77、0.76、0.83 與 0.83 mΩ。整理成表二。結果發現，實驗量測都比模擬結果高，高約 12 至 14%，主要是因爲模擬採用的電阻率是在 20^{o}C，而實驗量測溫度是在 25 到 30^{o}C，可見模擬結果很符合實驗量測，從電阻的幾何效應可以反推電流集中效應。

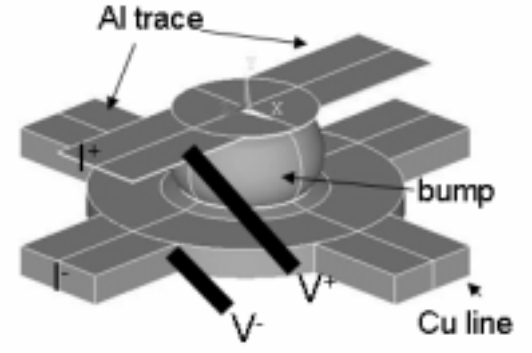


圖三十九、(a)單一顆銲錫的電位分佈圖;(b)沿鋁導線取橫截面之電位分佈圖。

Approach (node-node)	Experimental (mΩ)	Simulation (mΩ)
1 (4-5)	0.89	0.77
2 (2-5)	0.87	0.76
3 (3-5)	0.96	0.83
4 (5-6)	0.94	0.83

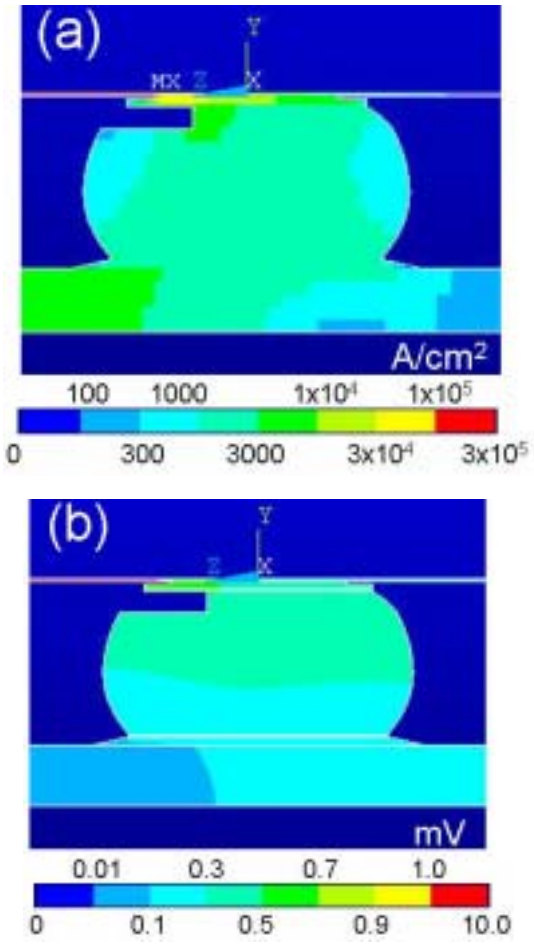
表二、實驗與模擬電阻之比較表。

然而實際電阻值量測位置應該改爲電流進到銲錫的導線前端一段距離，見圖四十，此時定義其爲方法五，從模擬得到這各電阻值爲 7.7 mΩ，如果理論計算此結構的電阻約爲 1.0 mΩ，可見因爲電流路徑與電流集中效應影響之下，操作電阻爲均勻分布電流下電阻的 7.7 倍。



圖四十、新結構以供量測銲錫接點電阻之示意圖。

而當銲錫接點因爲電遷移產生空孔時，其影響電流密度與電位的結果如圖四十一。當產生一個佔據底部金屬層開口 18%的空孔時，方法一到四電阻上升 0.12mΩ，上升率約爲 15%，可是方法五雖然上升 0.5mΩ，可是其上升率只有 6.5%。見表三。所以說如果我們想偵測因爲電遷移產生空孔而造成電阻上升，方法一到四都是一個不錯的方式。



圖四十一、(a)當銲錫接點產生佔據底部金屬層開口 18%時的電流密度橫截面分佈圖;(b) 當銲錫接點產生佔據底部金屬層開口 18%時的電位橫截面分佈圖。

Approach (node-node)	R0 (mΩ)	R1 (mΩ)	R/R0 (%)
1 (4-5)	0.77	0.89	15.6
2 (2-6)	0.76	0.88	15.7
3 (3-5)	0.83	0.95	14.5
4 (5-6)	0.83	0.95	14.5
5 (1-2)	7.7	8.2	6.5

表三、電阻隨空孔發生而上升之結果表。

結論

本年度主要之結果如下:我們可以利用 IR 與 3-D 電腦模擬來分析出覆晶結構之焦耳熱效應，並且發現在鋁導線與 UBM 入口再通電的過程中會有一個熱點(hot spot)產生，並且會隨著外加電流的提高而有更高的溫昇，更探討不同結構對於銲錫接點的電熱效應之影響。本研究更利用凱文銲錫結構（Kelvin bump probes）來觀測與測量覆晶銲錫球受電遷移時孔洞遷移與成長的現象，研究銲錫受電遷移影響而產生的破壞。鋁導線的尺寸影響電遷移的破壞時間甚鉅，研究結果顯示，在相同的通電參數之下，越寬與越短的鋁導線設計可以延長銲錫結構之電遷移破壞時間。在釐清各種銲錫之破壞機制後，未來研究之重點將著重在如何有效抑制電遷移所造成之破壞。

本研究群的相關研究結果，於 94 年發表於 Applied Physics Letter 期刊論文四篇、journal of material research 一篇、Journal of Electronic Materials、國際會議論文三篇。

6、參考文獻

1. H. B. Huntington, J. Phys. Chem. Solid, 20, p76-87, 1961.
2. J. R. Black, IEEE Trans Electron Device, ED-16, p338, 1969.
3. I. A. Blech, J. Appl. Phys. 40（2）, p485, 1969.
4. K. N. Tu, “Electromigration in stressed thin films,” Phys. Rev. B45, 1409 (1992).
5. K. N. Tu, C. C. Yeh, C. Y. Liu, and C. Chen, Appl. Phys. Lett., 76, 7 (2000).
6. S. Brandenberg and S. Yeh, Surface Mount Int. Conference and Exposition, SMI 98 Procedings, p.337 (1998)
7. C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett., 75, 58 (1999).
8. C. Y. Liu, C. Chen, and K. N. Tu, J. Appl. Phys, 88, 5703 (2000) .

參加 2006 TMS Annual meeting 研習心得

Presentation schedule for Chih Chen's group in 2006 TMS Annual meeting

3/13, Mon

EMPMD Council Meeting **12:00 PM - 2:00 PM** Conference Rooms 17 & 18

1.

2:55 PM
Integration of Electroplating and Electropolishing of Cu Damascene Process: *Sue-Hong Liu*[1]; Chih Chen[1]; Jia-Min Shieh[2]; Bau-Tong Dai[2]; Shih-Song Cheng[3]; Karl Hensen[3]; [1]National Chiao-Tung University; [2]National Nano Device Laboratories; [3]BASF Electronic Material Ltd.

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9:25 AM
Effect of Aging on Electromigration of Flip-Chip Solder Joints: *Che Cheng Chang*[1]; Chih Chen[1]; [1]National Chiao Tung University

3.

10:25 AM
Electromigration Study Using Kelvin Bump Structure: *Yuan-Wei Chang*[1]; Shih-Wei Liang[1]; Chih Chen[1]; [1]National Chiao Tung University

4.

11:05 AM
Mechanism of Void Formation in Flip-Chip Solder Joints: *Shih-Wei Liang*[1]; Yuan-Wei Chang[1]; Tung-Liang Shao[1]; Chih Chen[1]; [1]National Chiao Tung University

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11:40 AM
Redistribution of Pb-Rich Phase during Electromigration in Eutectic SnPb Solder Stripes: *Cheng-Chang Wei*[1]; Chung-Kwang Chou[1]; Chih Chen[1]; [1]National Chiao Tung University

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Joule Heating Effect in Flip-Chip Solder Joints for Various Dimension of Al Traces: *Sheng-Hsiang Chiu*[1]; Chih Chen[1]; S. S. Lin[2]; C. M. Chou[2]; Y. C. Liu[2]; K. H. Chen[2]; [1]National Chiao Tung University; [2]MEGIC Technology

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4:00 PM
Growth of Self-Organized Carbon Nanotubes Using Anodic Aluminum Oxide Template on a Si Substrate: *Ching-Jung Yang*[1]; Jia-Min Shieh[2]; Chang-Hsuan Lee[1]; Chih Chen[1]; Fu-Ming Pan[1]; Bau-Tong Dai[2]; [1]National Chiao Tung University; [2]National Nano Device Laboratories

2006 TMS Annual Meeting & Exhibition 會議為每年都會舉辦的大型學術會議之一，參加人數及論文數皆相當眾多，學術界與業界都是相當看重這個研討會，舉凡金屬、陶瓷、高分子...等都有非常多的議題討論，其中不乏在此領域之國際知名學界與業界專家與會，與會中很多論文議題內容相當充實，因此與其他參加者討論，都有相當收穫。我們更有幸在與中與中研院院士，美國 UCLA 材料系杜經寧教授討論銲錫在電遷移效應底下的問題，並且給我們很多寶貴的意見。

此次帶領學生參加場次主要為 Lead Free solder implementation: Reliability, Alloy Development, and new Technology: Electromigration and reliability，與會中發現許多發表有關於電遷移重要文獻的作者，都出現在此次的會議中，更帶來許多精采的演講內容，令我們大開眼界。與會中可以發現其實在電遷移這個領域，仍有許多未知的問題需要發掘，也還有非常多已知的問題需要克服。而伴隨著現今可攜式電子元件小尺寸化的趨勢，覆晶封裝技術具有極佳的電性和較好的散熱能力，此技術已經很普遍的被採用在高密度電子封裝產業中。伴隨著對於電子元件功能的需求越來越高，在現今的電路設計上，每一個覆晶凸塊所承載的電流愈來越大，當整個覆晶凸塊體積越來越小時，裡面的介面反應與電熱的相互效應勢必更加嚴重，如何開發新的材料或是討論出新的解決方法，這對於往後的覆晶封裝研究又是另一個重要的挑戰。此次參與國際會議獲益良多，本

實驗室的研究成果在電遷移的領域中是在於領先的地位，有許多的研究也引用到我們的論文。參加這個會議除了感受到著名的 TMS 年會盛況空前的氣氛外，更有機會能夠與國際知名專家學者會面並解與其討論，希望將來能再帶領學生參加這種國外的研討會，除了能訓練他們的外語表達能力，更能藉此機會加強學生的國際觀。

今年(2006)發表關於銲錫電遷移之論文

1. S. H. Chiu, T. L. Shao, Chih Chen*, D. J. Yao, and C. Y. Hsu, Infrared Microscopy of Hot Spots Induced by Joule Heating in Flip-chip SnAg Solder Joints under Accelerated Electromigration, **Appl. Phys. Lett.** 88, 022110 (2006) NSC 92-2216-E-009-008. SCI.
2. S. W. Liang, T. L. Shao, Chih Chen*, Everett CC Yeh, and K. N Tu, "Relieving Current Crowding Effect in Flip-chip Solder Joints during Current Stressing", **J. Mater. Res.** Vol. 21, No. 1, 137 (2006). NSC 92-2216-E-009-008.
3. C. K. Chou, C. A. Chen , S. W. Liang, and Chih Chen*, Redistribution of Pb-rich Phase during Electromigration in Eutectic SnPb Solder Stripes, **J. of Appl. Phys**. 99, 054502 (2006). NSC 92-2216-E-009-008. SCI.
4. S. W. Liang, Y. W. Chang, and Chih Chen* , Effect of Al-trace dimension on Joule heating and current crowding in flip-chip solder joints under accelerated electromigration, **Appl. Phys. Lett.** 88, 172108 (2006). NSC 94-2216-E-009-021.SCI.
5. C. C. Wei and Chih Chen*, Critical Length of Eutectic SnPb Solder Stripe, **Appl. Phys. Lett**. **88**, 182105 (2006). SCI.
6. Ying-Chao Hsu, Yuan-Ming Huang, Chih Chen*, and Henry Wang, Interfacial Reaction and Shear Strength of Pb-free SnAg2.5Cu0.8Sb0.5 and SnAg3.0Cu0.5Sb0.2 Solder Bumps on Au/Ni(P) Metallization, **J. of Alloy and Compound**, **417**, 180-186 (2006). SCI.
7. C. Y. Hsu, D. J. Yao*, S. W. Liang and Chih Chen, Everett C. C. Yeh, Temperature and current-density distributions in flip-chip solder joints with Cu traces, **J. Electronic Materials.** 35 (5): 947-953(2006). SCI.
8. S. W. Liang, Y. W. Chang, T. L. Shao, and Chih Chen*, K. N. Tu, Effect of 3-dimensional Current and Temperature Distribution on Void Formation and Propagation in Flip-chip Solder Joints during Electromigration, **Appl. Phys. Lett. 89**, 022117 (2006).
9. Y. W. Chang, S.W. Liang, and Chih Chen*: Study of void formation due to

electromigration in flip-chip solder joints using Kelvin bump probes, **Appl. Phys. Lett.**, **89**, 032103 (2006)

10. C. K. Chou, Y. C. Hsu, and Chih Chen*, Electromigration in Eutectic SnPb Solder Stripes, **J. Electronic Materials**. In press. SCI.
11. S. W. Liang, Y.W. Chang, and Chih Chen*, Geometrical effect of bump resistance measurement by Kelvin structure. **J. Electronic Materials.** In press. SCI.

12 S. H. Chiu, D.J. Yao, and Chih Chen*, Effect of Al-trace dimension on electromigration failure time of flip-chip solder joints, **J. Electronic Materials.** In press.

13. Chih Chen*, and S. W. Liang, **invited review** on "Electromigration Issues in Lead-Free Solder Joints" **J. Mater. Sci. : Materials in electronics.** In press.
14. K. N. Tu, Chih Chen, and Albert T. Wu, Stress analysis of spontaneous Sn whisker growth, **J. Mater. Sci.: Materials in electronics.** Invited review. **In press.**

以下附上其中五篇 APL 與一篇 JMR 論文供參考

Effect of Al-trace dimension on Joule heating and current crowding in flip-chip solder joints under accelerated electromigration

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Three-dimensional thermoelectrical simulation was conducted to investigate the influence of Al-trace dimension on Joule heating and current crowding in flip-chip solder joints. It is found that the dimension of the Al-trace effects significantly on the Joule heating, and thus directly determines the mean time to failure (MTTF). Simulated at a stressing current of 0.6 A at 70 °C, we estimate that the MTTF of the joints with Al traces in 100 μm width was 6.1 times longer than that of joints with Al traces in 34 μm width. Lower current crowding effect and reduced hot-spot temperature are responsible for the improved MTTF. © *2006 American Institute of Physics*.
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To meet the relentless drive for miniaturization of portable devices, flip-chip technology has been adopted for high-density packaging due to its excellent electrical characteristic and superior heat dissipation capability. As the required performance in microelectronics devices becomes higher, the design rule indicates that in each bump the operation current is expected to attain a value of 0.2 A, with further increase to 0.4 A likely in the near future.[1] Loading with such a high current at the confined space of the solder bump, electromigration inevitably becomes a critical reliability issue.[2] In addition, during accelerated electromigration test, the applied current may reach 2.0 A,[3] rendering substantial Joule heating in the solder bumps.[4] The total length of the Al trace is typically few hundreds to few thousands micrometers, which corresponds to a resistance of approximately few hundreds milliohms or few ohms. In contrast, the resistances of the solder bumps and the Cu trace in the substrate are relatively low, typically in the order of few or tens of milliohms. Therefore, the primary contributor for Joule heating in the solder joints is the Al trace.[4] As a result, the temperature in the bumps during accelerated testing is likely to be much higher than that of the ambient because of the Joule heating. The other critical issue is the current crowding effect in the solder bumps. The line-to-bump geometry is believed to render undesirable current crowding behavior, resulting in elevated current density in the solder regime than the average current density.[5] These two issues play substantial roles in the mean-time-to-failure (MTTF) analysis, as delineated by Black's equation,[6]

$$\mathrm{MTTF} = A\frac{1}{j^n}\exp\left(\frac{Q}{kT}\right), \tag{1}$$

where A is a constant, j is the current density, n is a model parameter for current density, Q is the activation energy, k is the Boltzmann constant, and T is the average bump temperature. It follows that the MTTF decreases exponentially with increasing bump temperature. Wu *et al.*[7] conducted a series of electromigration tests for SnPb solder bumps, and observed that the MTTF decreased from 711 to 84 h as the testing temperature was raised from 125 to 150 °C at a current density of 5.0×10^3 A/cm^2. In addition, the MTTF decreased from 277 to 84 h as the current density was doubled from 2.5×10^3 to 5.0×10^3 A/cm^2 at 150 °C. Predicted by Black's equation and validated experimentally by Wu *et al.*, the stressing temperature and the current density both play substantial role in determining the observed MTTF.

Several intrinsic material characteristics contribute to the Joule heating and current crowding effects. They include the dimension of Al trace, the thickness of under bump metallization (UBM), the UBM materials, the solder materials, as well as the dimension of passivation.[8] Among them, the dimension of Al trace is believed to be the critical one. However, no systematic studies have been initiated to elucidate the effect of Al-trace dimension in Joule heating and current crowding of the solder joints during electromigration. This is because the solder joints are completely encapsulated by Si die, underfill, and underlying substrate. Hence, it is somewhat difficult to analyze the temperature fluctuation and the current density inside the solder joints. To overcome this problem, in this study we used a three-dimensional thermoelectrical simulation to identify the temperature and the current density inside the solder bumps. This study offers a better insight on the effect of Al-trace dimension in the Joule heating and current crowding during accelerated electromigration of solder joints.

To proceed our simulation, four models with identical structure of solder bumps and Cu lines but with different dimensions of Al trace were constructed. Shown in Fig. 1(a) is a standard model, which includes two SnPb solder bumps connected by an Al trace of 1840 μm in length, 34 μm in width, and 1.5 μm in thickness. For the second model, as shown in Fig. 1(b), the width of the Al trace was increased to 100 μm with the remaining structure unchanged. Figure 1(c) exhibits the third model, in which the thickness of the Al trace was adjusted to 4.4 μm with the remaining dimension identical to those of the first model. It is noted that the second and the third model had the same cross-sectional area of Al trace. For the fourth model, as depicted in Fig. 1(d), a shorter Al trace which is 670 μm less than the standard model was used while the remaining features identical to those in the first model. The dimension of the Si chip was

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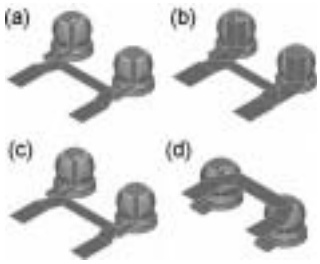

FIG. 1. The four models constructed in this study. (a) The first model with a 34-μm-wide, 1.5-μm-thick, and 1848-μm-long Al trace. (b) The second model with a wider Al trace of 100 μm. (c) The third model with a thick Al trace of 4.4 μm. (d) The fourth model with a shorter Al trace of 1178 μm.

7.0×4.8 mm^2 with its thickness of 290 μm. The dimension of the bismaleimide triazine (BT) substrate was 5.4 mm in width, 9.0 mm in length, and 480 μm in thickness. The bottom of the BT substrate was maintained at 70 °C and the convection coefficient was set to be 10 W/m^2 °C in a 25 °C ambient temperature. The intrinsic parameters of materials used in this simulation can be found in our previous publication.[9] Constant currents, ranging from 0.1 to 0.6 A, were applied through the two Cu lines on the BT substrate.

The current crowding effect can be relieved to some extent by increasing the width or the thickness of the Al trace. In this letter, we designate the crowding ratio to be the maximum current density inside the solder bump divided by the average current density in the UBM opening, which was obtained assuming the current spreads uniformly on the UBM opening. The crowding ratio indicates the degree of nonbalance in the current distribution in the solder bump. It is realized that the current crowding would accelerate the damage caused by electromigration because of the enhanced wind force in the current crowding region. Figures 2(a)–2(d) demonstrate the cross-sectional views for the current density distribution of the four models as they were stressed at 0.6 A. As shown, the local current density inside the solder bump near the entrance of the Al trace was reduced substantially in the second and the third model. The crowding ratio for the first model reached a value of 19.8. When the cross section of the Al trace was increased by 2.9 times, the crowding ratios were reduced down to 12.0 and 11.7 for the second and the third model, respectively. Since the geometry of the Al trace near the solder bump was not varied for the fourth model, the distribution of current remained the same as the first model. From our simulation, we conclude that increasing the cross section of the Al trace directly reduced the crowding ratio.

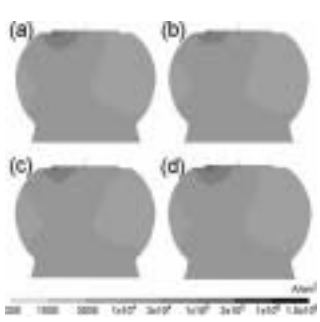

FIG. 2. The cross-sectional views for the current-density distribution in the solder bump when they were stressed by 0.6 A. (a) The first model. (b) The second model. (c) The third model. (d) The fourth model.

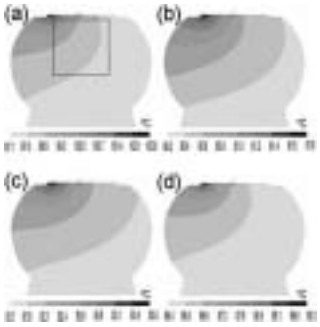

FIG. 3. The cross-sectional views for the temperature distribution in the solder bumps when they were applied by 0.6 A at 70 °C. (a) The first model. (b) The second model. (c) The third model. (d) The fourth model.

Furthermore, the dimension of the Al trace exerts significant effect on Joule heating of the solder bumps. Figures 3(a)–3(d) illustrate the temperature distributions in the center cross sections for the four models when they experience a stress current of 0.6 A at 70 °C. A hot spot inside the solder bump was observed near the entrance point of the Al trace into the solder bump just beneath the passivation opening. The mean temperature was obtained by averaging the node temperatures in a 70×70 μm^2 area, as shown in Fig. 3(a). The temperatures in the hot spot were 102.8, 81.7, 83.6, and 90.3 °C for the four models, respectively, whereas the average temperatures were 97.9, 80.6, 82.0, and 86.1 °C, respectively. It can be seen that the Joule heating effect was greatly reduced when the cross section of the Al trace was increased. Figures 4(a) and 4(b) show the hot-spot and average temperatures as a function of the applied current up to 0.6 A. Also, the trend for lower stressing current behaves the same with smaller magnitude in temperature difference as that stressed by 0.6 A. Due to the hot spot, a thermal gradient was built up across the solder bump. The thermal gradient was derived from the temperature difference between the hot-spot and the average temperature of the solder close to the BT side, divided by the bump height. It can be observed that the second model exhibits the lowest thermal gradient among the four models.

In general, the Al trace is considered to be the primary Joule heating source during accelerated electromigration test as its cross-section area is typically one to two orders of magnitude less than that of the solder bump and the Cu line. Under the same applied current, the Joule heating power is proportional to the total resistance of the stressing circuit. The resistance of the Al trace for the first model was 1331 mΩ, whereas it decreased to 530, 551, 532 mΩ for the rest of the three models, respectively. Therefore, the Joule heating effect was less significant for the stressing circuit configuration with smaller total resistance. In addition, for the third and fourth models, the total resistance and the cross section for heat dissipation were almost identical, yet there is still 6.7 °C difference in hot-spot temperature. Since the average current density in the Al trace for the fourth model was about three times larger than that for the third model, the local Joule heat power, which is proportional to the square of the local current density, is likely to be responsible for the temperature difference in these two models.

Furthermore, the effect of Al-trace dimension on the MTTF could be estimated using Eq. (1). For the same solder joint with different dimensions of the Al traces under the

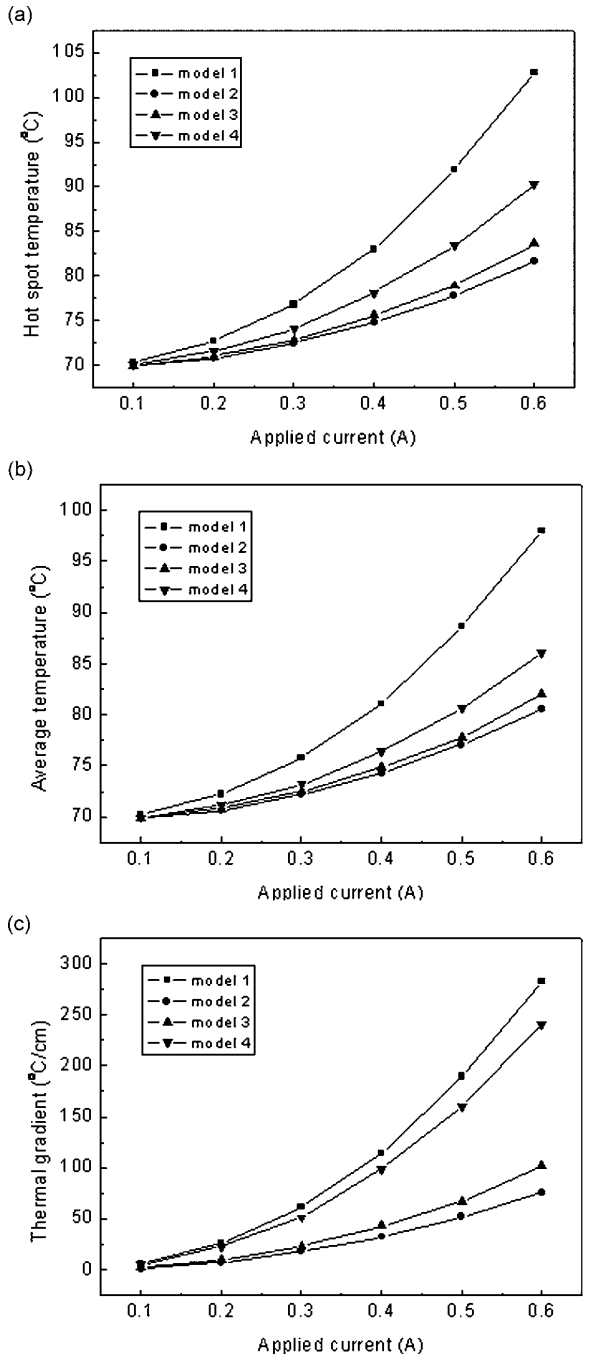

FIG. 4. (a) The hot-spot temperature. (b) The average temperature. (c) The thermal gradient in the solder bump as a function of applied current up to 0.6 A at 70 °C for the four models.

same stressing conditions, the activation energy Q and the constant A are kept identical for the four models. Choi *et al.* proposed that the term j^{-n} in the equation needs to be revised to $(cj)^{-n}$ in order to include the high current crowding effect in the solder joints. In addition, the temperature factor is modified to $(T+\Delta T)$ to account for considerable Joule heating effect during the accelerated electromigration test. Brandenburg and Yeh found that n is equal to 1.8 for the eutectic solder joints when the average current density is employed, and the activation energy they measured was 0.5 eV for the SnPb solder with Al/Ni(V)/Cu UBM.[10] Since voids typically form near the entrance point of the Al trace where the solder experiences the maximum current density and the hot-spot temperature, we propose that the (cj) term to be taken as the maximum current density and the hot-spot temperature should be adopted for the $(T+\Delta T)$ term. For the solder joint in the standard model, the maximum current density reached 1.05×10^5 A/cm^2 and the hot-spot temperature was 102.8 °C. For the solder joint with Al trace in 100 μm width, the maximum current density was 6.39×10^4 A/cm^2 and the hot-spot temperature was reduced down to 81.7 °C. The MTTF would be 6.1 times longer than that of the standard model under 0.6 A at 70 °C, in which the relief of current crowding contributed about 2.5 times, and the decrease in Joule heating contributed approximately 2.5 times on the lifetime increase. For the joint with Al trace in 4.4 μm thickness, the maximum current density decreased to 6.20×10^4 A/cm^2 and the hot-spot temperature was reduced to 83.6 °C. The estimated MTTF would be 5.9 times longer than that of the standard. For the fourth model, the MTTF is about 1.7 times longer than that of the standard model, mainly due to lower Joule heating effect. It is noteworthy that the Joule heating effect could be further reduced if the length of the Al trace is further decreased, but the current crowding effect remains the same when only the length is changed. The above estimation demonstrates that the solder joints with wider or thicker Al traces could significantly increase the electromigration resistance. In addition, it also indicates that the Joule heating effect needs to be taken into account during the accelerated electromigration test. Otherwise, the MTTF may be underestimated.

In conclusion, the dimension of the Al trace plays a crucial role in the Joule heating effect during accelerated electromigration test since the Al trace is the dominant heating source. The solder joints with wider or thicker Al trace would render reduced current crowding and Joule heating effects. Therefore, the electromigration lifetime would be extended significantly for the solder joints with wider or thicker Al traces under the same stressing conditions.

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[1] K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[2] International Technology Roadmap for Semiconductors, Assembly and Packaging Section, Semiconductor Industry Association, San Jose, CA, 2003, pp. 4–9.
[3] W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. **94**, 5665 (2003).
[4] T. L. Shao, S. H. Chiu, Chih Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. **33**, 1350 (2004).
[5] Everett C.C. Yeh, W. J. Choi, and K. N. Tu, Appl. Phys. Lett. **80**, 4 (2002).
[6] J. R. Black, IEEE Trans. Electron Devices **ED-16**, 338 (1969).
[7] J. D. Wu, P. J. Zheng, Kelly Lee, C. T. Chiu, and J. J. Lee, Proceedings of the 52th Electronic Components and Technology Conference, IEEE Components, Packaging, and Manufacturing Technology Society, San Diego, CA, 2002 (unpublished), p. 452.
[8] S. W. Liang, T. L. Shao, and Chih Chen, J. Mater. Res. **21**, 137 (2006).
[9] S. H. Chiu, T. L. Shao, Chih Chen, D. J. Yao, and C. Y. Hsu, Appl. Phys. Lett. **88**, 022110 (2006).
[10] S. Brandenburg and S. Yeh, *Proceedings of Surface Mount International Conference and Exhibition*, San Jose, CA, 23–27 August 1998 (SMTA, Edina, MN, 1998), p. 337.

Effect of three-dimensional current and temperature distributions on void formation and propagation in flip-chip solder joints during electromigration

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Effect of *three-dimensional* current distribution on void formation in flip-chip solder joints during electromigration was investigated using thermoelectrical coupled modeling, in which the current and temperature redistributions were coupled and simulated at different stages of void growth. Simulation results show that a thin underbump metallization of low resistance in the periphery of the solder joint can serve as a conducting path, leading to void propagation in the periphery of the low current density region. In addition, the temperature of the solder did not rise significantly until 95% of the contact opening was eclipsed by the propagating void. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2220550]

Electromigration has become a critical reliability issue for high-density solder joints in flip-chip technology.[1,2] Electromigration-induced failures and mean time to failure (MTTF) of flip-chip joints have been investigated for both eutectic SnPb and Pb-free solders.[3–10] It was found that voids were formed inside the solder adjacent to the underbump metallization (UBM),[4] and propagated along the interface between the solder and the UBM, causing opening failure of the joints when the voids eclipsed the entire contact opening. However, the mechanism of void nucleation and growth and especially the corresponding change of current distribution in the solder joint due to void formation are unclear. In particular, it is unknown why some voids are formed at the periphery of the UBM opening under the dielectric, where the current density is low.[8,11] In Blech structure of Al stripes, Tu *et al.* proposed that resistive vacancy might move to the low current density region to form voids due to the high gradient of current density, which was as high as 10^{10} A/cm^3.[12] However, for flip-chip solder joint, the gradient is estimated to be only 1.33×10^6 A/cm^3 owing to its large dimension.[8] Therefore, the growth of voids in the periphery of the UBM opening, which is located at the low current density region, may not be driven by the gradient of current density. In this letter, three-dimensional finite element method was employed to simulate the effect of void formation on redistribution of current density and temperature in a flip-chip solder joint, especially in the periphery area where a low-resistance thin-film UBM exists.

Three-dimensional (3D) thermoelectrical coupled simulation was carried out by finite element analysis to find out the current density and temperature redistributions in our test samples.[13] The model used was a SOLID69 eight-node hexahedral coupled field element with ANSYS software. The electrical and thermal resistivities of the materials as well as the boundary conditions used in this modeling followed those of our previous study.[13] In our samples, the diameters of the passivation opening and the UBM opening were 85 and 120 μm, respectively. Figure 1(a) shows the cross-sectional view of the current density distributions before void growth when 0.28 A was applied to the bump. The Al trace, the UBM in the chip side, and the metallization in the substrate were ignored. It was found that the current crowded into the solder bump in the passivation opening. The current crowding behavior near the entrance of the Al trace can be clearly demonstrated. The maximum current density reached 5.42×10^4 A/cm^2, which is about 22 times higher than the average value. It is proposed that this local high current density was responsible for the initial void formation due to flux divergence.[4,6] Figure 1(b) illustrates the temperature distribution before void formation. The maximum temperature inside the solder bump was 109.6 °C; therefore, the increase in temperature due to Joule heating was only 9.6 °C. The temperature was quite uniform inside the bulk of the solder.

In stage I, a semicylindrical void, 45.5 μm in diameter and 13.0 μm in height, was formed inside the solder near the entrance of the Al trace. The current redistributed due to void formation, and the maximum current density occurred in the solder near the upper left corner of the periphery of the UBM opening under the Al trace. As shown in Fig. 2(a), void for-

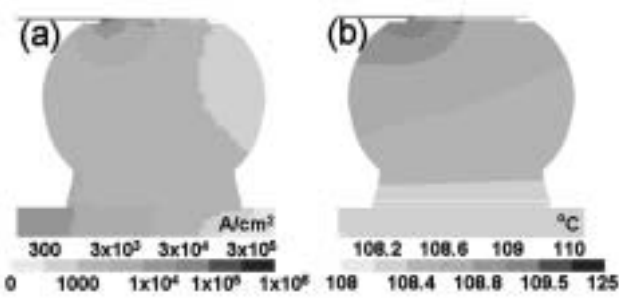

FIG. 1. (a) Cross-sectional view of current density distribution in solder joint before void formation; (b) corresponding cross-sectional view for temperature distribution.

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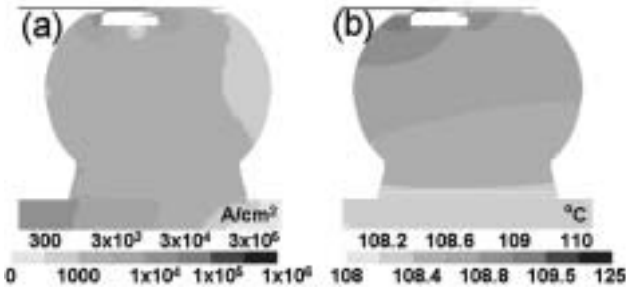

FIG. 2. (a) Cross-sectional view of current density distribution in solder joint at stage I; (b) corresponding cross-sectional view for temperature distribution.

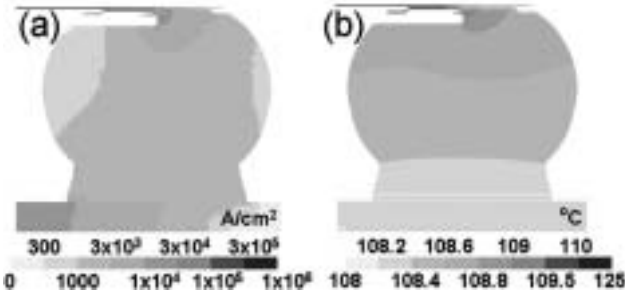

FIG. 3. (a) Cross-sectional view of current density distribution in solder joint at stage II; (b) corresponding cross-sectional view for temperature distribution.

mation resulted in redistribution of current in two ways. First, current may drift farther along the Al trace, passing the void, and entered the solder. Second, the current may drain down to the solder through the surrounding UBM/intermetallic layer (IMC) layer. It is intriguing that the UBM/IMC layers served as a current path, directing the current into the upper left corner of the periphery of the UBM opening. Since the UBM/IMC layers have much higher electromigration resistance,[2] voids are formed mainly inside the solder. It is clear that the solder on the left of the void has higher current density than that under the passivation opening. Therefore, voids may propagate toward the solder in the UBM periphery. Compared with that shown in Fig. 1, the maximum current density inside the solder has been reduced to 4.43×10^4 A/cm^2 due to void formation. On the other hand, the temperature inside the solder decreased slightly to 109.5 °C, which was 0.1 °C lower than that before void formation, as illustrated in Fig. 2(b). This may be attributed to the smaller crowding effect as a result of void formation.

Since the maximum current density occurred near the periphery of the UBM opening, we assume that the void propagates toward the left-hand-side periphery, as illustrated in Fig. 3(a). The void depleted 50% of the UBM opening, which is denoted as stage II. Since the UBM/IMC layers still serve as a current path, the void may be able to propagate to the edge of the solder bump. Therefore, we postulate that the growth of void in the low current density region under the periphery of the UBM opening is mainly attributed to current redistribution, not to the gradient of current density. The maximum current density inside the solder bump reduced further to 4.04×10^4 A/cm^2 due to void formation. Figure 3(b) shows the corresponding temperature distribution in the solder bump. The maximum temperature in the solder was 109.3 °C, which was 0.2 °C lower than that in stage II. Again, this may be due to the smaller crowding effect in the solder joint at this stage. Although there was a slight increase in temperature in the Al pad, the temperature inside the solder did not alter much at this stage. From the results reported by Gee *et al.*,[11] the shape of the void may resemble a pancake shape for solder joints with thin-film UBM. In addition, due to the limitation of our simulation modeling, semicylindrical voids were adopted in this study. However, whether it is circular, semicircular, or irregular remains unclear at this moment, and needs further experimental investigation.

The void was then assumed to propagate to fill 80.5% of the UBM opening, as shown in Fig. 4(a). It is denoted as stage III. The current entered the joints through a smaller contact area, causing an increase in maximum current density. It rose to 8.70×10^4 A/cm^2, and almost the whole passivation opening experienced current density higher than 1.0×10^4 A/cm^2. Therefore, void propagation would expedite in this stage. The maximum temperature in the solder bump increased to 109.4 °C because of the higher current crowding effect at this stage, as shown in Fig. 4(b). In the absence of current flowing through the solder in the left-hand side of the joint, the temperature on the right-hand side was higher than that on the left-hand side. However, there was still no obvious temperature increase in the solder close to the entrance point of the current into the solder.

The solder in the passivation opening was completely depleted at this final stage, leaving a small amount of solder near the periphery of the UBM opening, as illustrated in Fig. 5(a). There was approximately 4.0% of contact area left for conducting the current at this stage. With further decrease in contact area, the maximum current density became 1.69×10^5 A/cm^2. The UBM/IMC layers served as a conducting path to direct the current to the remaining solder. Hence, the remaining solder near the periphery of the UBM opening could be completely depleted and failure followed. Figure 5(b) shows the temperature distribution at this stage. The maximum temperature in the solder bump was 110.4 °C, which was 0.8 °C higher than that before void formation.

TABLE I. The simulated maximum current density inside the solder, the corresponding crowding ratio as well as the bump resistance at each stage.

	Original bump	Stage I	Stage II	Stage III	Stage IV
Void proportion (area%)	0	28.8	50.0	80.5	96.0
Maximum current density inside solder (A/cm^2)	5.42×10^4	4.43×10^4	4.04×10^4	8.70×10^4	1.69×10^5
Bump resistance (mΩ)	11.2	14.6	19.0	25.3	42.9
Maximum temperature inside solder (°C)	109.6	109.5	109.3	109.4	110.4

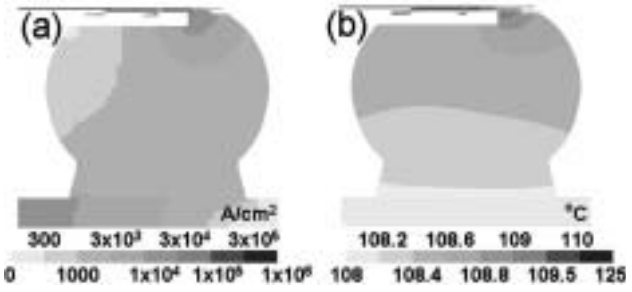

FIG. 4. (a) Cross-sectional view of current density distribution in solder joint at stage III.; (b) corresponding cross-sectional view for temperature distribution.

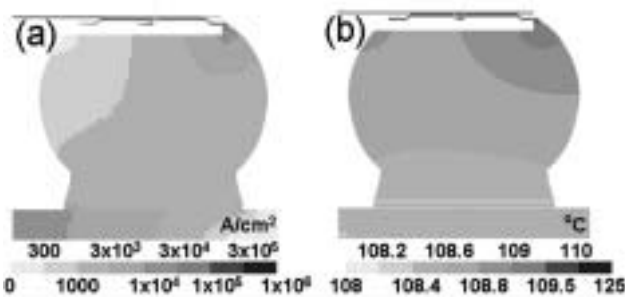

FIG. 5. (a) Cross-sectional view of current density distribution in solder joint at stage IV; (b) corresponding cross-sectional view for temperature distribution.

Our simulation also shows that bump resistance increased gradually in the first three stages, and then increased rapidly in the final stage, as shown in Table I. Bump resistance was defined as the decrease in voltage between the entrance point of the Al trace into the Al pad (disk) and the junction point of the Cu line with the solder joint. In stage I, the bump resistance increased from 11.2 to 14.6 mΩ. It increased to 19.0 and 25.3 mΩ in stages II and III, respectively. It rose to 42.9 mΩ in stage IV. This increase in bump resistance may also enhance the local Joule heating effect. However, no significant local Joule heating was found in the thermal simulation up to stage IV. This may be attributed to the fact that the major heating source was the Al trace.[14] In our model, the total resistance of the Al trace was about 1800 mΩ. Consequently, the increase in bump resistance was quite small compared with that of the Al trace. In addition, the increase in bump resistance was mainly due to the following manner: owing to void formation, the current needed to drift farther in the Al pad (disk), and then flowed down to the solder bump. Therefore, the local Joule heating in the Al pad (disk) increased when voids were formed. Since there was good heat dissipation in the Si side, the increase in temperature due to void formation was quite small. Nevertheless, the increase might be higher when larger current was applied, since the overall Joule heating would be significantly higher at higher stressing current.

In summary, we have employed the 3D finite element method to simulate the current and temperature redistributions due to the formation and propagation of a pancake-shape void in solder joints during electromigration. It is proposed that current redistribution is the main reason accounting for void formation and propagation, especially the propagation into the low current density region below the contact passivation. It is found that UBM provided a conducting path for current to go below the passivation, and it directed the current to the periphery of the solder joint, which is in agreement with the experimental observation of void formation in those regions. Increase in temperature due to void formation was not significant since the major heat source was the Al trace and the applied current was as low as 0.28 A.

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[1]International Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, 2003.
[2]K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[3]C. Y. Liu, Chih Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
[4]Everett C.C. Yeh, W. J. Choi, and K. N. Tu, Appl. Phys. Lett. **80**, 4 (2002).
[5]W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. **94**, 5665 (2003).
[6]J. W. Nah, K. W. Paik, J. O. Suh, and K. N. Tu, J. Appl. Phys. **94**, 7560 (2003).
[7]J. D. Wu, P. J. Zheng, C. W. Lee, S. C. Hung, and J. J. Lee, Microelectron. Reliab., **46**, 41 (2006).
[8]T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen, J. Appl. Phys. **96**, 4518 (2004).
[9]J. W. Jang, L. N. Ramanathan, J. K. Lin, and D. R. Frear, J. Appl. Phys. **95**, 8286 (2004).
[10]H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. **82**, 7 (2003).
[11]L. Zhang, S. Ou, J. Huang, K. N. Tu, S. Gee, and L. Nguyen, Appl. Phys. Lett. **88**, 012106 (2006).
[12]K. N. Tu, C. C. Yeh, C. Y. Liu, and Chih Chen, Appl. Phys. Lett. **76**, 988 (2000).
[13]S. H. Chiu, T. L. Shao, Chih Chen, D. J. Yao, and C. Y. Hsu, Appl. Phys. Lett. **88**, 022110 (2006).
[14]T. L. Shao, S. H. Chiu, Chih Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. **33** 1350 (2004).

Infrared microscopy of hot spots induced by Joule heating in flip-chip SnAg solder joints under accelerated electromigration

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Joule heating effect in solder joints was investigated using thermal infrared microscopy and modeling in this study. With the increase of applied current, the temperature increased rapidly due to Joule heating. Furthermore, modeling results indicated that a hot spot existed in the solder near the entrance point of the Al trace, and it became more pronounced as the applied current increased. The temperature difference between the hot spot and the solder was as large as 9.4 °C when the solder joint was powered by 0.8 A. This hot spot may play an important role in the initial void formation during electromigration. © *2006 American Institute of Physics*.
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Electromigration has emerged as another reliability issue for high-performance and high-density flip-chip solder joints,[1,2] and electromigration in solder joints has been studied in recent years.[3–7] The current crowding effect has been found to be responsible for the failure in the chip/anode side of the solder joint.[8,9] The current used for typical accelerated electromigration tests ranges from 0.5 A to 2.2 A. Although whether a hot spot exists at the current crowding region is of interest, only a few studies have addressed the Joule heating effect in solder joints.[10–12] However, there are still no experimental data to verify the temperature in the bump because the solder joints are completely surrounded by a chip, a substrate, and underfill; so no direct temperature measurement can be made to investigate the Joule heating effect inside the solder joints.

For this study, we used thermal infrared (IR) microscopy to measure the temperature distribution in the Al trace at various stressing conditions. Based on the experimental data, we constructed a finite element model to simulate the temperature distribution inside the solder bump during current stressing. Therefore, this study provides a deeper understanding of the Joule heating effect inside the flip-chip solder joints during current stressing.

The fabrication procedure for the SnAg bumps can be found in our previous publication.[8] The thickness of the Si chip was 300 μm. The under-bump metallization (UBM) consisted of 0.7 μm Cu, 0.3 μm Cr–Cu, and 0.1 μm Ti. It is assumed that a layer-type Cu_6Sn_5 intermetallic compound (IMC) of 1.4 μm thick grew in the interface of the UBM and the solder, whereas a layer-type Ni_3Sn_4 IMC of 1.0 μm thick formed in the interface of the pad metallization and the solder in the substrate side. The UBM and passivation openings were 120 μm and 85 μm in diameter, respectively. The Al trace on the chip side was 34 μm wide and 1.5 μm thick.

The temperature increase inside the bumps when powered by electric current was detected by thermal IR microscopy, that had resolution of 0.1 °C in temperature sensitivity and 2.8 μm in spatial resolution.

On the basis of the experimental results, a three-dimensional (3D) simulation was carried out by finite element analysis. Only two of the solder bumps had electrical current passing through. The electrical and thermal resistivities for the materials used in this modeling are listed in Table I. The effect of temperature coefficient of resistivity (TCR) was considered, and the TCR values for the metals are also listed in Table I. In addition, 3D coupled thermal-electric simulation was conducted to predict the steady-state temperature distribution using the ANSYS software package developed by ANSYS, Inc. The model used in this study was a SOLID69 eight-node hexahedral coupled field element. All the boundary conditions followed the experiment setup. The area

TABLE I. Thermal conductivities, electrical resistivities, and temperature coefficients of resistivity for the materials used in the simulation model.

Material	Thermal conductivity (W m °C)	Resistivity ($\mu\Omega$ cm) at 20 °C	TCR (10^{-3} K^{-1})
Silicon	147.00	···	···
Al trace	238.00	2.70	4.2
UBM(Ti+Cr/Cu+Cu)	147.61	5.83	4.9
SnAg3.5	33.00	12.3	4.6
Ni	76.00	6.8	6.8
Cu pad	403.00	1.7	4.3
BT (substrate)	0.70	···	···
Underfill	0.55	···	···
Passivation	0.34	···	···

Note: The materials not given in electric resistivity are assumed to be electrical insulators.

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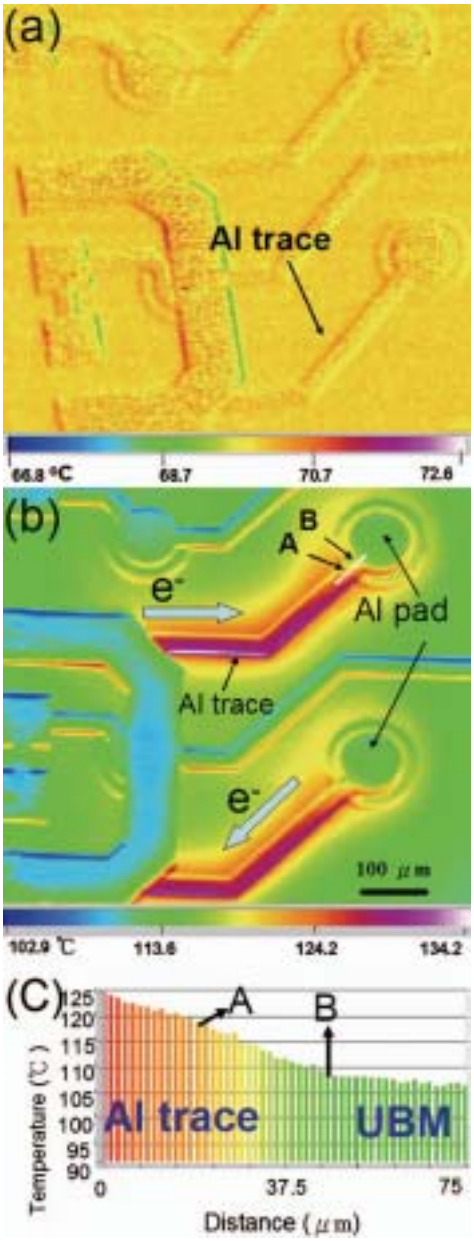

FIG. 1. (Color) (a) Temperature distribution in the package before current stressing, showing a uniform temperature in the package; (b) Temperature distribution in the Al trace measured by the IR microscope when powered by 0.59 A; (c) Temperature profile along the white line in (b).

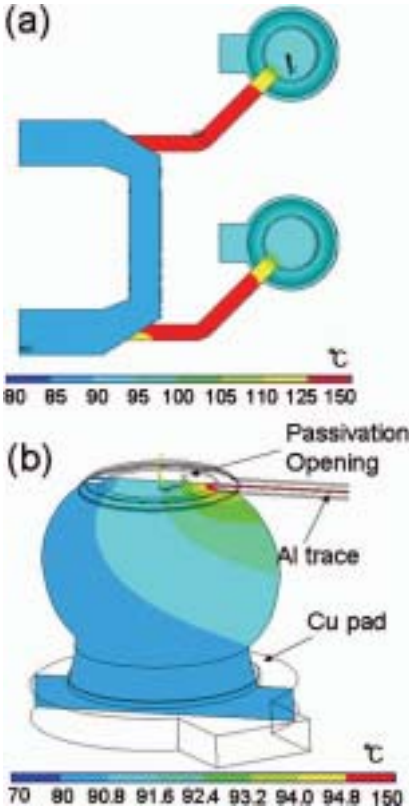

FIG. 2. (Color) (a) Simulated temperature distribution in the stressing circuit when powered by 0.59 A. (b) Temperature distribution inside the solder for one of the cross sections near the Al trace. A hot spot was found in the entrance point of the Al traces.

of the Si chip was 10.0 mm×6.0 mm and the thickness was 290 μm, whereas the bismaleimide triazine (BT) substrate was 4.75 mm wide, 7 mm long, and 350 μm thick.

Before the current stressing, calibration was performed on a hot plate maintained at 70 °C. The temperature distribution without current stressing is shown in Fig. 1(a). The circuit of the Al trace can barely be seen since the Si substrate is transparent to IR radiation. Figure 1(b) shows the temperature increase for the Al trace in the package when stressed by 0.59 A at the ambient temperature of 70 °C. The current path is indicated by two of the arrows in the figure. There were two solder bumps located directly below the two circular Al pads/UBMs, as labeled in the figure. It is noteworthy that the Al trace has much higher temperature than the circular Al pads, which were directly connected to the UBM and the solder bumps. The maximum temperature was as high as 134 °C, which occurred approximately at the middle of the Al trace, whereas the temperature was only about 105 °C for the Al pads above the solder bumps. The inner circle of the Al pad in Fig. 1(b) represents the passivation opening, whereas the outer circle corresponds to the UBM opening of the solder joint.

Furthermore, whether a hot spot exists inside the solder is of interest for electromigration study. Figure 1(c) illustrates the temperature profile along the 75 μm long dashed line in Fig. 1(b). The points A and B in Fig. 1(b) represent the edges of the UBM and the passivation openings, respectively. The temperatures at points A and B were approximately 118.2 °C and 109.7 °C, respectively, which are much higher than the average temperature of 105.2 °C in the Al pad. The average temperature was calculated by averaging the temperatures in a 10 μm×10 μm square in the center of the passivation opening. In addition, there is a thermal gradient since the temperature at the Al pad near the entrance of the Al trace was higher than that at the opposite end. The gradient in this junction was as high as 1700 °C/cm.

Figure 2(a) shows the simulated temperature distribution in the Al trace and in the solder joints when stressed by 0.59 A. The simulation results fit the experimental results very well. The temperature distribution inside the solder in one of the cross sections near the entrance of the Al trace is shown in Fig. 2(b). A hot spot existed in the solder adjacent to the entrance points of the Al trace into the solder at the passivation opening. The temperature at the spot was 95.6 °C, which was 4.5 °C higher than the average value in the solder. The temperature on the chip side was higher than

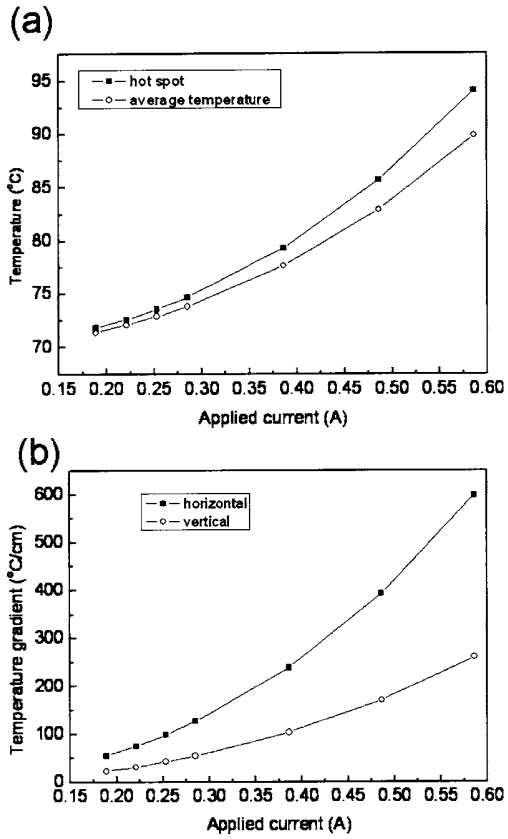

FIG. 3. (Color) (a) Simulated temperature in the solder joint and in the hot spot as a function of applied current up to 0.8 A. (b) Vertical and horizontal thermal gradients in the solder bumps as a function of applied current up to 0.8 A.

that on the substrate side. In addition, the vertical thermal gradient was measured to be 276 °C/cm, whereas the horizontal thermal gradient was calculated to be 634 °C/cm at this stressing condition. The thermal gradient is denoted in this letter as the subtraction of the temperature in the hot spot by the temperature at the opposite end of the solder, then divided by the distance between the two locations. Under this stressing condition, the current density in the Al trace was 1.1×10^6 A/cm^2. The average current density in the joint was 5.2×10^3 A/cm^2 based on the UBM opening. In the hot spot, the maximum current density was 1.7×10^5 A/cm^2, whereas the average current density involved in a volume of 5 μm$\times$5 μm$\times$5 μm was estimated to be 1.4×10^5 A/cm^2.

The Joule heating effect was also inspected at various applied currents. Figure 3(a) depicts the temperature in the hot spot and the average temperature in the solder as a function of applied current up to 0.8 A. Both of them increased rapidly with the increase of applied current. The difference in these two temperatures increases as the applied current increases, and it may be as high as 9.4 °C when stressed by 0.8 A. Figure 3(b) shows the vertical and horizontal thermal gradients as functions of the applied current. They also increase with the increase in stressing current. Moreover, the horizontal thermal gradient rose more quickly than the vertical one, reaching 1320 °C/cm under the stressing of 0.8 A.

The existence of the hot spot may be attributed to two reasons. First, it may be due to the local Joule heating inside the solder itself. The heating power can be expressed as

$$P = I^2R = j^2\rho V,$$

where P is Joule heating power, I is the current, R is the resistance, j is the local current density, V is the volume of the material, and ρ is the resistivity. The product of I^2R is the total heating power, whereas $j^2\rho$ is the heating power per unit volume. In our simulation model, the total resistance of the Al trace was about 900 mΩ, and the resistance of the solder bump was about 10 mΩ. Therefore, the Al trace generated most of the heat. Due to the serious current crowding in the solder joint, the current density in the vicinity of the Al entrance into the solder joint is typically one to two orders higher than the average value,[7,8] causing local Joule heating there. Second, the Al trace has higher Joule heating effect, and the hot spot was close to the Al trace. At lower stressing current, the hot spot is not obvious because there is less heat generation. However, it became more pronounced as the applied current increased due to large heat generation and difficulty in heat dissipation. The solder in the hot spot was the most vulnerable part in the solder joint during electromigration testing, since it may experience much larger electron wind force due to the higher current density and the higher diffusivity owing to the higher temperature as well as its low melting point. Hence, voids start to form at this spot.[8]

In summary, the Joule heating effect in the solder joints has been experimentally investigated using an IR microscope and a 3D coupled thermal-electrical simulation. The temperature distribution in joints can be determined thoroughly. A hot spot was found in the vicinity of the entrance point of the Al trace, which is detrimental to the electromigration lifetime of the solder joints.

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[1] K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[2] *International Technology Roadmap for Semiconductors*, Assembly and Packaging Section, Semiconductor Industry Association, San Jose, CA (2003), pp 4–9.
[3] S. Brandenburg and S. Yeh, in *Proceedings of Surface Mount International Conference and Exhibition*, San Jose, CA, 23–27 August 1998 (SMTA, Edina, MN, 1998), p. 337.
[4] C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
[5] W. J. Choi, E. C. C. Yeh, and K. N. Tu, J. Appl. Phys. **94**, 5665 (2003).
[6] T. Y. Lee, K. N. Tu, and D. R. Frear, J. Appl. Phys. **90**, 4502 (2001).
[7] Everett C. C. Yeh, W. J. Choi, and K. N. Tu, Appl. Phys. Lett. **80**, 4 (2002).
[8] T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen, J. Appl. Phys. **96**, 4518 (2004).
[9] J. W. Nah, K. W. Paik, J. O. Suh, and K. N. Tu, J. Appl. Phys. **94**, 7560 (2003).
[10] T. Y. T. Lee, T. Y. Lee, and K. N. Tu, in *Proceedings of the 51st Electronic Components and Technology Conference* (IEEE Components, Packaging, and Manufacturing Technology Society, Orlando, FL, 2001), p. 558.
[11] H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. **82**, 7 (2003).
[12] T. L. Shao, S. H. Chiu, C. Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. **33**, 1350 (2004).

Critical length of electromigration for eutectic SnPb solder stripe

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The critical length of eutectic SnPb solder was investigated using solder stripes. By employing focus ion beam, solder stripes of various lengths, including 5, 10, 15, 20, 30, 100, and 200 μm, can be fabricated. Length-dependent electromigration behavior was observed, which implies that there may be back stress under stressing. The critical length was determined to be between 10 and 15 μm under stressing by 2×10^4 A/cm^2 at 100 °C, and the corresponding critical product was between 20 and 30 A/cm. Both values show good agreement with their theoretical values. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2200158]

With the portable devices becoming smaller and more compact in size, flip-chip technology has been adopted for fine-pitch packaging in microelectronics industry.[1] Area array of tiny solder joints can be fabricated on Si chips to achieve high-density packaging. In addition, as the required performance continues to increase, the input/output (I/O) pin count of flip-chip products has dramatically increased and the current that each bump needs to carry continues to increase, resulting in higher current density flowing in each solder bump. Therefore, electromigration (EM) has become an important reliability issue in solder joints.[2–4]

A lot of research has been done on electromigration of solder joints. However, only a few studies have been focused on the measurement of fundamental electromigration parameters of solder. Liu *et al.* found that the dominant diffusion species was Sn atoms in a thin SnPb stripe when stressed at room temperature.[5] Huynh *et al.* conducted another electromigration study at 150 °C using V-groove samples, and found that Pb atoms were the dominant diffusion species.[6] Yeh *et al.* used Blech structure to measure the threshold current density.[7] However, one of the fundamental parameters of electromigration, the critical length, has not been measured experimentally. The critical length represents the stripe length below which there was no electromigration damage due to balanced back stress.[8] The critical length for the Al and Cu lines has been investigated, from which an very important parameter, critical product, can be obtained.[8,9] The critical length of solder has not been measured because it is very difficult to prepare short solder stripes. In this letter, we report a technique that is capable of fabricating solder stripes with various lengths down to a few microns. Therefore, the critical length for solder can be obtained experimentally.

In general, the mass transport by electromigration in Blech specimens is governed by the following equation:[8,10]

$$J=\frac{CD}{kT}Z^*eE-\frac{CD}{kT}\frac{d\sigma\Omega}{dx}, \tag{1}$$

where J is the net electromigration flux, C is the atomic concentration per unit volume, D is the diffusivity, Z^* is the effective charge number, E is the electric field, k is Boltzmann's constant, T is the absolute temperature, σ is the hydrostatic stress in the metal, and Ω is the atomic volume. The first term on the right-hand side of the equation represents the flux due to electromigration, whereas the second term stands for the opposite flux due to back stress.[10] Under the same current density, the shorter the stripe is, the higher the back stress will be. Back stress increases with decreasing stripe length due to higher stress gradient. At the critical length, the stress balances with the wind force, and thus there is no net electromigration flux. If we assume that $-d\sigma/dx$ is equal to σ_c/L_c, the critical length can thus be expressed as

$$L_c=\frac{\sigma_c\Omega}{Z^*eE}=\frac{\sigma_c\Omega}{Z^*ej\rho}, \tag{2}$$

where σ_c is the stress at the critical length, L_c is the critical length, j is the applied current density, and ρ is the resistivity of the stripe.

To investigate the critical length of solder, short Blech stripes down to a few micrometers need to be fabricated. We have reported a technique for fabricating solder Blech stripes of 370 μm long in a Si trench.[7] Nevertheless, it is quite challenging to fabricate short solder stripes because it is very difficult to reflow the solder on underbump metallization (UBM) of less than 20 μm long. In addition, the thickness of the solder stripe was not uniform at both ends, since the two ends were thinner due to reflow and polishing process. To overcome these problems, focus ion beam (FIB) was employed to fabricate short stripes from the 370-μm-long solder stripe. Figure 1(a) shows the SnPb stripe of 370 μm long fabricated using our previous approach. The stripe was 80 μm wide and 2.1 μm thick. FIB was used to etch away part of the stripe, and desired lengths of solder stripes can thus be fabricated on a Blech specimen. Figure 1(b) shows the stripes with abrupt edges fabricated by the above technique. The FIB etched away three solder slices of 80 $\times10$ μm^2 at the desired positions. Various lengths, including 10, 30, 100, and 200 μm, can be fabricated on a Blech specimen. Figure 1(c) shows the tilt-view scanning electron microscopy (SEM) image for one of the surfaces after the FIB etching. The solder layer was almost etched away and it became discontinuous. The intermetallic compounds (IMCs) below the solder were also etched slightly, but it was still continuous. They might not migrate during the electromigration test, because Cu_6Sn_5 and Cu_3Sn IMCs have higher melting point and higher elastic modulus. They were expected to

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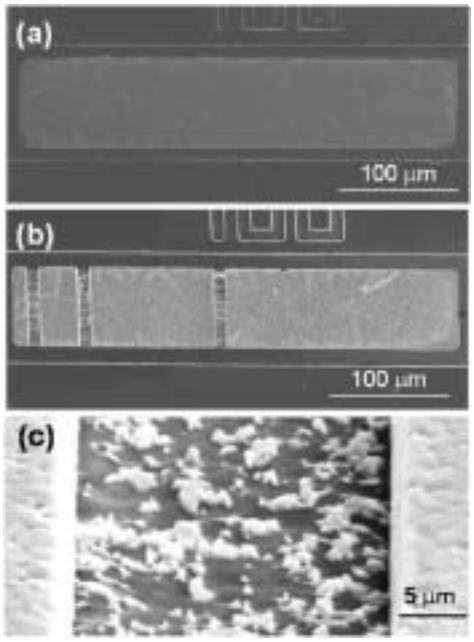

FIG. 1. (a) Plan-view SEM image for the fabricated solder Blech specimen of 370 μm long. (b) Plan-view SEM image for a solder Blech specimen after FIB etching. Solder stripes of 30, 100, and 200 μm long were fabricated. (c) Tilt-view SEM image showing the surface after FIB etching. Solder stripe became discontinued after etching.

have better electromigration resistance. The etching depth was controlled so that the Ti film remained intact, and thus it was able to carry the stressing current. Since the remaining solder/IMC on the etched surface became isolated, and their length might be shorter than the critical length of solder and IMC, they did not migrate during current stressing, thus affecting the electromigration behavior of the neighboring solder stripes. The sample was annealed at 150 °C for 5 h prior to electromigration testing to remove the damage in the solder caused by FIB etching.

Figure 2 shows the cross-sectional schematic for the solder stripes in Fig. 1(b). The IMC was about 0.8 μm thick, and the SnPb solder was about 1.3 μm thick. There was a 400 nm Cu metallization layer on a 120 nm Ti film before the reflow process, and it was almost consumed after the reflow process. Thus, there was almost no additional IMC formation during electromigration testing. Because the solder was thinner on both ends of the solder stripe in Fig. 1(a), the electromigration behavior for the solder stripe on the far left was not considered. During electromigration test, a constant current was applied through the pads on the two ends. There was around 80% of the applied current drifting in the solder strip, 19% in the IMC layer, and only 1% in the Ti layer.

Critical length of the solder stripe could be determined using these short strips. Figure 3(a) shows the same specimen in Fig. 1(b) after stressing by the current density of 5×10^4 A/cm^2 at 100 °C for 104 h. It is found that electromigration occurred in the three solder stripes of 30, 100, and 150 μm long. In addition, the longer the stripe is, the higher the electromigration rate will be. Length-dependent electromigration behavior was also observed on the solder stripes, which means that there may be back stress in the solder stripe under stressing. The critical length is below 30 μm from these results. To further explore the critical length, shorter solder stripes of 5, 10, 15, 20, and 30 μm long were fabricated, as shown in Fig. 4(a). Lower current density of 2×10^4 A/cm^2 was used in order to determine the critical length more precisely. After the stressing condition at 100 °C for 490 h, electromigration occurred in the stripes longer than 15 μm as indicated by the arrows in Fig. 4(b), yet no depletion was observed in those of 5 and 10 μm long, as shown in the figure. Therefore, the critical length for eutectic SnPb solder was determined to range between 10 and 15 μm. The corresponding critical product was between 20 and 30 A/cm.

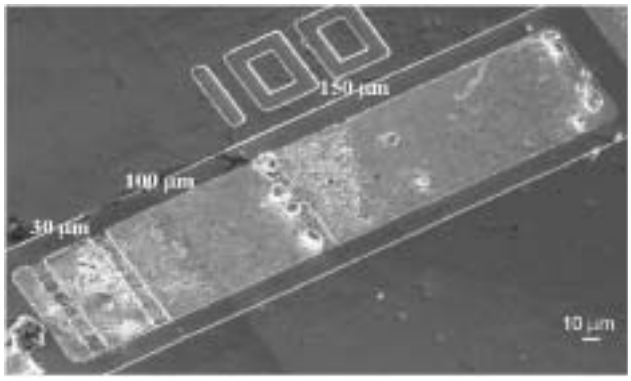

FIG. 3. Tilt-view SEM image showing the solder stripes in Fig. 1(b) after current stressing of 5×10^4 A/cm^2 at 100 °C for 104 h. Depletion occurred for all solder stripes, and it was larger for longer solder stripes.

To examine whether the measured critical length is reasonable, the theoretical value in Eq. (2) was estimated. We take the critical compressive stress in the anode end of the SnPb solder stripe to be the yield strength of solder, which is 27.2 MPa. Wang *et al.* reported that the stress gradient is linear in an Al stripe of 200 μm long,[11] therefore, it is assumed that the gradient in the solder stripe behaves linearly. If we assume that the tensile stress in the cathode end is also 27.2 MPa, the stress difference between the anode side and cathode side will be 54.4 MPa. In addition, Z^*, Ω, and ρ are taken to be 30, 2.78×10^{-23} cm^3, and 14.5×10^{-6} Ω cm, respectively. By substituting all the parameters in Eq. (2), the critical length is estimated to be 11 μm under the current density of 2×10^4 A/cm^2, which is quite close to our experi-

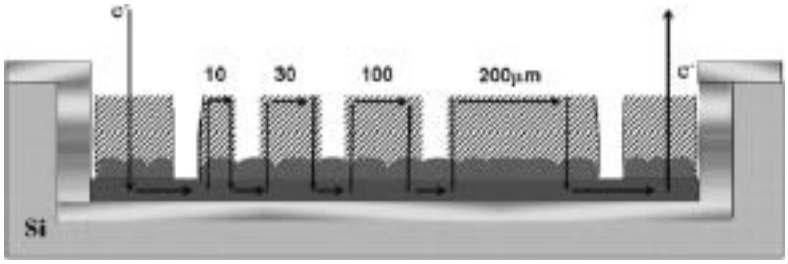

FIG. 2. Cross-sectional schematic of the solder stripe inside a Si trench. The solder layer and the IMC layer were about 1.3 and 0.8 μm thick, respectively.

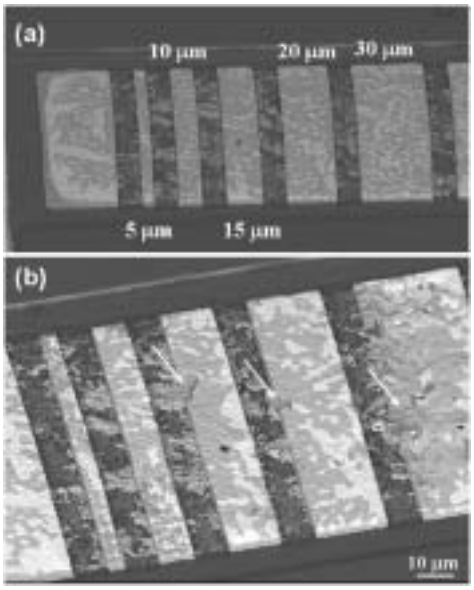

FIG. 4. (a) Back-scattered SEM image showing another solder Blech specimen with stripes of 5, 10, 15, 20, and 30 μm long before current stressing. (b) The same specimen in (a) after current stressing of 2×10^4 A/cm^2 at 100 °C for 490 h. No depletion was found for the 5 and 10 μm stripes.

mental value. The corresponding value of critical product is 22 A/cm.

It is estimated that the current density required to cause failure in a solder joint is about two orders of magnitude less than that needed for an Al or Cu line to fail.[3] Electromigration in a flip-chip solder joint occurs at lower current density because of the high lattice diffusivity in the solder alloys, together with higher resistivity, lower Young's modulus, and higher effective charge number of the chemical elements in solder alloys than those of Al or Cu. The critical product is 1260 A/cm for a 115 μm Al stripe at 350 °C,[8] whereas it is 3700 A/cm at 340–400 °C for dual-damascene Cu/oxide interconnects.[9] These values are about 50–150 times larger than those obtained in our experiment. Therefore, the critical product we measured is quite reasonable.

Significant phase redistribution was observed after current stressing for stripes longer than 15 μm, as shown in Fig. 4. The Pb-rich phase migrated toward the anode end, and thus Pb atoms were found to be the dominate diffusion species at 100 °C. This phase redistribution may have effect on the back stress. In addition, after stressing for a long time, the Pb-rich phase accumulated on the anode end, leaving the Sn-rich phase on the cathode end. This redistribution also affects the yield stresses on the cathode and the anode ends. Further study is needed to address these issues.

In conclusion, eutectic SnPb solder stripes of various lengths have been fabricated using FIB. It is found that no electromigration damage occurred for the 5 and 10 μm stripes under stressing by the current density of 2×10^4 A/cm^2 at 100 °C for 490 h, whereas length-dependent electromigration behavior was observed for longer stripes. The critical length was between 10 and 15 μm, which is quite close to the theoretical value of 11 μm. The corresponding critical product was between 20 and 30 A/cm, which is approximately two orders of magnitude smaller than that of the dual-damascene Cu/oxide interconnects.

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[1] J. H. Lau, *Flip Chip Technology* (McGraw-Hill, New York, 1995), p. 123.
[2] *International Technology Roadmap for Semiconductors* (Semiconductor Industry Association, San Jose, CA, 2003), Assembly and Packaging Section, pp. 4–9.
[3] K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[4] C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
[5] C. Y. Liu, Chih Chen, and K. N. Tu, J. Appl. Phys. **88**, 5703 (2000).
[6] Q. T. Huynh, C. Y. Liu, Chih Chen, and K. N. Tu, J. Appl. Phys. **89**, 4332 (2001).
[7] Y. T. Yeh, C. K. Chou, Y. C. Hsu, Chih Chen, and K. N. Tu, Appl. Phys. Lett. **86**, 203504 (2005).
[8] I. A. Blech, J. Appl. Phys. **47**, 1203 (1976).
[9] E. T. Ogawa, A. J. Bierwag, K. D. Lee, H. Matsuhashi, P. R. Justison, A. N. Ramamurthi, and P. S. Ho, Appl. Phys. Lett. **78**, 2652 (2001).
[10] I. A. Blech, Acta Mater. **46**, 3717 (1998).
[11] P. C. Wang, G. S. Cargill, I. C. Noyan, and C. K. Hu, Appl. Phys. Lett. **72**, 1296 (1998).

Study of void formation due to electromigration in flip-chip solder joints using Kelvin bump probes

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Kelvin bump probes were fabricated in flip-chip solder joints, and they were employed to monitor the void formation during electromigration. We found that voids started to form at approximately 5% of the failure time under 0.8 A at 150 °C, and the bump resistance increased only 0.02 mΩ in the initial stage of void formation. Three-dimensional simulation was performed to examine the increase in bump resistance at different stages of void formation, and it fitted the experimental results quite well. This technique provides a systematic way for investigating the void formation during electromigration. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2226989]

Electromigration in flip-chip solder joints has become an important reliability issue due to the high-density and high-performance requirements,[1,2] and it has been studied extensively in recent years.[3–7] The current-crowding-induced voiding on the cathode/chip side was proposed to be responsible for the failure at the cathode/chip side of the solder joints.[2,4,5] For Al and Cu interconnects, void nucleation and propagation during electromigration are monitored by the change in resistance.[8–10] In addition, Kelvin probes have long been employed to measure via or contact resistance in the interconnects.[11–13] With the aid of Kelvin probes, via or contact resistance can be monitored to investigate the initial stage of void formation or microstructure change in the via or in the contact. In previous electromigration studies of flip-chip solder joints, daisy-chain structures were used to monitor the change in resistance. Nevertheless, the resistance of a solder bump was estimated in the order of a few milliohms, whereas the resistance of the metallization trace ranges from a few hundred to a few ohms, depending on its dimension. Thus, the bump resistance is quite small compared with the resistance of the metallization traces,[14] and the daisy-chain structure cannot detect the slight changes in resistance due to void formation in the solder joint. Kelvin probes have recently been implemented in flip-chip solder joints for electromigration study.[15,16] However, void nucleation and propagation as well as the change in bump resistance due to void formation remain unclear.

In this study, we used Kelvin bump probes to monitor the change in bump resistance during electromigration. It was found that a change in bump resistance as small as 0.01 mΩ could be detected. The increase in bump resistance due to void formation can be examined at different stages. Three-dimensional (3D) finite element modeling was also performed to simulate the increase in bump resistance due to void formation. This approach facilitates the systematic study of void formation due to electromigration in flip-chip solder joints.

We have designed and fabricated Kelvin probes for flip-chip eutectic SnPb solder joints. Figure 1(a) shows the cross-sectional schematic for the structure. The test structure consisted of four bumps, which were connected by an Al trace. The four bumps were labeled bump 1–bump 4. The Al trace was 1.5 μm thick and 100 μm wide. The pitch for the solder joints was 1 mm. Six Cu lines on the FR4 substrate were connected to the four bumps, and they were labeled as nodes 1–6, as shown in the figure. The Cu lines were 30 μm thick and 100 μm wide. With these six Cu lines, various experimental setups can be performed to measure the bump resistance for bump 2 or bump 3, or the resistance for the middle segment of the Al trace. In this study, current was applied through nodes 3 and 4, i.e., electrons flowing from the chip side to the substrate side for bump 3, and the opposite direction for bump 2, as illustrated in Fig. 1(a). The voltage change in bump 2 was monitored through nodes 1 and 2, whereas the voltage change in bump 3 was monitored through nodes 5 and 6. Therefore, the change in bump resistance during electromigration for the two bumps with opposite direction of electron flow can be monitored simultaneously. In general, void is formed in the chip side of bump 3 due to the serious current crowding effect.[2] Hence, we will present the results only for bump 3 in this letter. The power supply used in this measurement was a Keithley 2400, which has a 0.1 μV resolution in voltage measurement. The error in measuring resistance in this study was estimated to be 1–10 $\mu\Omega$.

The schematic structure of the flip-chip bumps used in this study is shown in Fig. 1(b). The underbump metalliza-

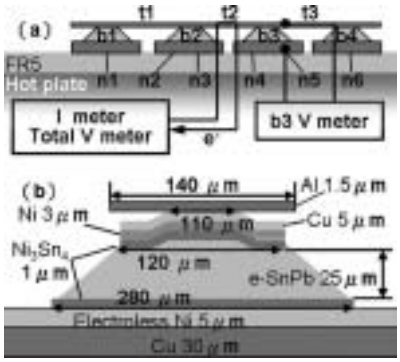

FIG. 1. (a) Cross-sectional schematic of the layout design. The Al trace connected all the four solder bumps together. (b) Schematic structure for the solder bump used in this study.

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TABLE I. The properties of materials used in the simulation models.

Materials	Al	Cu	Ni	Ni_3Sn_4	Eutectic SnPb	Electroless Ni
Resistivity	3.2	1.7	6.8	28.5	14.6	70 $\mu\Omega$ □ cm

tions (UBM) was 0.5 μm Ti/0.5 μm Cu/5 μm Cu/3 μm Ni. The Ti layer and the 0.5 μm Cu seed layer were sputtered, whereas the 5 μm Cu and the 3 μm Ni layers were electroplated. The passivation and UBM openings were 110 and 125 μm in diameter, respectively. Eutectic SnPb solder was used for the joint. The dimension of the pad opening was 280 μm in diameter. Owing to the large opening in the substrate side, the bump height was as small as 25 μm. Our previous simulation results showed that current crowding effect occurred within 20 μm depth in solder bump near the entrance of the electron flows on the chip side.[17] Therefore, it is expected that mechanism of void formation for these low-bump-height joints should be quite similar to those with normal bump height of about 100 μm.

3D simulation was performed to examine the change in bump resistance due to void formation. The morphology of Ni_3Sn_4 intermetallic compound (IMC) was assumed to be of layered type with uniform thickness of 1.0 μm, as shown in Fig. 1(b). The resistivity values of the materials used in this simulation are listed in Table I. ANSYS simulation software was employed and the model used in this study was SOLID5 eight-node hexahedral coupled field element.

The increase in bump resistance during electromigration can be precisely measured using Kelvin bump probes, and it can be employed to monitor the void formation and microstructure change during electromigration. Figure 2(a) shows the total resistance for the stressing circuit as a function of stressing time up to failure when powered by 0.8 A at 150 °C. The initial resistance was 1.77 Ω, and no obvious increase in resistance could be observed until 90% of the stressing time. Yet, the enlarged curve up to 80% of the failure time shows that the total resistance decreased initially, and then increased with stressing time, as illustrated in the inset of Fig. 2(a). The decrease in total resistance may be attributed to the reduction in contact resistance of the whole stressing circuit. The total resistance increased about 30 mΩ after stressing for 80% of the failure time. This resistance increase may be mainly due to the degradation or oxidation of Cu lines in the FR4 substrate and of the Cu wires used to connect the package to the power supply during current stressing, since no obvious resistance increase was detected in the Al trace between bumps 2 and 3. In addition, the noise of the resistance curve was about 5–10 mΩ. The noise may be mainly attributed to the temperature coefficient of resistance (TCR). If we take the average TCR value for the stressing circuit to be 4×10^{-3} K^{-1}, the fluctuation in resistance in the stressing circuit would be 7 mΩ/deg. However, the bump resistance measured by Kelvin bump probes showed a different behavior. This can be seen in Fig. 2(b), which shows the measured resistance of bump 3 up to failure. The initial bump resistance was only 0.6 mΩ. As the stressing time increased, the bump resistance continued to increase slowly up to 80% of failure time, and the bump failed when the resistance rose abruptly at around 756.6 h. The inset in Fig. 2(b) shows the data in 2(b) up to 80% of the stressing time. The bump resistance started to increase after 20 h. The time for the resistance to reach 1.03 times of the initial value

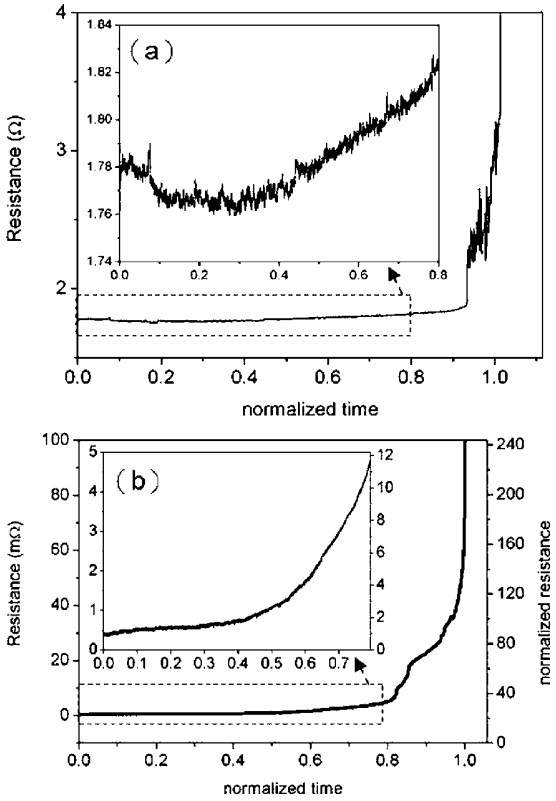

FIG. 2. (a) The total resistance as a function of normalized stressing time. The inset shows the change in resistance up to 80% of the failure time. (b) The bump resistance measured as a function of normalized stressing time up to failure. The inset shows the data up to 80% of the failure time.

was 29.8 h, which was 4% of the failure time. Voids may start to form at this stage, and we will discuss this point below. In contrast to the results from the daisy-chain structure, this technique can detect the subtle change in bump resistance. This is because the total resistance of the daisy-chain circuit was in the order of several ohms and noise in resistance due to TCR effect was over 7 mΩ,[2] whereas the increase in resistance in the initial stage of void formation is less than 1 mΩ. Therefore, the noise in the total resistance makes it difficult for the daisy-chain structure to detect the slight change in resistance due to void formation.

The initial bump resistance was only 0.6 mΩ measured at 0.8 A at 150 °C, which was much lower than expected. Two reasons may be responsible for this low bump resistance. First, the bump height was only 25 μm, which was about a quarter of the typical value. Second, the Kelvin probes for measuring voltage drop were located in a low current density region of the Al pad. Our previous 3D simulation showed that the current did not spread uniformly in the UBM opening, instead the current crowded into the solder bump in a small volume near the entrance point of the Al trace.[17] Since only a small amount of the current passed through the opposite end of the entrance point of the current, the voltage drop measured by the Kelvin probes was lower than expected.

The Kelvin probes can detect different stages of void formation and propagation, and Figs. 3(a)–3(c) show the void formation at different stages. Figure 3(a) shows the cross-sectional scanning electron microscope (SEM) image for the bump before current stressing, while Fig. 3(b) shows the SEM image for another bump stressed by 0.8 A at

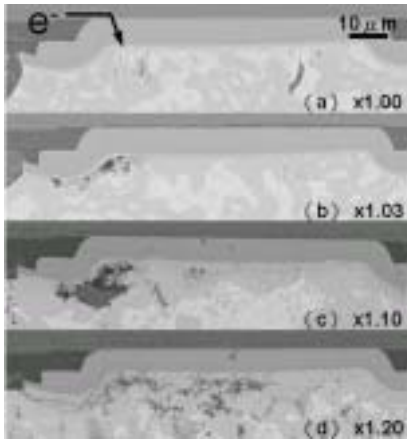

FIG. 3. (a) Cross-sectional SEM image for the bump before current stressing; cross-sectional SEM image for the bump stressed by 0.8 A at 150 °C for (b) 29.8 h and (c) 101.5 h.

150 °C for 29.8 h. The bump resistance increased from 0.60 to 0.62 mΩ after the current stressing, which is an increase of 1.03 times the initial value. The direction of the electron flow is indicated by the arrow in the figure. This condition is denoted as stage I in this letter. Small voids started to form under the IMC layer in the left corner of the passivation opening, where current crowding occurred most seriously. Owing to the slower IMC formation rate between Ni and Sn, no clear IMC formation was observed in the initial stage. Another bump was stressed at the same condition for 101.0 h, and the current was terminated when the bump resistance reached 1.10 times the initial value. The cross-section image is shown in Fig. 3(c), which shows larger voids at the interface of the solder and the IMC. This condition is denoted as stage II. Under the stressing conditions, voids started to form at approximately 5% of the failure time, and they grew for the rest of the stressing time. The incubation time for void formation is relatively short compared with the failure time. This may be attributed to the fact that the cross section of the UBM opening is quite large, and thus it takes time for the voids to propagate and deplete the UBM opening.

To investigate the change in bump resistance due to void formation, 3D modeling was performed to simulate the voltage distribution in the solder joint. Figure 4(a) shows the voltage distribution in the solder joint without void formation when 0.2 A was applied. The voltage drop on the right-hand side was much smaller than that on the left-hand side, resulting in the low bump resistance of about 0.5 mΩ measured by the Kelvin probes. The simulated voltage drop across the right-hand side of the solder was 0.002 mV, and thus the corresponding bump resistance was 0.4 mΩ, which is close to the experimental values. Figure 4(b) illustrates the voltage distribution in the solder joint for stage I when a small void is formed near the entrance of the Al trace on the left-hand side. The void depleted about 8% of the UBM opening. The bump resistance increased only 0.02 mΩ, which is about 1.04 times of the initial value. As the void grew bigger, the available cross section for conducting current became smaller and more current drifted to the right-hand side of the bump, resulting in the increased bump resistance, as shown in Figs. 4(c). The bump resistance increased to 1.11 times its initial value for stage II. The experimental and simulation results for the two stages show good agreement.

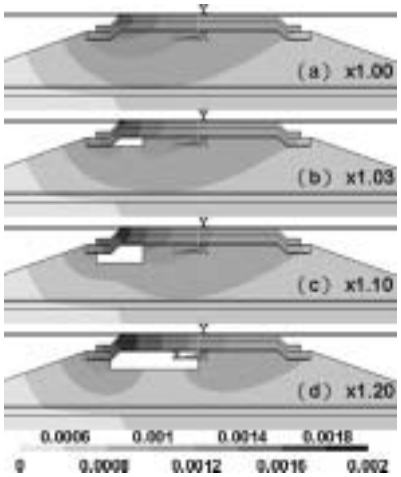

FIG. 4. (a) Simulation results showing the voltage distribution in the solder joint when 0.2 A was applied (a) without void formation, and then after the void formed (b) at stage I and (c) at stage II.

In summary, the Kelvin probes appear to be very sensitive to void formation and propagation, so they can detect the different stages of void formation during electromigration. Therefore, they can be employed to investigate the electromigration behavior systematically.

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[1]International Technology Roadmap for Semiconductors (Semiconductor Industry Association, San Jose, CA, 2003).
[2]K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
[3]C. Y. Liu, Chih Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
[4]Everett C. C. Yeh, W. J. Choi, K. N. Tu, Peter Elenius, and Haluk Balkan, Appl. Phys. Lett. **80**, 580 (2002).
[5]J. W. Nah, K. W. Paik, J. O. Suh, and K. N. Tu, J. Appl. Phys. **94**, 7560 (2003).
[6]Hua Ye, Cemal Basaran, and Douglas Hopkins, Appl. Phys. Lett. **82**, 7 (2003).
[7]T. Y. Lee, D. R. Frear, and K. N. Tu, J. Appl. Phys. **90**, 4502 (2001).
[8]C. K. Hu, M. B. Small, K. P. Rodbell, C. Stanis, P. Blauner, and P. S. Ho, Appl. Phys. Lett. **62**, 1023 (1993).
[9]C. K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Domenicucci, X. Chen, and A. K. Stamper, Appl. Phys. Lett. **81**, 1782 (2002).
[10]P. S. Ho and T. Kwok, Rep. Prog. Phys. **52**, 301, 1989.
[11]S. L. Zhang, M. Ostling, H. Norstrom, and T. Arnborg, IEEE Trans. Electron Devices **41**, 1414 (1994).
[12]W. M. Loh, K. Saraswat, and R. W. Dutton, IEEE Electron Device Lett. **EDL-6**, 105 (1985).
[13]M. Natan, S. Purushothan, and R. Dobrowski, J. Appl. Phys. **53**, 5776 (1982).
[14]T. L. Shao, S. H. Chiu, Chih Chen, D. J. Yao, and C. Y. Hsu, J. Electron. Mater. **33**, 1350 (2004).
[15]S. N. Gee, N. Kelkar, J. Huang, and K. N. Tu, Proceedings of IPACK 2005 ASME InterPACK, San Francisco, CA (unpublished).
[16]B. Ebersberger, R. Bauer, and L. Alexa, *Proceeding of Electronic Components and Technology Conference*, IEEE Components, Packaging, and Manufacturing Technology Society, Lake Buena Vista, FL (IEEE, New York, 2005), p. 1407.
[17]T. L. Shao, Shih-Wei Liang, T. C. Lin, and Chih Chen, J. Appl. Phys. **98**, 044509 (2005).

Relieving the current crowding effect in flip-chip solder joints during current stressing

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Three-dimensional simulations for relieving the current crowding effect in solder joints under current stressing were carried out using the finite element method. Three possible approaches were examined in this study, including varying the size of the passivation opening, increasing the thickness of Cu underbump metallization (UBM), and adopting or inserting a thin highly resistive UBM layer. It was found that the current crowding effect in the solder bump could be successfully relieved with the thick Cu UBM or with the highly resistive UBM. Compared to the solder joint with Al/Ni(V)/Cu UBM, for instance, the maximum current density in a solder bump decreased dramatically by a factor of fifteen, say from 1.11×10^5 A/cm^2 to 7.54×10^3 A/cm^2 when a 20-μm-thick Cu UBM was used. It could be lowered by a factor of seven, say to 1.55×10^4 A/cm^2, when a 0.7-μm UBM of 14770 μΩ cm was adopted. It is worth noting that although a resistive UBM layer was used, the penalty on overall resistance increase was negligible because the total resistance was dominated by the Al trace instead of the solder bump. Thermal simulation showed that the average temperature increase due to Joule heating effect was only 2.8 °C when the solder joints with UBM of 14770 μΩ cm were applied by 0.2 A.

I. INTRODUCTION

The flip-chip solder joint has become the most important technology of high-density packaging in the microelectronics industry.[1] Thousands of solder bumps can be fabricated into one chip. To meet performance requirements, the input/output (I/O) numbers keep increasing, and the size of the joints progressively shrinks. Their diameter is about 100 μm or less.[2] The design rule of packaging requires that each bump is to carry 0.2–0.4 A, resulting in a current density of approximately 2×10^3 to 2×10^4 A/cm^2. Therefore, electromigration has become an important reliability issue for flip-chip solder joints.[3–5]

In this work, current density distribution in a solder joint was thoroughly studied by a three-dimensional finite element simulation. It was found that the maximum current density in a solder bump can be much higher than the average one that was previously projected. It locates itself near the solder/underbump metallization (UBM) interface, which serves as a vacancy flux divergence plane and favors electromigration occurring at that location. Consequently, the solder joint is more prone to electromigration. The cause of such locally high current density is a result of the current crowding effect. Current crowding occurring in the solder joints is due to the current flow experiencing a dramatic geometrical and resistance transition from the thin on-chip metal line to the solder bump. Because the cross-section of the Al trace on the chip side is about two orders smaller than that of the solder joints, the majority of the current will tend to gather near the Al/UBM entrance point to enter the solder bump instead of spreading uniformly across the opening before entering the bump. The materials near the entrance point experience a current density of about one order of magnitude higher than the average value. The materials included a bump metallization (UBM), intermetallic compound (IMC), and solder, where the

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solder has high lattice diffusivity, higher resistivity, lower Young's modulus, and a higher effective charge number than the other two materials.[3,6–9] Therefore, the current crowding effect enhances the possibility of voids forming in the solder near the entrance and then propagating to cause electromigration failure. Current crowding

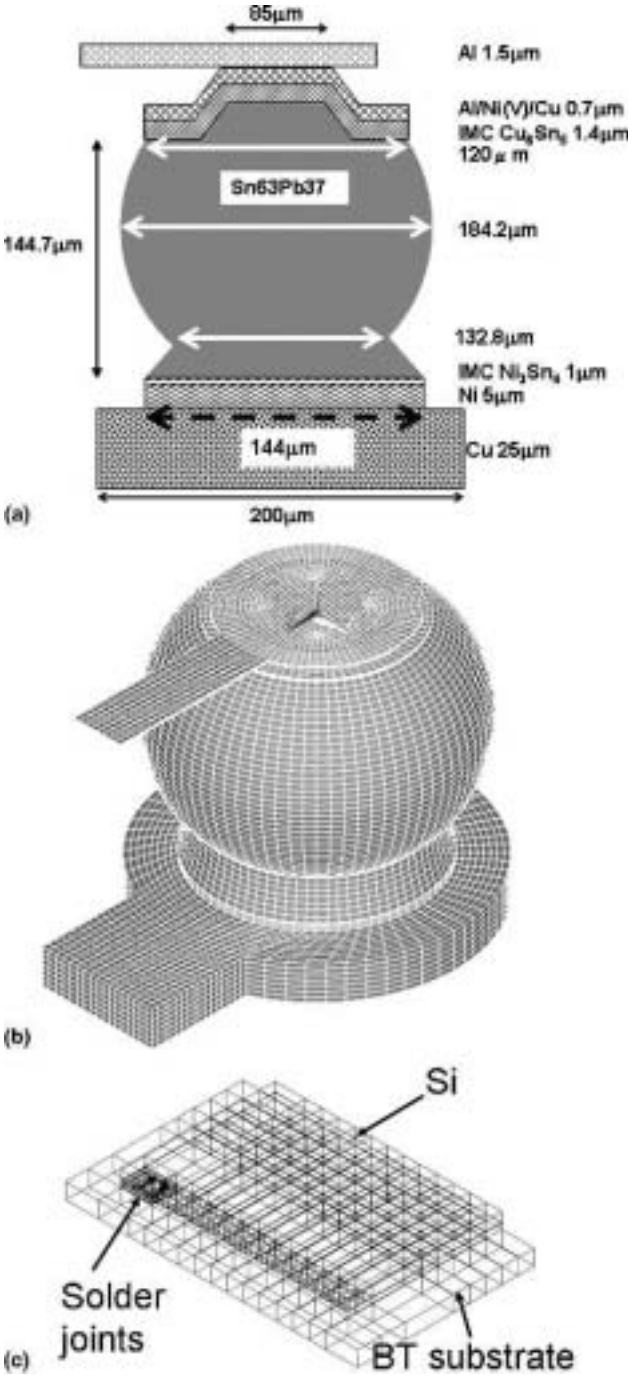

FIG. 1. (a) Schematic diagrams of the solder joint with Al Ni(V)/Cu UBM used in this study. (b) Three-dimensional view of the model in (a) with meshes contained in it.

TABLE I. Properties of materials used in the simulation models.

Material	Thermal conductivity (W/m °C)	Resistivity (μΩ cm)
Silicon(chip)	147.0	···
Al trace	238.0	3.2
UBM(Ti + Cr/Cu + Cu)	147.6	18.8
Eutectic SnPb	34.1	14.6
Ni	70.0	6.8
Cu pad	403.0	1.7
BT (substrate)	0.7	···
Underfill	0.55	···
Polyimide	0.26	···
Ni(V)	71.4	63.2

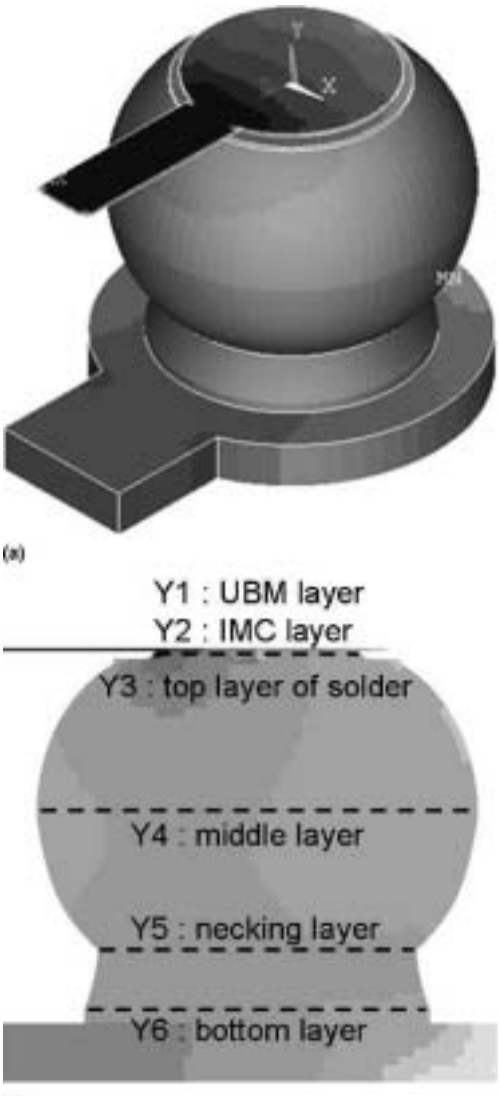

FIG. 2. Current density distribution in the solder joint with Al Ni(V)/Cu UBM when powered by 0.567 A. (b) Cross-sectional view along the Z-axis of (a). Current crowding occurs in the entrance of the Al trace. The dotted lines show the six cross-sections examined in this study.

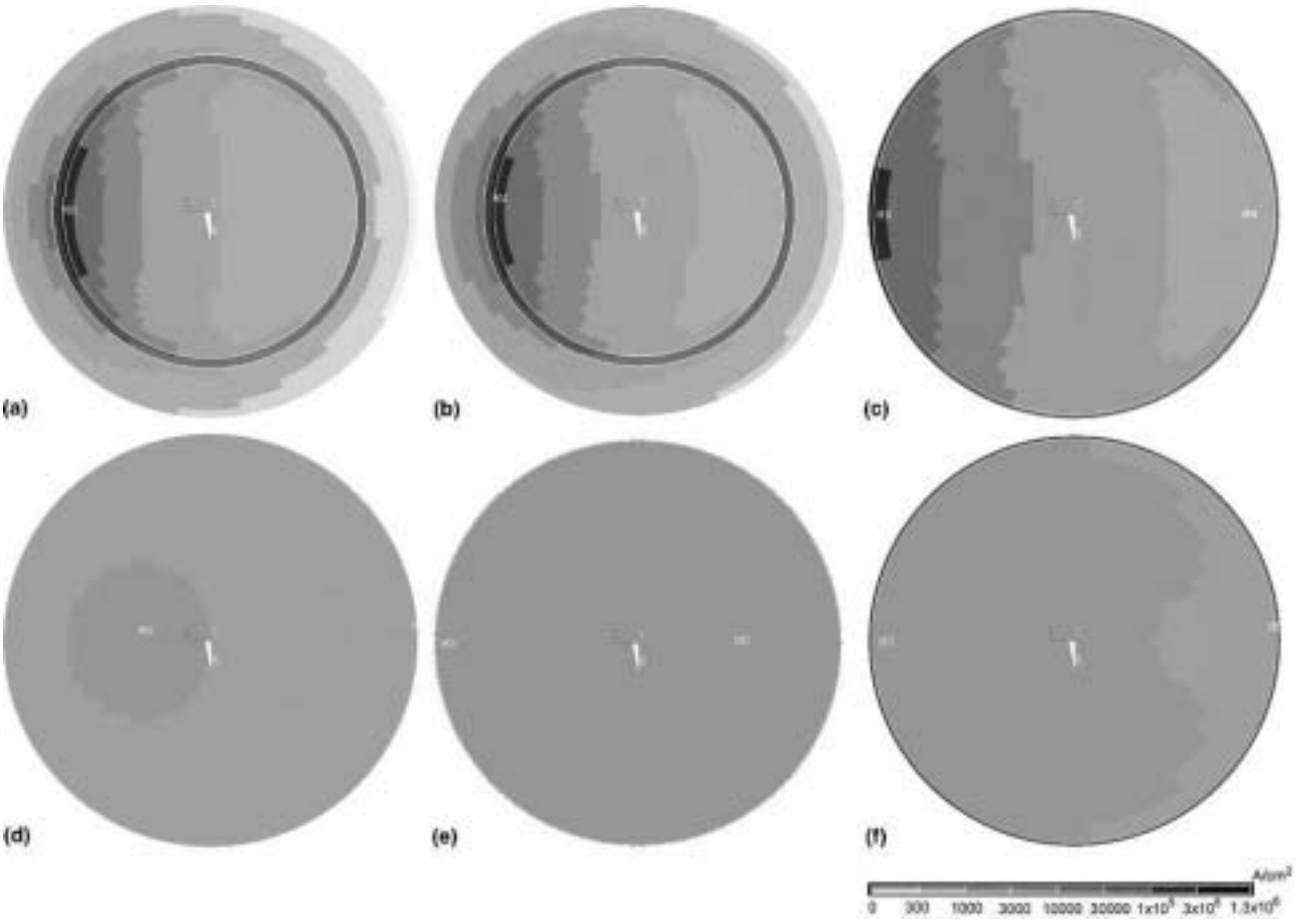

FIG. 3. Current density distribution in the different cross-sections: (a) cross-section Y1, located inside the UBM; (b) cross-section Y2, the IMC layer between the UBM and the solder; (c) cross-section Y3, the top layer of the solder connected to the IMC; (d) cross-section Y4, which has the largest diameter in the joint; (e) cross-section Y5, which has a smaller diameter due to the solder mask process; (f) cross-section Y6, which is situated at the bottom of the solder joint.

plays a critical role in the electromigration failure of the solder joints.[10]

Hence, increasing the electromigration resistance of the joints is an important and urgent issue. There are two approaches to increasing electromigration resistance: first, using a solder alloy that has better electromigration resistance; second, relieving the current crowding effect in solder joints by proper circuit or UBM design. For the former approach, Wu et al. developed a Pb-free solder alloy that has excellent electromigration resistance, close to that of the high-Pb solder.[11] For the latter approach, it is expected that relieving the current crowding effect in solder joints would retard the formation rate of the voids and thus would increase the lifetime of the solder joints. However, no literature related to this issue has been reported so far. For this paper, we used finite element analysis to simulate the current density distribution of the solder joints with various structures of flip-chip solder joints. Possible solutions for the relieving current crowding effect will be proposed.

TABLE II. Maximum current density and crowding ratios at different cross sections for the solder joint with the Al/Ni(V)/Cu thin film UBM.

Method		Cross section					
		Y1, UBM layer	Y2, IMC layer	Y3, top layer of solder	Y4, middle layer of solder	Y5, necking layer of solder	Y6, bottom layer of solder
Standard	Maximum	2.09×10^5	1.81×10^5	1.11×10^5	3.45×10^3	7.55×10^3	5.91×10^3
	Ratio	41.9	36.2	22.2	0.7	1.5	1.2

II. SIMULATION

The simulation model used in this study is schematically shown in Fig. 1(a). Throughout this text, it will be denoted as the standard model. A thin film UBM of 0.4-μm Al/0.3-μm Ni(V)/0.4-μm Cu was adopted for the chip side, and Ni metallization was used on the substrate side. Eutectic SnPb solder was adopted for the bump materials. The Cu layer in the UBM was assumed to be completely consumed to form 1.4 μm Cu_6Sn_5 IMC. Therefore, an effective layer of 0.7-μm UBM with an effective resistivity of 29.54 μΩ cm was used in the simulation model. On the substrate side, we assumed that 1 μm Ni_3Sn_4 IMC was formed in the interface of the solder and the Ni metallization. Both Cu_6Sn_5 and Ni_3Sn_4 IMCs were assumed to be the layered-type. The resistivity and thermal conductivity values of the materials used in this simulation are listed in Table I. The model used in this study was SOLID69 8-node hexahedral coupled field element using Ansys simulation software (Ansys Inc., PA). For thermal simulation, we used an infrared microscope to measure the temperature in the solder bumps during current stressing[12] and then adjusted the simulation parameters so that the simulated temperature in the solder matched the one measured by the infrared microscope under the same applied current. The three-dimensional (3D) schematic solder joint with meshes is shown in Fig. 1(b). The dimension of the mesh was 3.8 μm. The passivation and UBM openings are 85 and 120 μm in diameter, respectively. The contact opening on the substrate is 144 μm in diameter. The dimension of the Al trace is 34 μm wide and 1.5 μm thick, whereas the Cu line on the substrate side is 80 μm wide and 25 μm thick. A current of 0.567 A was applied from the Al trace, which drifted out of the bump from the Cu line. If one assumes the current drifts uniformly through the joint, the average current density in the Al trace was 1.11×10^6 A/cm^2, and the calculated average current densities were 5.01×10^3 and 3.48×10^3 A/cm^2 for the UBM opening of the chip side and the contact opening of the substrate side, respectively. Figure 1(c) shows the constructed model for thermal simulation, in which only two solder joints were stressed by current, as indicated by one of the arrows in the figure. The dimension of the Si chip was 7.0 × 4.8 mm and the thickness was 290 μm, whereas the dimension of the bismaleimide triazine (BT) substrate was 5.4 mm wide, 9.0 mm long, and 380 μm thick.

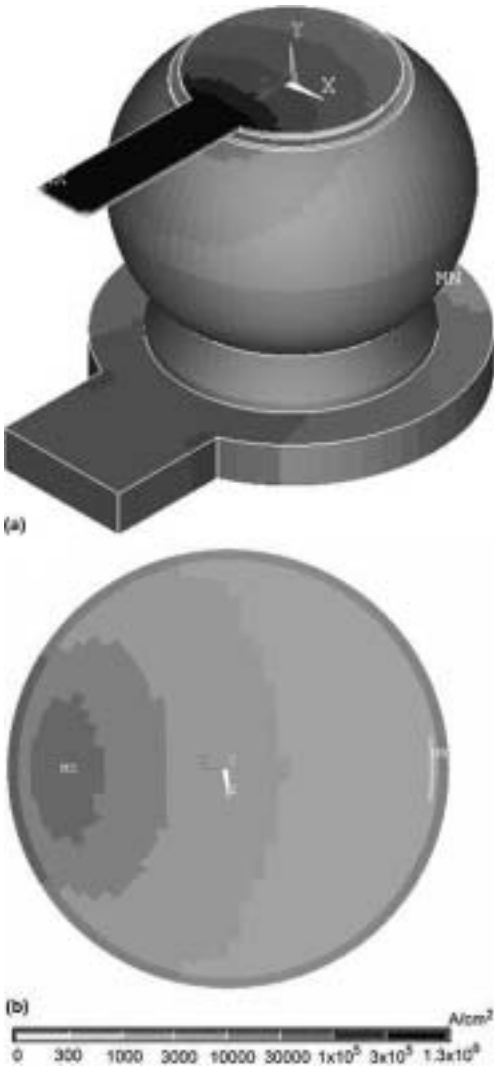

FIG. 4. (a) 3D current density distribution in the solder joint with a larger passivation opening of 100 μm in diameter. (b) Current density distribution in the top layer of the solder (cross-section Y3) in (a).

The current density distribution of the flip-chip solder joint was shown in Fig. 2(a). Current crowding is clearly observed in the vicinity of the entrance of the Al trace into the solder bump. However, it spreads out prior to reaching the half distance of the bump height, and there is no obvious current crowding at the bottom of the

TABLE III. Maximum current density and crowding ratios at different cross sections for the solder joint with larger passivation opening.

		Cross section					
Method		Y1, UBM layer	Y2, IMC layer	Y3, top layer of solder	Y4, middle layer of solder	Y5, necking layer of solder	Y6, bottom layer of solder
Passivation opening: 100 μm	Maximum	2.33×10^5	2.03×10^5	1.22×10^5	3.67×10^3	8.16×10^3	6.04×10^3
	Ratio	46.6	40.6	24.4	0.7	1.6	1.2

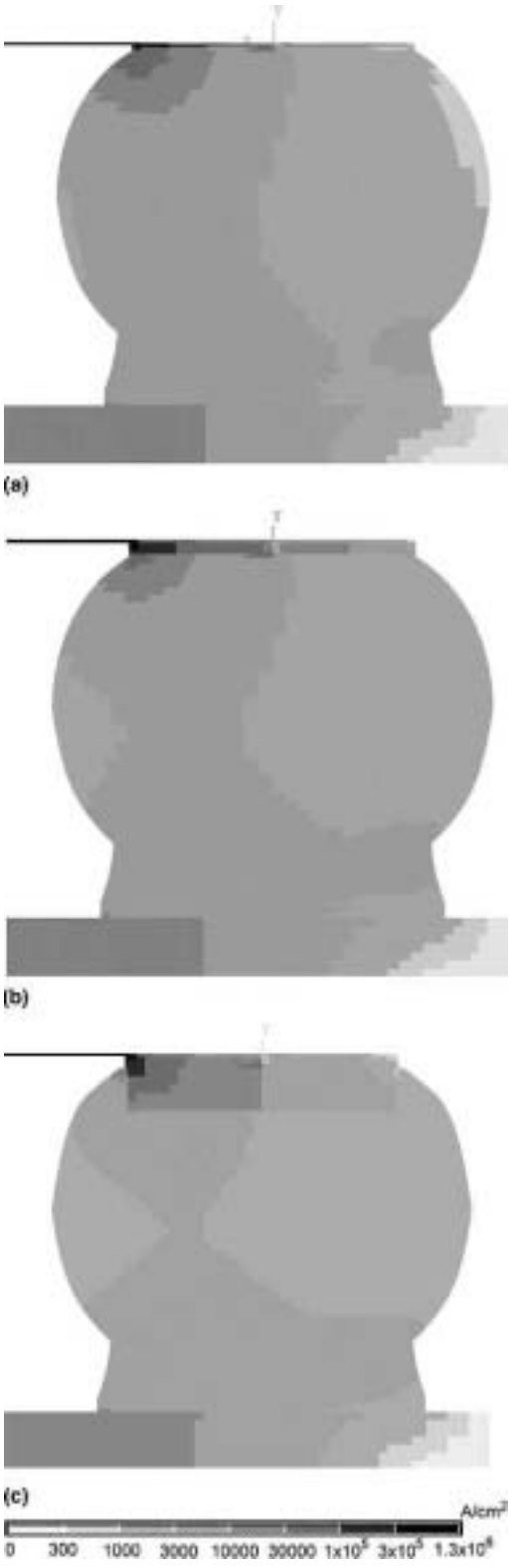

FIG. 5. Current density distribution in the cross-section along the Z axis for (a) 0.7-μm Cu UBM, (b) 5-μm Cu UBM, and (c) 20-μm Cu UBM.

solder bump. The cross-sectional view of Fig. 2(a) along the Z-axis is shown in Fig. 2(b). The current crowding effect can be clearly seen at the entrance of the Al trace. The maximum current density inside the solder is 1.11×10^5 A/cm^2. In this paper, to evaluate the current crowding effect, we denote a "crowding ratio" as the local maximum current density divided by the average current density at the UBM opening. The average current density at the UBM opening is 5.01×10^3 A/cm^2 for the standard simulation model. Therefore, the corresponding crowding ratio for the solder near the entrance is 22.2, which means that the local current density at the solder bump near the Al entrance is 22.2 times larger than the average value at the UBM opening. The larger the value is, the higher the current crowding effect.

To examine the current density distribution in various locations of the joint, six cross-sections were inspected. Their locations are shown in Fig. 2(b), in which cross-section Y1 is located inside the UBM layer, cross-section Y2 represents the IMC layer, cross-section Y3 is located in the top layer of the solder joint connecting to the IMC, and cross-section Y4 is situated near the middle of the solder joint, which has the largest cross-section 184 μm in diameter. Cross-section Y5 is situated between the middle and the bottom of the solder, which has a necking due to the necessity of there being a solder mask, and cross-section Y6 represents the bottom of the solder joint close to the Ni_3Sn_4 IMC on the substrate side.

The current density distributions at the six cross sections are shown in Figs. 3(a)–3(f). The current density distribution in the UBM layer is shown in Fig. 3(a), in which the maximum current density occurs near the Al entrance inside the passivation opening. The value reaches 2.09×10^5 A/cm^2, and its crowding ratio is as high as 41.9. For the IMC layer shown in Fig. 3(b), the maximum value is 1.81×10^5 A/cm^2, and the corresponding crowding ratio is 36.2. The maximum current density inside the solder occurs near the Al entrance inside the passivation opening, as shown in Fig. 3(c). The value reaches 1.11×10^5 A/cm^2, and its crowding ratio remains as high as 22.2. For the remaining three layers, as shown in Figs. 3(d)–3(f), current distribution became more uniform, and thus the crowding ratios for the three layers were 0.7, 1.5, and 1.2, respectively. Therefore, changing the angle between the Al trace and the Cu conductor may not be able to alter the current density distribution. These results agreed with the thermal simulation results conducted by Lee et al.[13] The maximum current density and the crowding ratios at different cross sections for the solder joint are listed in Table II. Since the top-layer of the solder (Y3 plane) is the most vulnerable location during current stressing, we will examine the current density distribution on this layer for the following models that aim to relieve the current crowding effect.

III. METHODS FOR RELIEVING CURRENT CROWDING EFFECT

A. Effect of the dimension of the passivation opening

Figure 4(a) shows the 3D distribution of current density in the solder bump with a larger passivation opening 100 μm in diameter. The cross-section area of the contact opening in this case is 1.4 times larger than that of standard model. However, as seen in Fig. 4(a), current crowding still occurs in the vicinity of the Al entrance. Figure 4(b) shows the distribution of current density in the top layer of the solder. Surprisingly, its maximum current density increases up to 1.22×10^5 A/cm^2, which is higher than 1.11×10^5 A/cm^2 for the standard model. This increase may be attributed to the decrease in bump resistance since the cross section of the bump became larger after the enlargement of the UBM opening.

TABLE IV. Maximum current density and crowding ratios at different cross sections for the solder joint with various thicknesses of Cu UBM.

Method			Cross section					
			Y1, UBM layer	Y2, IMC layer	Y3, top layer of solder	Y4, middle layer of solder	Y5, necking layer of solder	Y6, bottom layer of solder
UBM Cu thickness (μm)	0.7	Maximum	2.58×10^5	2.36×10^5	1.17×10^5	4.07×10^3	8.23×10^3	6.10×10^3
		Ratio	51.5	47.1	23.4	0.8	1.6	1.2
	5	Maximum	6.15×10^5	7.53×10^4	4.37×10^4	3.31×10^3	7.75×10^3	5.92×10^3
		Ratio	122.6	15.0	8.7	0.7	1.5	1.2
	20	Maximum	1.55×10^6	1.27×10^4	7.54×10^3	3.04×10^3	7.71×10^3	5.78×10^3
		Ratio	309.2	2.5	1.5	0.6	1.5	1.2

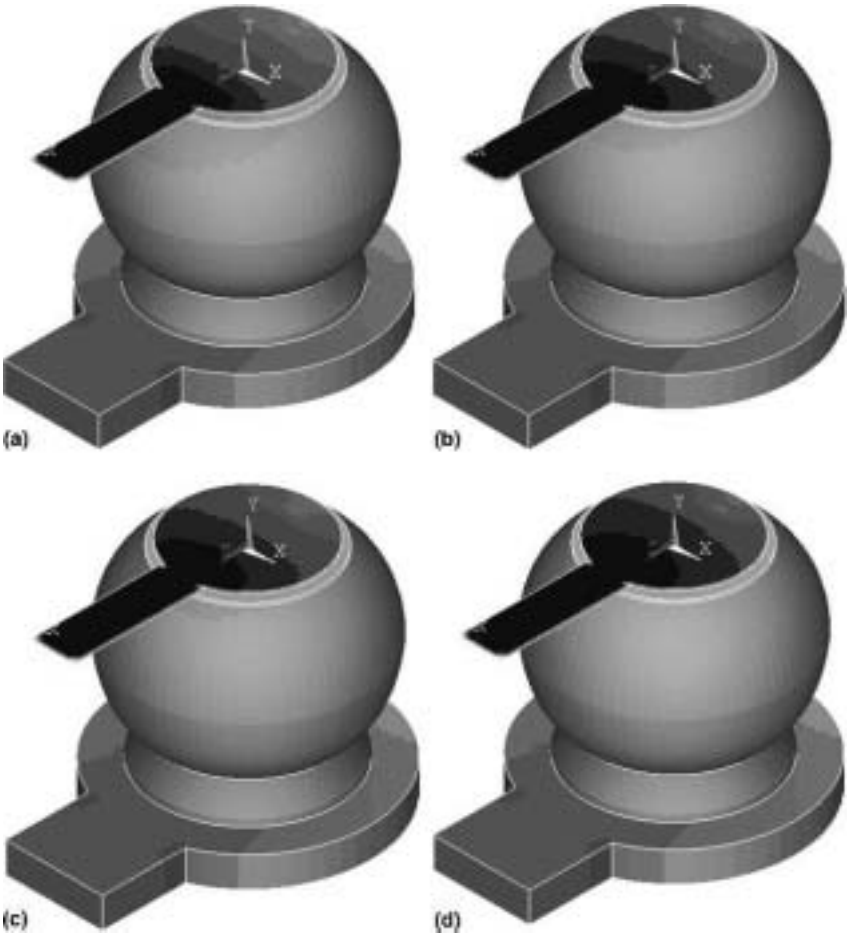

FIG. 6. 3D current density distribution in the solder joint with different UBM resistivity values: (a) 295.4 μΩ cm, (b) 1477 μΩ cm, (c) 2954 μΩ cm, and (d) 14770 μΩ cm.

Table III lists the maximum current density and the corresponding crowding ratio at cross sections Y1 to Y6 for this model. Hence, solder bumps with larger passivation opening have no effect on relieving the current crowding effect.

B. Effect of UBM thickness

To examine the effect of UBM thickness on the distribution of current density, three thicknesses of Cu UBM were simulated, including 0.7, 5, and 20 μm. Figures 5(a)–5(c) show the 3D distribution of current density in the solder joints for the three models, respectively. Although serious current crowding still occurs near the entrance of the Al trace for the three models, the solder bump is moved away from the crowding site due to the thicker UBM. The net effect is a lower maximum current density in the solder joint, and the current density inside the solder becomes more uniform. The maximum current density and the corresponding crowding ratio at cross sections Y1 to Y6 for the three models are listed in Table IV. The maximum current densities in the top layer of the solder are 1.17×10^5, 4.37×10^4, and 7.54×10^3 A/cm^2, respectively. It was surprising that the value dramatically decreased to 7.54×10^3 A/cm^2 for the solder joint with 20-μm Cu UBM, which corresponds to a low crowding ratio of 1.5. Thus, the current crowding effect inside the solder bump was effectively relieved by adding a thick UBM, that is, by moving the UBM/solder interface away from the current crowding region.

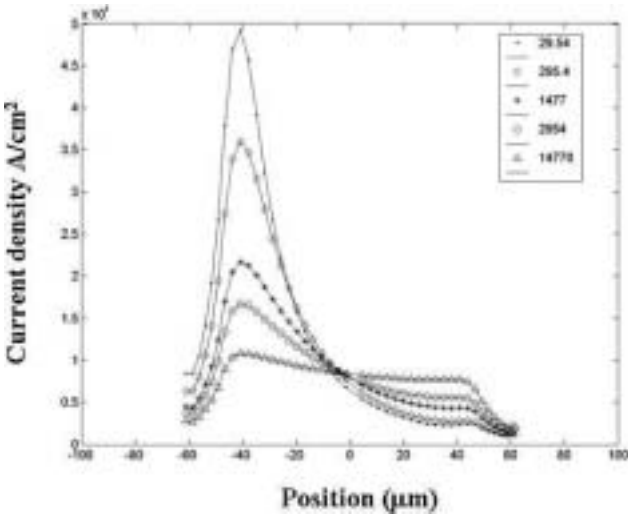

FIG. 7. Current density distribution inside the solder along the Z axis for the five UBM resistivity values at the top layer of the solder (cross-section Y3).

C. Effect of UBM resistivity

The best method of suppressing the current crowding effect in this study was to use a resistive UBM layer. In this simulation, we simulated four solder joints with 295, 1477, 2954, and 14770 μΩ cm, which corresponded to 10, 50, 100, and 500 times the UBM resistivity of the standard model. Figures 6(a)–6(d) show the 3D distribution of current density in the solder joint for the four models. It was found that the current density redistributed in the contact opening. With the increase in UBM resistivity, a greater amount of current traveled further along the Al pad before flowing down into the contact opening. In addition, the current density distribution in the top layer of the solder became more uniform as UBM resistivity increased. Figure 7 shows the current density distribution inside the top layer of the solder along the Z axis. The current became uniformly distributed inside the solder layer, and maximum current densities ranged from 7.01 to 1.55×10^4 A/cm^2. The corresponding crowding ratios are 14.0, 7.4, 5.4, and 3.1 for the solder joint with UBM resistivities of 295, 1477, 2954, and 14770 μΩ cm, respectively, as listed in Table V. Furthermore, the current distribution in the UBM, IMC layers, and solder bump also became more uniform when highly resistive UBM layers were used.

Because the insertion of the resistive layers may increase the bump resistance and thus cause higher Joule heating in the solder joints, thermal simulation was performed to examine temperature distribution in the above

TABLE V. Maximum current density and crowding ratios at different cross sections for the solder joint with various UBM with high resistivities.

Method			Cross section					
			Y1, UBM layer	Y2, IMC layer	Y3, top layer of solder	Y4, middle layer of solder	Y5, necking layer of solder	Y6, bottom layer of solder
UBM resistivity (μΩ·cm)	295.4	Maximum	9.52×10^4	1.04×10^5	7.01×10^4	3.40×10^3	7.45×10^3	5.87×10^3
		Ratio	19.0	20.8	14.0	0.7	1.5	1.2
	1477	Maximum	4.34×10^4	5.00×10^4	3.69×10^4	3.23×10^3	7.27×10^3	5.80×10^3
		Ratio	8.7	10.0	7.4	0.6	1.5	1.2
	2954	Maximum	2.96×10^4	3.49×10^4	2.68×10^4	3.16×10^3	7.17×10^3	5.76×10^3
		Ratio	5.9	7.0	5.4	0.6	1.4	1.2
	14770	Maximum	1.49×10^4	1.87×10^4	1.55×10^4	3.10×10^3	7.04×10^3	5.71×10^3
		Ratio	3.0	3.7	3.1	0.6	1.4	1.1
	29540	Maximum	1.25×10^4	1.60×10^4	1.36×10^4	3.10×10^3	7.01×10^3	5.70×10^3
		Ratio	2.5	3.2	2.7	0.6	1.4	1.1

models. Figures 8(a)–8(e) show the temperature distributions in the solder joints with 29.5 (standard model), 295, 1477, 2954, and 14770 μΩ·cm UBM, respectively. The solder joints were applied by 0.567 A, and the bottom of the BT substrate was maintained at 70 °C. For the standard model in Fig. 8(a), the average temperature in the solder bump was 94.5 °C, which was obtained by averaging the temperatures in the white dotted line in the figure. The solder near the entrance area of the Al trace has higher temperature of 98.8 °C. As the resistivity of the UBM increased, Joule heating effect became significant, as shown in Figures 8(b)–8(e). The temperature increase due to Joule heating was as large as 30.7 °C for the solder joint with 14770 μΩ cm UBM. However, the current flowing in the solder joints is generally less than 0.2 A during device operation. Figure 8(f) shows the temperatures in the solder joints as a function of applied current up to 0.567 A. It is found that Joule heating effect was not serious under 0.2 A. For the standard model, the temperature increase was 2.2 °C, whereas it was 2.8 °C for the solder joint with 14770 μΩ cm UBM. This indicates that the temperature increase due to the resistive UBM was only 0.6 °C at 0.2 A.

IV. DISCUSSION

Figures 9(a)–9(c) depict the crowding ratios at cross sections Y1 to Y6 for the above four methods. It is clear

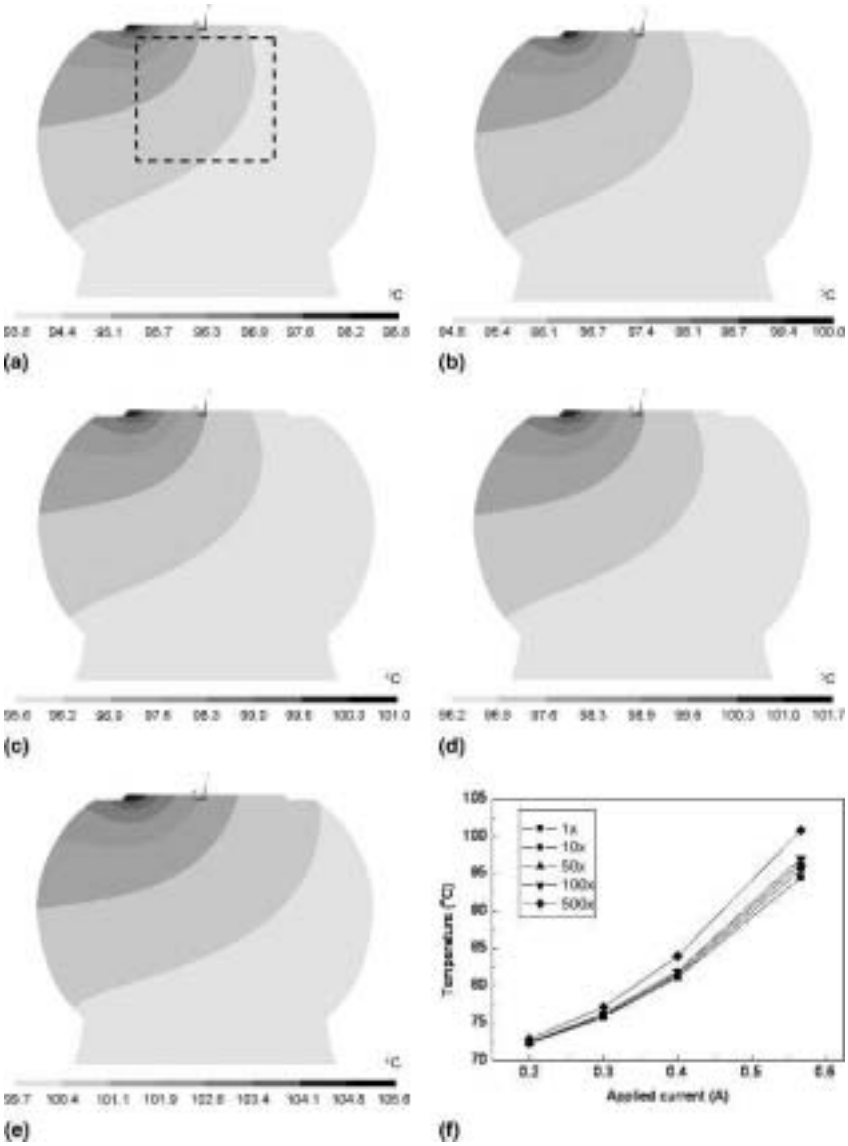

FIG. 8. Temperature distribution in the solder bumps when stressed by 0.567 A: (a) standard model, (b) solder joint with resistive UBM of 295.4 μΩ·cm, (c) solder joint with resistive UBM of 1477 μΩ·cm, (d) solder joint with resistive UBM of 2954 μΩ·cm, (e) solder joint with resistive UBM of 14770 μΩ·cm, and (f) simulated temperature in the solder joint as a function of applied current up to 0.567 A.

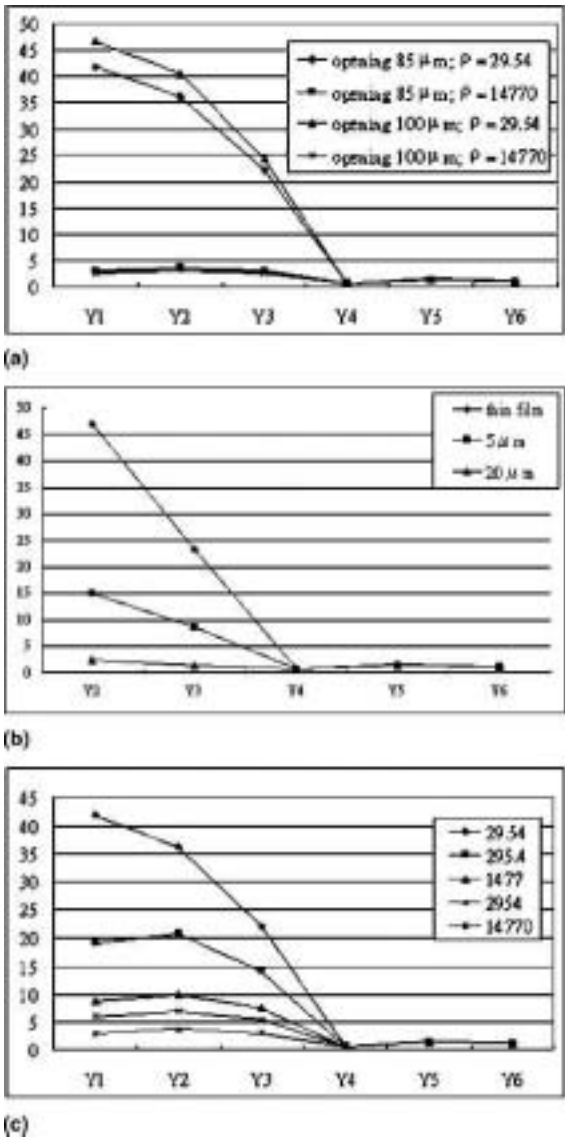

FIG. 9. The crowding ratios for the Y1 to Y6 cross-sections for (a) effect of dimension of passivation opening, (b) effect of Cu UBM thickness, and (c) effect of UBM resistance. It shows that the current crowding effect can be successfully relieved in the solder joints with a thick Cu UBM or with the highly resistive UBM.

that there is no effect on relieving current crowding by the enlargement of the passivation opening, as shown in Fig. 9(a). A thicker Cu UBM can relieve current crowding in the solder bump by moving the UBM/solder interface away from the current crowding region, as seen in Fig. 9(b). The thicker the UBM is, the less the current crowding effect. Figure 9(c) shows that the crowding ratios in the solder joint can be lowered to 3.1 through use of more resistant UBM. This UBM layer can suppress current crowding at the UBM/solder interface.

The best methods for relieving the current crowding effect inside the solder bump fall into two categories: (i) moving the UBM/solder interface away from the current crowding region, and (ii) suppressing current crowding at the UBM/solder interface. If the UBM/solder interface can be moved away from the current crowding region, the threat from the high current density can be avoided. As shown in Figs. 6(a)–6(c), one can clearly see that the current density drops very rapidly when it is moved way from the chip side. Therefore, if one increases the thickness of UBM, the current crowding region will locate within the UBM, and therefore, the UBM/solder interface will be further away from it. Thick Cu UBM has been adopted for use in the flip-chip solder joints.[14] Thus, it is expected the joints would have better electromigration resistance.

To suppress the current crowding effect, the best scenario would be to have the current flowing though the whole solder uniformly. To achieve this goal, increasing the resistivity of UBM would be the best method. Our simulation shows that the current crowding ratio can be reduced to 3.1 when the UBM resistivity is increased to 4770 $\mu\Omega$ cm. However, the tradeoff is the increase in the resistance of the solder joint. The vertical resistance of the standard model was estimated to be 1.2 mΩ. The total resistances of the solder joint became 1.4, 2.1, 3.0, and 10.3 mΩ for the solder joints with a UBM resistivity of 295, 1477, 2954, and 14770 $\mu\Omega$ cm, respectively. This resistive layer could be a TiN, TaN, or Ta material, and could be deposited with UBM, or it could be an additional layer between the Al pad and the UBM. Furthermore, our thermal simulation shows that the Joule heating effect due to the resistive layers was less than 0.6 °C when the applied current was less than 0.2 A. Therefore, the insertion of the resistive layers could relieve current crowding effect significantly and cause very small Joule heating effect at low applied current. Nevertheless, it is still unknown if it is compatible with the current flip-chip manufacturing process, and thus it requires further experimental study.

Furthermore, one can use the hybrid of the above approaches to relieve the current crowding effect. If one adopts the highly resistant layer to relieve the current crowding effect, increasing the cross-section of the passivation opening would have a further effect in reducing the maximum current density in the solder bump. When the model in Sec. III. B is used with a larger passivation opening and the high resistivity UBM of 14770 $\mu\Omega$ cm is adopted, the maximum current density can be further reduced down from 1.6×10^4 to 1.3×10^4 A/cm^2.

V. CONCLUSIONS

A three-dimensional simulation was used to demonstrate that current crowding in the solder joints can be successfully suppressed either by thick Cu UBM or a highly resistive UBM layer. The crowding ratio in the

solder can be reduced from 23.4 to 1.5 when a 20-μm Cu UBM is used, and it can be diminished to 3.1 when a 0.7-μm UBM of 14770 μΩ cm in resistivity is adopted. In addition, the current crowding effect could not be relieved merely by increasing the diameter of the passivation opening or changing the angle between the Al trace and the Cu line. The solder joints with a lower crowding ratio were expected to have better electromigration resistance, and experimental data are needed to verify the simulation results.

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REFERENCES

1. R. Glenn: *Blackwell, The Electronic Packaging Handbook,* CRC Press in cooperation with IEEE Press, Boca Raton, FL (2000).
2. *The International Technology Roadmap for Semiconductor* (Semiconductor Industry Association, San Jose, CA, 2003).
3. K.N. Tu: Recent advances on electromigration in very-large-scale-integration of interconnects, *J. Appl. Phys.* **94,** 5451 (2003).
4. S. Brandenburg and S. Yeh: Electromigration studies of flip chip bump solder joints, in *Proceedings of Surface Mount International Conference and Exhibition,* San Jose, CA (SMTA, Edina MN 1998), p. 337.
5. C.Y. Liu, C. Chen, C.N. Liao, and K.N. Tu: Microstructure-electromigration correlation in a thin strips of eutectic SnPb solder stressed between Cu electrodes. *Appl. Phys. Lett.* **75,** 58 (1999).
6. P.S. Ho and T. Kwok: Electromigration in metals, *Rep. Prog. Phys.* **52,** 301 (1989).
7. C.K. Hu and J.M.E. Harper: Copper interconnections and reliability. *Mater. Chem. Phys.* **52,** 5 (1998).
8. E.C.C. Yeh, W.J. Choi, and K.N. Tu: Current-crowding-induced electromigration failure in flip chip solder joints. *Appl. Phys. Lett.* **80**(4), 580 (2002).
9. W.J. Choi, ECC. Yeh, and K.N. Tu: Mean-time-to-failure study of flip chip solder joints on Cu/Ni(V)/Al thin-film under-bump-metallization. *J. Appl. Phys.* **94,** 5665 (2003).
10. J.W. Nah, K.W. Paik, and J.O. Suh: Mechanism of electromigration-induced failure in the 97Pb–3Sn and 37Pb–63Sn composite solder joints. *J. Appl. Phys.* **94,** 7560 (2003).
11. J.D. Wu, C.W. Lee, P.J. Zheng, J.C.B. Lee, and S. Li: Electromigration reliability of $SnAg_xCu_y$ flip chip interconnects, in *2004 Electronic Components and Technology Conference,* (IEEE, New York) p. 961.
12. T.L. Shao, S.H. Chiu, C. Chen, D.J. Yao, and C.Y. Hsu: *J. Electron. Mater.* **33,** 1350 (2004).
13. T.Y. Tom Lee, T.Y. Lee, and K.N. Tu: A study of electromigration in 3D flip chip solder joint using numerical simulation of heat flux and current density, in *Proceedings of the 51th Electronic Components and Technology Conference, Packaging, and Manufacturing Technology Society,* (2001), p. 558.
14. J.W. Jang, L.N. Ramanathan, J.K. Lin, and D.R. Frear: Spalling of Cu_3Sn intermetallics in high-lead 95Pb5Sn solder bumps on Cu under bump metallization during solid-state annealing. *J. Appl. Phys.* **95,** 8286 (2004).