行政院國家科學委員會專題研究計畫　成果報告

子計畫二：超低耗能系統之智慧型電源管理

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I. The Purpose and the Importance

Recently, new emerging applications such as RFID and wireless sensor network, which consume very low power and utilize the energy harvested from the environment, are gaining more attention. In these applications, the energy are collected from solar, vibration, heat or radioactive decay of matters and at the same time the amount of energy available is limited and the source is unstable.

In some environment, such as the MEMS power generator, the harvested voltage source may be much lower. At the same time in order to reduce the cost of the device, expensive voltage regulator should be avoided. Unstable source poses new challenges in the design of the power management circuit and computation paradigm for the applications.

Moreover, the battery charger is also considered for the no dynamics environment. The charger charge the battery in the standby period.

In this work, we propose a power management system for energy-limited source applications. We propose a supply-side charge-based computation paradigm where computation is carried out only when the energy harvested from the environment is enough to execute a specified operation of the computation.

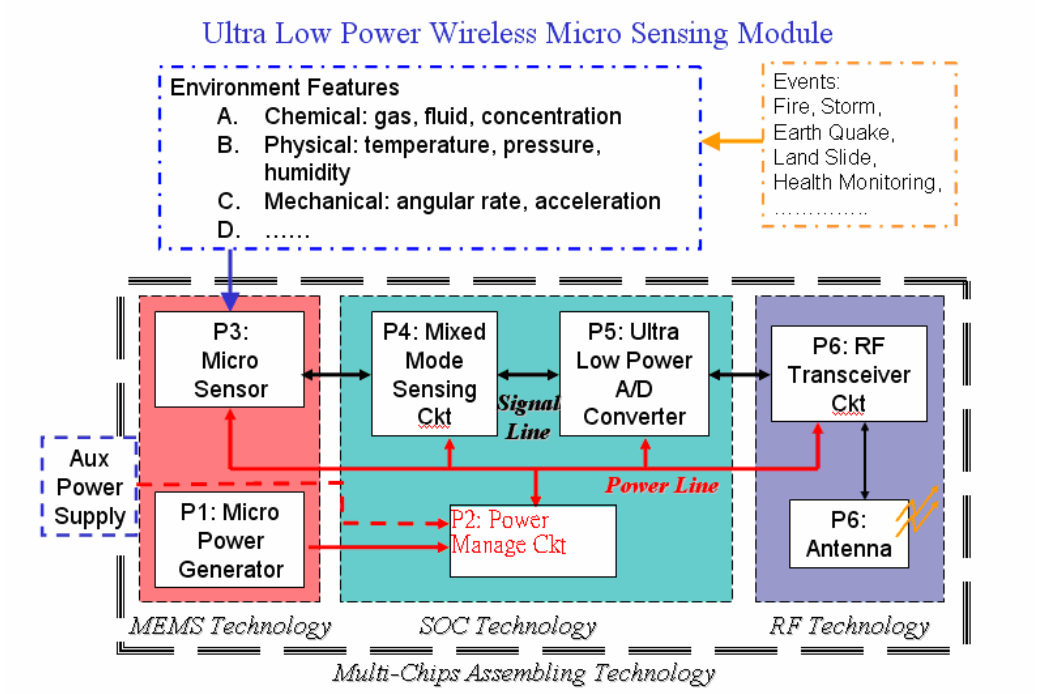

Figure 1: The whole system of the integrated micro sensor system

II. Research Steps

Due to the output power of the MEMS generator could be unstable caused by the vibration of the surrounding and the variation of the load, we need the adaptive power management mechanism to enhance the transfer efficiency of the converter with a stable power output. The conventional power transfer module is designed a constant value, and this output power must make the load to work normally in any situations.

In other words, this output power value is the maximum value of the load consumption. But considering the actual application, the processor, DRAM, monitor, etc. are not in heavy load situation any time. Especially the portable communication device is often at the standby mode, so the efficiency of the whole load range will get much attention at the actual application. The output power of the adaptive power management will be reduced when the needed processing speed is lower. The power just be lifted up when the system needed.

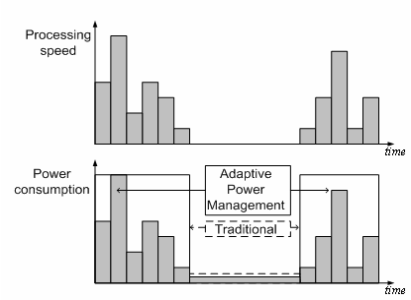

Figure 2: The power consumption of the conventional and the adaptive power management

In theory, the dynamic power is proportional to the square of the operation voltage, so we should utilize the average voltage scaling to reduce the unnecessary power consumption. However in order to adjust the operation voltage to conform to every demand for the load, we have to export the wide range and high efficiency power supply.

i. Integrated System Analysis

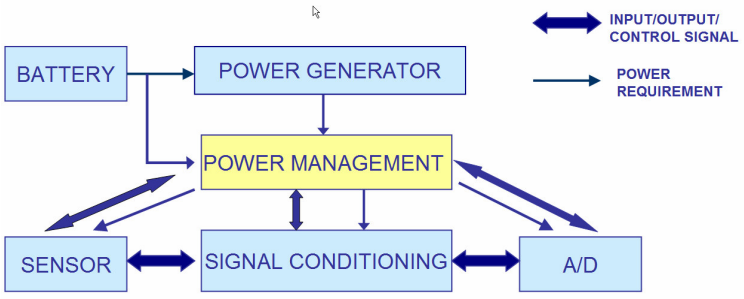

Figure 3: The overall system architecture

The output voltage of the MEMS generator is a time-variable voltage. The property of this voltage may be an aperiodic or unreliable voltage. So we must regulate this voltage to ensure operating the functions of the whole circuit. We expect to utilize a low power consumption DC/DC switching converter.

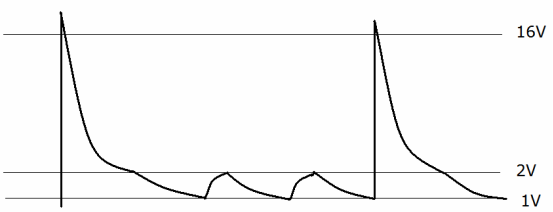

Figure 4: The sketch of the output voltage of MEMS

The peak voltage generated by MEMS is about 16V. Thus high voltage level will damage the circuit device seriously if the circuit isn't fabricated by high voltage CMOS technology.

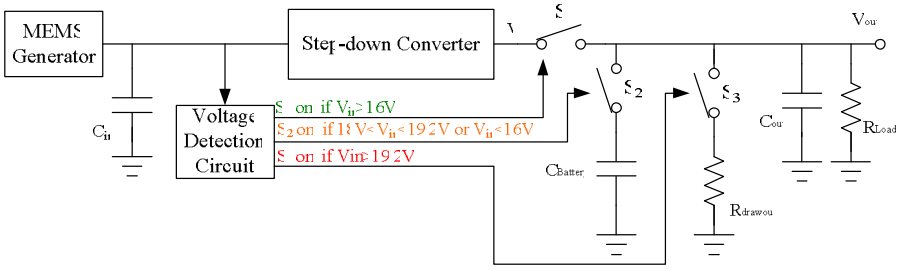

Figure 5: The whole power structure include the MEMS generator

Except the main step-down converter circuit, we should take care of the ultra high voltage level unexpectedly. If the voltage is too high, it can draw out the current to press the voltage. And it also charge the large capacitor to reduce the output ripple if the input power is enough.

ii. Structure Discussion

Typically, we often use the linear regulator, such as low dropout regulator (LDO). However, the drawback of this structure is the low transfer efficiency at the large drop voltage between the output and supply voltage. Presently currently applied switching regulator, the transfer efficiency will be up to 90%, and the large output load range.

	Linear	Switching
Function	**Only steps down**; input voltage must be greater than output.	**Steps up, steps down, or inverts**

Efficiency	**Low to medium,** but actual battery life depends on load current and battery voltage over time; **high** if V_{IN}-V_{OUT} difference is small.	**High,** except at very low load currents (μA), where switch-mode quiescent current is usually higher.
Waste Heat	**High,** if average load and/or input/output voltage difference are high	**Low,** as components usually run cool for power levels below 10W
Complexity	**Low,** which usually requires only the regulator and low-value bypass capacitors	**Medium to high,** which usually requires inductor, diode, and filter caps in addition to the IC; for high-power circuits, external FETs are needed
Size	**Small to medium** in portable designs, but may be larger if heatsinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heat sink
Total Cost	**Low**	**Medium to high,** largely due to external components
Ripple/Noise	**Low**; no ripple, low noise, better noise rejection.	**Medium to high,** due to ripple at switching rate

Table 1: The linear and switching regulator compare

In this project, LDO is not the suitable choice because the low efficiency. Although the switching converter is difficult to design, its several advantages still drive us to implement it.

iii. Implement the DC-DC Power Converter

■ Power Management Review

As we know, dynamic (or adaptive) voltage scaling (DVS) technique is widely used as one of the most effective means for achieving energy-efficiency design. Generally speaking, power consumption has become the most important issue in portable battery-powered applications and high-performance desktop and server applications. The attractive salient features of DVS systems trigger the design of fast and adaptive-output-voltage DC-DC converters with high efficiency over a wide load range.

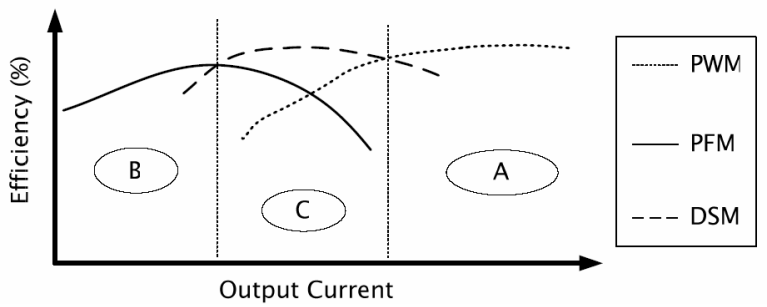

Figure 6: Three control modes converter that efficiency as functions of output current.

A popular technique to improve the efficiency over a wide load range is the hybrid mode, which is composed of pulse-width modulation (PWM) and pulse-frequency modulation (PFM). Hybrid mode achieves a high efficiency for the load current region A and B in Figure 6. However, there exists an efficiency dropping region C in Figure 6. It means that the efficiency curve is not smooth

at the transition between PWM mode and PFM mode. It is a matter of efficiency and current load range for hybrid-mode modulation technique. The hybrid-mode modulation can maintain a high efficiency by closing the two peak efficiency values to reduce the efficiency drop at the sacrifice of load range. Therefore, a dithering skip modulator is proposed to raise the efficiency between PWM and PFM curves in Figure 6. In other words, the efficiency drop between PWM and PFM modes can be raised by the novel DSM mode. Besides, a novel load sensor is also proposed for DSM in order to dynamically switch among these three modes, which are PWM, PFM, and DSM modes. Furthermore, compared with PSM mode and burst mode, DSM mode uses the dithering technique to reduce the output ripple. Due to the insertion of DSM mode, a wide load range and high efficiency can be achieved without sacrificing the load range of conventional hybrid mode. Besides, the improved result is expected as the smooth efficiency curve from PWM mode curve to DSM mode curve and further extending to PFM mode without increasing the output voltage ripple.

■ System Summary

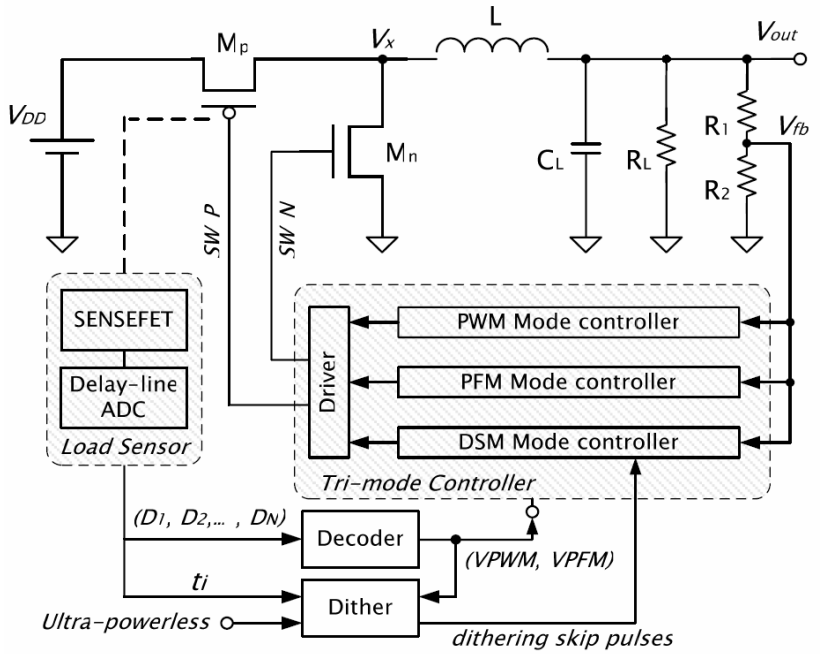

Figure 7: Block diagram of the tri-mode buck converter

	VPWM	VPFM
PWM mode	**1**	**0**
DSM mode	**0**	**0**
PFM mode	**0**	**1**

Table 2: Control mode table

In Figure 7, the buck DC-DC converter is modulated by a tri-mode controller, which is composed of PWM, PFM, and DSM modes. Besides, the load sensor estimates the load condition and sends the digital decision code (D1, D2,..., DN) to decoder in order to dynamically select an optimum modulator among these three modulators. Compared with the prior design, the buck DC-DC converter does not need an external pin to decide the optimum modulator because of the novel load sensor.

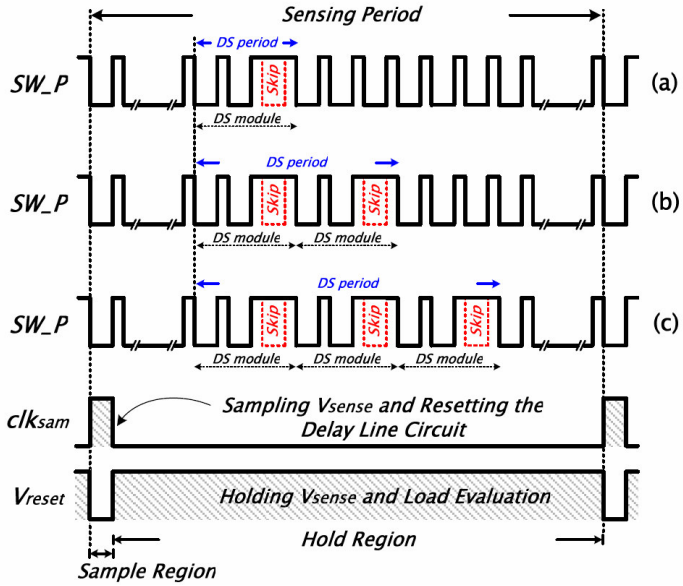

Figure 8: Timing diagrams for dithering skip modulator

The concept of DSM mode is illustrated in Figure 8. The decreasing load current increases the size of DS period as shown in Figure 8 (a) to (c). The latter section will prove the size of DS period is inversely proportional to the load current. Thus, a DS period gradually contains more DS modules when the load current continuously decreases. In order to reduce the output voltage ripple, the dithering skip technique is implemented by the DS module. The function of a DS module is to make the DC-DC converter skip one switching pulse among three continuous switching cycles. Certainly, much power can be retrenched by reducing the switching consumption of power MOSFET because of the gradual decrease of load current.

■ Actual Circuit Design

1. Current Sensing Circuit

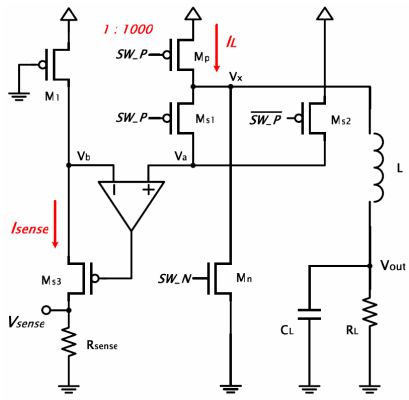

Figure 9: Current sensing technique with SENSEFET topology

In. Figure 9, a formal current sensing technique called SENSEFET topology is proposed by prior literature [8]. During the sensing period, the P-type power MOSFET is turned on by setting signal SW_P low and the sensing current Isense is equal to a thousandth of inductor current IL. By the sensing resistor Rsense, the sensing current can be transferred to sensing voltage Vsense. Thus, the peak value of sensing voltage can stand for the load condition of the output. However, even though Vsense is direct proportional to the load current, it is difficult for simple comparators to decide the switching points of three controllers because the variation of Vsense is too small.

2. Tri-mode Controller

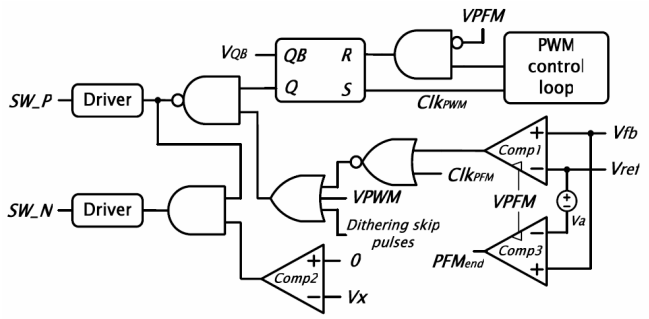

Figure 10: Tri-mode controller is composed of PWM, PFM, and DSM modes

According to the operation codes in Table 2, the tri-mode controller composed of three modulators is shown in Figure 10. Depending on the load condition, the tri-mode controller selects one optimum modulator from these three modulators to generate the switching signals SW_P and SW_N for P-type power MOSFET Mp and N-type power MOSFET Mn,

respectively. For the PWM mode, the conventional current-mode with feedback control is adopted.

The comparator named as 'comp1' is used for PFM mode to determine whether the output voltage is equal to the desired output voltage level or not. If VPFM signal is equal to "0", the comparators 'comp1' and 'comp3' are turned off and their output values are set to "1". The other comparator 'comp2' is utilized to turn off N-type power MOSFET Mn to prevent negative inductor current.

The digital decision code (VPWM, VPFM) decides one optimum modulator from the three modulators for the tri-mode controller. If the code (VPWM, VPFM) is equal to (1, 0), the converter is switched to PWM mode. Similarly, the converter is switched to DSM mode when the code (VPWM, VPFM) is equal to (0, 0). In the meanwhile the dithering skip circuit is ready to skip some pulses of PWM mode to save much power consumption. Owing to the dithering technique, the output voltage ripple can be smaller than that of PSM mode or burst mode [4-6]. Certainly, the power consumption can be reduced by the skipping pulses and the skipping pulses do not dramatically affect the output voltage because of dithering technique.

3. Current-Mode Delay-Line A/D Converter

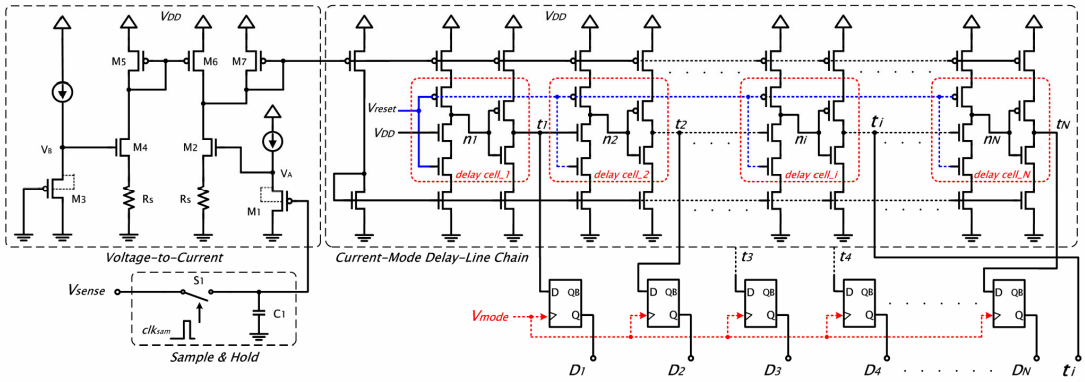

Figure 11: Schematic of the current-mode delay-line A/D converter

The proposed current-mode delay-line A/D converter is composed of a sample-and-hold circuit, a V-I converter, a current-mode delay-line chain, and a register. During a sensing period, there are two regions to complete the generation of dithering skip pulses. At the beginning of the sensing period, a sampling clock clksam starts the first region, which is the sample region. In order to avoid unnecessary mode switching and save the power

consumption, the sensing clock clksam is periodically generated for several times of switching cycles.

4. Decoder and Dithering Skip Code Generator

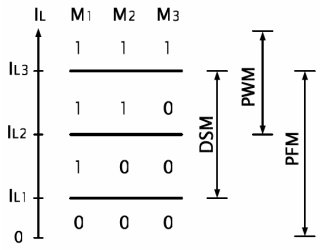

Figure 12: Diagram of the mode decoder

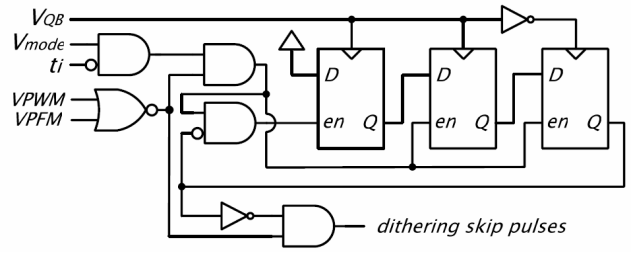

Figure 13: Dither skip pulses generator

$$VPWM_i = M_1 M_2 M_3 + M_2 (PWM)_{i-1}$$

$$VPFM_i = PFM_{end}\left(\overline{M_1}\ \overline{M_2}\ \overline{M_3} + (PFM)_{i-1}\right)$$

A simple example shows the implementation of the mode decoder in Figure 12. Three digital mode bits are selected from the digital word (D1, D2,..., DN). The selection of digital mode bits defines the sizes of three mode region. Thus, the selection rule is determined by the trade-off between efficiency and output voltage

III. Project Schedule & Achievement Anticipation

This integrated project is quite complex. The kinds of the low power DC/DC converter are numerous. However the research in the application to MEMS generator must consider the balance between the little generated power and the efficiency of the system.

i. Present Achievement

The high efficiency, wide input voltage range, stable output voltage, and low power DC/DC converter is proposed. This circuit transfers the power from the MEMS generator to supply the other SOC function blocks.

- **Implement the low power DC/DC converter IC:**

We will implement the low power DC/DC converter IC this year, which can receive the power from the MEMS generator and transfer the stable voltage to supply the whole system. Due to the voltage from the MEMS generator is about 16V, we designed the protect circuit and used high voltage CMOS process. We hope the efficiency of the power transfer achieve 95%.

- **The whole chip simulation:**

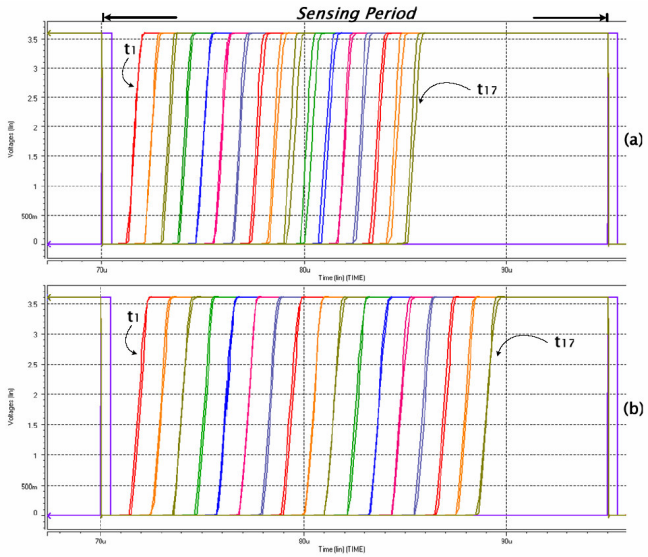

Figure 14: Waveforms of delay-line chain with temperature variations(-40°C~140°C). (a) Load current = 120 mA. (b) Load current = 40 mA.

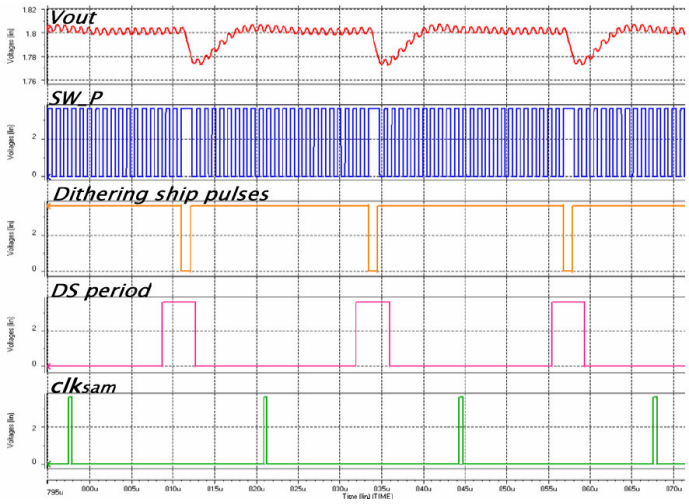

Figure 15: Waveforms of proposed DC-DC buck converter. Loadcurrent = 120 mA

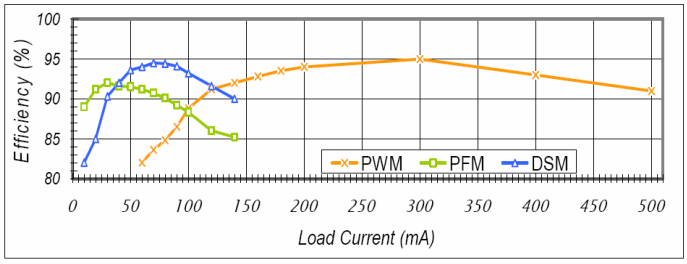

Figure 16: Measured PWM, DSM and PFM mode converter efficiency asVDD = 3.6v, Vout = 1.8v

ii. Research Plan

- ***The design of the DC/DC converter***

  We will research the DC/DC converter structure under the MEMS generator supply to find the maximum power transfer efficiency. The different implement of the DC/DC converter will follow the several problems at the different system. But we should reduce the number of the external component.

- ***Smart power supply***

  We will make efforts in optimum power management, according to the frequency of the digital signal process block, system power using efficiency, load variation, and the amount of the stored energy.

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