Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels

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***Abstract*—In this letter, we have investigated experimentally, for the first time, the feasibility of gate-all-around polycrystalline silicon (poly-Si) nanowire transistors with junctionless (JL) configuration by utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions. *In situ* doped poly-Si material features high and uniform-doping concentration, facilitating the fabrication process. The developed JL device exhibits desirable electrostatic performance in terms of higher ON/OFF current ratio and lower source/drain series resistance as compared with the inversion-mode counterpart. Such scheme appears of great potential for future system-on-panel and 3-D IC applications.**

***Index Terms*—Accumulation mode, gate all around (GAA), inversion mode (IM), nanowire (NW), thin-film transistor (TFT).**

I. Introduction

POLYCRYSTALLINE silicon (poly-Si) thin-film transistors (TFTs) have become very attractive for future 3-D electronics integration due to the low deposition temperature and mature fabrication processes [1], [2]. Recently, the adoption of nanowires (NWs) as the channel in TFTs has demonstrated superior performance, owing to their small volume and the accompanying reduction in defects [3], [4]. Moreover, when combined with multiple gate (MG) configuration, the NW device manifests enhanced drive current and subthreshold slope (SS), as well as good immunity to short-channel effects, because the gates can effectively control the electrostatic potential in the ultrathin channel, so that the channel suffers from less electrical interference between the source and drain [5], [6]. The MG field-effect transistor (FET) with NW channel is thus considered as one of the promising next-generation nanostructure devices. However, as the device size is continuously scaled down, the formation of extremely abrupt junctions between the source/drain (S/D) and channel regions is still very challenging, even for the NW FETs when operating in the inversion-mode (IM) regime. To circumvent this problem, we propose an NWFET with gate-all-around (GAA) structure using one *in situ* doped poly-Si layer to form source, NW channel, and drain regions without additional implantation procedure. Such structure is basically an accumulation-mode transistor and also named junctionless (JL) transistor [7], [8] because, essentially, no junction is contained throughout the device, and therefore, this mitigates the requirement of precise control of dopant concentration profile in the S/D regions. By taking advantage of the tiny body of NW channels and GAA configuration, excellent on–off characteristics are demonstrated in this letter.

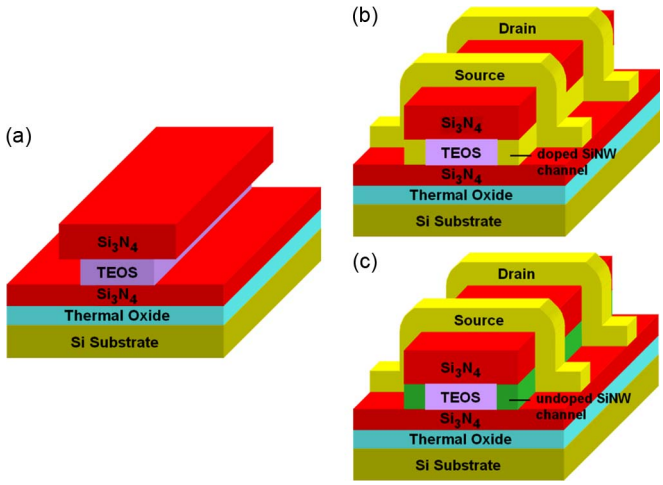

Fig. 1. Illustration of the key steps for forming the NW devices. (a) Formation of sub-100-nm cavities underneath the top nitride layer at the two sides of a nitride/oxide/nitride stack before active layer deposition. (b) Schematic of a JL poly-Si NW device. (c) Schematic of an IM poly-Si NW device. (b) and (c) are the temporary structures before the formation of the all-around gate.

II. Device Fabrication

The fabrication flow basically follows that described in one of our previous reports [9], with the implementation of GAA structure. The main feature of the fabrication is that the NWs were embedded in the sub-100-nm cavities underneath the nitride layer, as shown in Fig. 1(a). The formation of these cavities was carried out by carefully controlling the lateral etching of the tetraethyl orthosilicate (TEOS) oxide layer in dilute HF solution for 90 s. In this letter, poly-Si JL (n^+-n^+-n^+) and IM (n^+-i-n^+) NW devices were fabricated and characterized. The JL devices

Manuscript received December 31, 2010; accepted January 11, 2011. Date of publication February 22, 2011; date of current version March 23, 2011. This work was supported in part by the National Science Council of the Republic of China under Contract NSC 99-2811-M-009-007. The review of this letter was arranged by Editor A. Nathan.

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Digital Object Identifier 10.1109/LED.2011.2107498

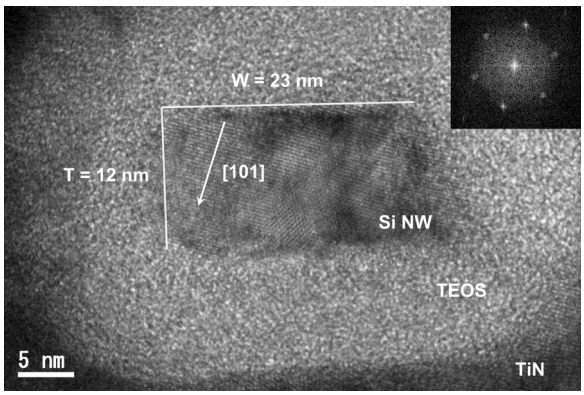

Fig. 2. Cross-sectional HRTEM view of a fabricated JL NW device. The inset is the corresponding diffraction pattern of the NW, revealing the monocrystalline structure of the grain with {110} orientation.

were simply fabricated by depositing *in situ* phosphorus-doped poly-Si using SiH_4 of 0.49 slm and PH_3 of 15 sccm with low-pressure chemical vapor deposition (LPCVD) at 550 °C and 600 mtorr onto the architecture in Fig. 1(a). The *in situ* doping process was chosen to yield a uniform resistivity distribution of around 2.7 m$\Omega \cdot$ cm on a 6-in wafer and has good reproducibility. Such heavily doped poly-Si is commonly employed as the material of gate electrode in the fabrication of FETs. The doped poly-Si was then patterned and etched in a transformer-coupled plasma reactor using Cl_2/HBr gases to define NW channels and S/D regions simultaneously, as shown in Fig. 1(b). For IM devices, undoped poly-Si NW channels were first formed. Afterward, the same *in situ* doped poly-Si as in the JL devices was deposited and patterned to serve as the S/D regions, as shown in Fig. 1(c). To fulfill GAA structure in both types of devices, the dielectric stack comprising nitride/TEOS oxide/nitride was sequentially removed by wet etching in order to expose the NW channels. Next, an LPCVD TEOS oxide of 15 nm was deposited as the gate dielectric layer, followed by deposition of a 10-nm TiN with atomic layer deposition and a 150-nm TiN by sputtering in sequence. The TiN layer was then patterned as the gate electrode. Because doping and activation processes can be done prior to the gate formation, such configuration is suitable for gate-last process and facilitates the utilization of metals as gate materials.

III. Results and Discussion

Fig. 2 shows the cross-sectional high-resolution transmission electron microscopic (HRTEM) image of a fabricated JL device with an NW size of 12 nm in thickness (T) and 23 nm in width (W). Diffraction pattern revealed in the inset is obtained by performing the fast Fourier transform technique on this HRTEM image, furthermore indicating the monocrystalline structure of the Si grain with {110} orientation. It has been reported that poly-Si with higher n-type doping concentration exhibits larger grain size [10]. Consequently, an n^+-poly-Si material is conducive to the production of poly-Si NW structure with enhanced crystallinity, which also would be one of the merits for JL NW devices.

Fig. 3(a) shows the experimental transfer characteristics of JL and IM devices with the NW cross-sectional dimension

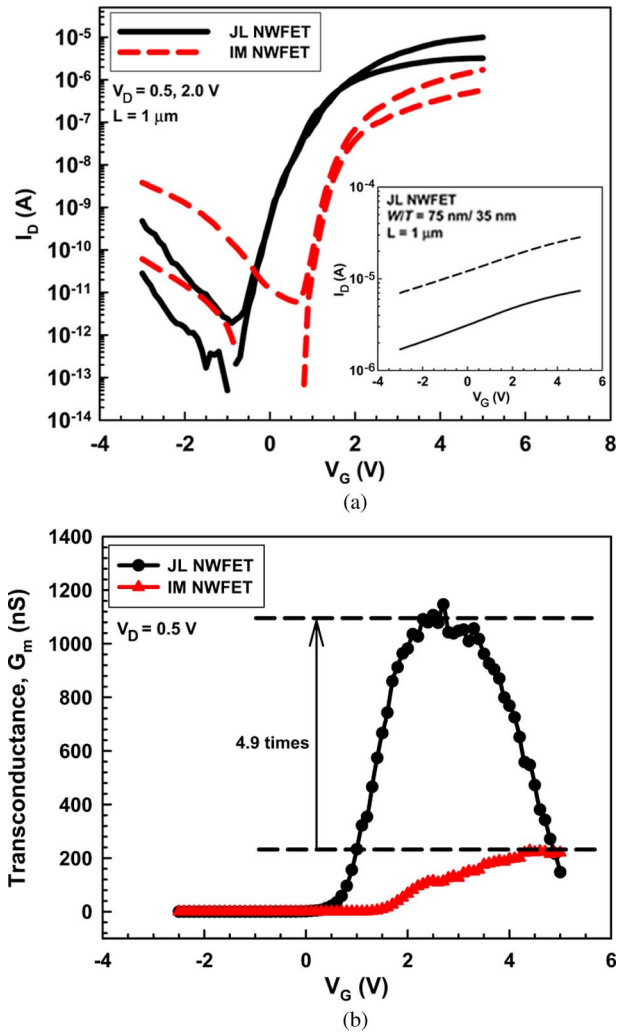

Fig. 3. (a) Transfer characteristics of JL and IM NWFETs with an NW channel dimension of $W/T = 23$ nm/12 nm and a channel length (L) of 1 μm. Characteristics of a JL device with a larger NW size of $W/T = 75$ nm/35 nm, and $L = 1$ μm is also plotted in the inset. (b) Comparison of transconductance (G_m) versus gate voltage for the JL and IM devices at $V_D = 0.5$ V.

as described in Fig. 2. A JL transistor with larger NW size $(W/T = 75$ nm/35 nm$)$ is also characterized and plotted in the inset for comparison purposes to show the NW volume effect. The JL device with smaller NW size exhibits excellent switch properties with SS of 199 mV/dec at $V_G = 0.5$ V and an $I_{\rm ON}/I_{\rm OFF}$ ratio of 5.2×10^6 at $V_G = 2$ V. In contrast, the inset shows poor ON/OFF behavior for the device with larger NW dimensions. In JL devices, the conduction mechanism is through the current of majority carriers flowing in the bulk of the NW channel, and this volume conduction path would be gradually shrunk by decreasing the gate voltage to turn off the device [8]. This implies that the thickness of the NW channel has a strong influence on the switch behavior in JL devices. It is also found that the SS of the smaller NW JL device is significantly improved (199 mV/dec) and becomes comparable to that in the IM device (184 mV/dec). The IM NWFET displays good characteristics, as expected due to the small volume of the NW channels together with GAA structure [9]. However, the ON-state performance of JL device is superior to the IM one. Fig. 3(b) shows the transconductance (G_m) versus gate voltage

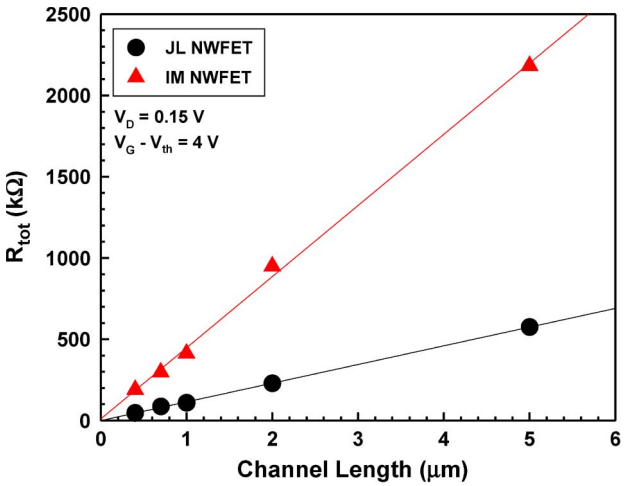

Fig. 4. Measured total resistance $R_{\rm tot} \equiv V_D/I_D = R_{\rm SD} + R_{\rm ch}$ versus channel length of JL and IM NWFETs.

of the JL and IM transistors at $V_D = 0.5$ V. The JL device's G_m peak value is approximately five times larger than that of the IM device. This is ascribed to the abundance of the carriers flowing through the body of channel. Accordingly, the ON current is boosted in the JL transistor.

The measured total resistance $(R_{\rm tot})$ versus channel length in Fig. 4 is generated using the output characteristics data of a series of JL and IM devices with various channel lengths. The $R_{\rm tot}$ can be written as $R_{\rm tot} \equiv V_D/I_D = R_{\rm SD} + R_{\rm ch}$, where $R_{\rm SD}$ and $R_{\rm ch}$ represent the series and channel resistances, respectively [11], [12]. The $R_{\rm SD}$ could be estimated by simply extrapolating the curves to $L = 0$ since $R_{\rm ch}$ decreases to zero and $R_{\rm tot}$ asymptotically approaches the value of $R_{\rm SD}$ at low V_D and high V_G, providing $R_{\rm SD}$ values of 0.49 and 9.65 kΩ for the JL and IM devices, respectively. The larger $R_{\rm SD}$ found in the IM device is speculated, in part, due to the existence of junctions in the devices. On the other hand, the slope of the curves in the plot reveals the information of $R_{\rm ch}$ per unit channel length, and it appears evidently larger in the IM devices, owing to the fact that the JL device is a gated resistor [8] and the cross section for carrier flow is much larger than that in the IM device. Therefore, the lower $R_{\rm SD}$ and $R_{\rm ch}$ in the JL device result in the enhanced ON-state performance.

IV. Conclusion

In summary, we have demonstrated the feasibility of GAA poly-Si NWFETs with JL structure by employing only one *in situ* doped poly-Si layer to act as the active regions without additional intentional doping procedure. The fabricated JL device exhibits high $I_{\rm ON}/I_{\rm OFF}$ ratio and low subthreshold slope. Lower S/D series resistance is also found in the JL device as compared with the IM one, further boosting the drive current. Consequently, the proposed JL NWFETs featuring simplified fabrication processes stand as highly promising transistors for future practical manufacturing and applications.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories and Nano Facility Center of National Chiao Tung University for the assistance in device fabrication.

References

[1] H. Wang, M. Chan, S. Jagar, Y. Wang, and P. K. Ko, "Submicron super TFTs for 3-D VLSI applications," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 439–441, Sep. 2000.

[2] E. K. Lai, H. T. Lue, Y. H. Hsiao, J. Y. Hsieh, C. P. Lu, S. Y. Wang, L. W. Yang, T. Yang, K. C. Chen, J. Gong, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A multilayer stackable thin-film transistor (TFT) NAND-type Flash memory," in *IEDM Tech. Dig.*, Dec. 2006, pp. 41–44.

[3] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, vol. 425, no. 6955, pp. 274–278, Sep. 2003.

[4] H. C. Lin and C. J. Su, "High-performance poly-Si nanowire NMOS transistors," *IEEE Trans. Nanotechnol.*, vol. 6, no. 2, pp. 206–212, Mar. 2007.

[5] M. Im, J. W. Han, H. Lee, L. E. Yu, S. Kim, C. H. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y. K. Choi, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102–105, Jan. 2008.

[6] S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Yeo, J. K. Ha, H. Lim, H. W. Park, D. W. Kim, T. Y. Chung, K. S. Oh, and W. S. Lee, "Characteristics of sub-5-nm trigate nanowire MOSFETs with single- and poly-Si channels in SOI structure," in *VLSI Symp. Tech. Dig.*, Jun. 2009, pp. 142–143.

[7] C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 053 511-1–053 511-2, Feb. 2009.

[8] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[9] H. H. Hsu, T. W. Liu, L. Chan, C. D. Lin, T. Y. Huang, and H. C. Lin, "Fabrication and characterization of multiple-gated poly-Si nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3063–3069, Nov. 2008.

[10] Y. Wada and S. Nishimatsu, "Grain growth mechanism of heavily phosphorus-implanted polycrystalline silicon," *J. Electrochem. Soc.*, vol. 125, no. 9, pp. 1499–1504, Sep. 1978.

[11] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, vol. 18, no. 5, pp. 953–959, May 1979.

[12] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," *IEEE Electron Device Lett.*, vol. 1, no. 9, pp. 170–173, Sep. 1980.