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The study of copper thin film resistivity for applications beyond 65 nm technology node

(微電子 65 奈米世代後銅薄膜阻抗係數之探討)

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Abstract

As device continues scaling down to 65 nm node, the copper line resistance is seen to rise non-linearly, which has negative impact on RC delay. While the industry is relieving this problem by implementing a conformal and thinner barrier using a dep/etch/dep ionized physical vapor deposition (i-PVD) of tantalum, fundamental understanding of the relationship between resistivity and copper thin films and the mechanisms of the resistivity increase is urgently necessary for delving methods to contain this issue beyond 65 nm node. Due to within-die non-uniformity from the process variation and line-width variations in the patterned line structures, it is very difficult to quantify the discrete contributions either from grain boundary scattering, impurities scattering or surface scattering. As a result, blanket films stacks with different copper grain sizes are specially prepared using state-of-art 12-inch production tools, whose resistivity are characterized by scanning resistance probe (SRP) technique and four-point-probe (FFP) technique. This report summarizes our novel and unique sample preparation methodology to control the same grain size at various thicknesses, and the effect of seed grain size on resistivty as function of thickness, especially below 100 nm. The influence of surface scattering in copper films with large copper seed grain can be clearly observed when thick films are thinned after a high temperature anneal in which case the grain size is considerably larger than the electron mean free path of copper at room temperature (39nm).

I. Introduction

Copper metallization was first implemented at 180 nm technology node by IBM Corp. for its lower resistivty reducing RC delay and better electromigration resistance than those of aluminum [1]. However, as device continues scaling down to 65 nm

node, the copper line resistance is seen to rise non-linearly, which has negative impact on RC delay [2, 3]. The increase of copper resistivity will become severe when the line-width of the copper in the metallization stack is comparable to the conduction electron's mean-free-path of copper, 39 nm [4]. Fundamentally, several parameters may contribute to the copper resistivity increase through different scattering mechanisms such as (1) surface scattering arisen from surface roughness at various copper interface and line edge roughness induced by patterning, which can be described by a model developed by Fuchs and Sondheimer (FS) [5, 6], (2) grain boundary scattering by smaller grain size, which is described by the Mayadas–Shatzkes (MS) model, and (3) defect and impurity scattering [7]. However, it is very difficult to quantify the discrete contributions from these parameters in the patterned line structures due to the process variation, within-die and within-wafer non-uniformity and line-width variations. Recent research efforts have focused on blanket film stack to understand the scattering contributions [8-11]. In order to compare the resistivity of films with different thicknesses, but at the same grain size, one approach is to probe the resistivity along the beveled surface of a thin copper film based on scanning resistance probe (SRP) technique [reference]. The other approach is to polish thick copper films back to various desired thicknesses, which are measured by conventional four-point-probe (FFP), which will be described in details in the following section. In the backend interconnects, copper metallization stack consists of electroplated Cu/PVD seed/PVD Ta/TaN barrier/dielectric in the line structure. As the copper thickness or line-width reduces below 100 nm, PVD copper seed may play a role in controlling the grain size in the copper thin film, in turn its resistivity. However, the contribution from grain size of copper seed is still not well understood yet. The objective of this study is to elucidate the role of the grain size of copper seed on copper resistivity and copper final grain size in very thin electroplated copper films.

II. Experimental

In order to investigate the effects of seed and its grain size on the resistivity of thin electroplated copper films, two sets of samples with two different seed grain sizes, but at various thicknesses ranging from 20 to 200 nm are designed and prepared, assuming that the impurity scattering is the same in all cases described below.

Preparation of sample set #1 (copper seed with large grain)

A 450 nm SiO_2 film is first deposited onto a 12-inch bare silicon wafer (p-type, Si(001)) as the substrate. Then, 50 nm Ta is deposited by ionized

physical-vapor-deposition (i-PVD) as the diffusion barrier, which is followed by a 20 nm thin PVD copper as seed layer for copper electroplating. A 200 nm Cu is deposited by electroplating, which is then annealed at 200℃ for 30 minutes to ensure large grain size even though self-annealing occurs in the electroplated copper. Afterwards, this layer is polished back to 20 nm copper which is used as the seed layer with large grain. A 2000 nm electrochemical plating (ECP) copper film is deposited again, then annealed at 200℃ for 30 minute. Various thicknesses with fixed grain size are obtained by polishing back using chemical-mechanical polish (CMP) to desired thickness. A 7 nm Ta thin film is then deposited as a passivation layer to avoid any oxidation of copper films schematically shown in Figure 1. In this set, the effect of grain boundary scattering is kept constant for various thicknesses.

Preparation of sample set #2 (normal copper seed)

A 450 nm SiO2 film is first deposited onto a 12-inch bare silicon wafer (p-type, Si(001)) as the substrate. Then, 50 nm Ta is deposited by ionized physical-vapor-deposition (PVD) as the diffusion barrier. Copper is deposited by self-ionized physical vapor deposition (i-PVD) with different thicknesses. A 7 nm Ta thin film is then deposited as a passivation layer to avoid any oxidation of copper films as schematically illustrated in Figure 2. In this set of samples, different thickness possesses different grain size leading to our investigation on the effect of the grain boundary scattering.

Thin film and sheet resistance characterization

A 20 mm x 20 mm sample is cut out of a 12-inch wafer with the film stack described above. A four-point probe (FPP, DektakST 32) is used to measure sheet resistance. Copper film thickness is measured by a scanning electron microscope (SEM) (JEOL JSM 6500), which is calibrated by transmission electron microscope (TEM) (TECNAI 20). Thin film resistivity is then obtained from known thickness. The grain size is measured by focus ion beam (FIB) (A dual beam, focus ion beam & electron beam system, FEI Corp).

Spreading resistance probe technique

The SRP technique (SSM 150 Automatic spreading Resistance) uses beveled samples where two probes are stepped down from the full thickness layer to the substrate as show in Figure 3. This has been widely used for measuring the depth resistivity distribution, and corresponding electrically active doping profile in silicon. Such technique can be adapted to measure the resistivity depth profiles in thin metal film, where the sample of about 4 mm x 6 mm size is first beveled under a small angle

(8 minute). Then, two metal probes with a load of about 10g are aligned parallel to the bevel edge and later are stepped (with 1 mm step) from the surface toward the substrate while measuring the resistance. The typical depth resolution thus obtained is about 6 nm. For silicon, this procedure is known to result in high-quality beveled surfaces with sharp bevel edge delineation. In this work, we will explore the capabilities of SRP for metal resistivity characterization of thin films with the same grain size.

III. Results and Discussion

SRP technique is first employed for characterizing the resistivity of copper thin films with the same grain size. The raw data obtained from known test sample is comparable to that of published papers [12]. However, we encounter technical complications when converting the raw data to resistivity which is based on many assumptions. One of the required parameters, contact resistance (Rc), which is related to the conditions of tip and beveled surface, could not be consistently obtained due to the condition of rough, beveled surface [12,14]. In addition, our SRP system can only measure resistance larger than 1 ohm, which is equivalent to copper thickness below 80 nm if the bulk Cu resistivity of 1.8 μΩ-cm is applied. Because of its limited thickness range (< 80 nm) and difficulties in the validation of assumptions, SRP measurement is dropped until better instrumentation and sample preparation are available. The result in this section is based on four-point probe measurements of a series of thicknesses in either set #1 or 2 as described in the experimental section.

Since thin copper films (20-50 nm) is normally employed as the seeding layer to reduce the IR drop across the wafer during the subsequent ECP copper in the typical dual damascene process, the relationship between resistivity and PVD seed thickness will be first studied using the sample set #2 in the range between 20 and 200 nm. The resistivity as a function of thickness shown in Figure 4 indicates that copper resistivity increases significantly as thickness decreases below 100 nm. A 50% increase is seen for 30 nm thick film (3.0 μΩ-cm) as compared to that of 200 nm thick film (2.0 μΩ-cm). FIB is employed to measure the copper grain sizes in 20 nm PVD Cu seed/80 nm PVD Cu and 20 nm PVD Cu seed/200 nm PVD Cu as shown in Figure 5(a) and Figure 5(b), respectively. The average grain size in 100 nm PVD copper film is 600 nm while the grain size in 220 nm PVD copper is 900 nm. Preliminary data on copper grain size shows clear increase in grain size with increasing thickness. The drastic increase of resistivity with decreasing thickness below 100 nm shown in Figure 4 is presumably dominated by grain boundary scattering [13].

This highlights the potential impact of PVD copper seed on the metal resistance if its grain size cannot grow into micron range after electroplating copper is added on and subsequent annealed. In order to address the impact of the seed grain size on the copper thin film resistivity, we first utilize a 20 nm thick copper with largest grain size estimated in ~1 μm range, as the seed, and then design a series of ECP Cu thickness from 40 nm to 200 nm with the same copper grain size as described in the preparation of sample set #1. The resistivities of thin ECP copper films with large seed grain stated in sample set #1 show a graduate increase with decreasing thickness. For example, the resistivity of 70 nm film is 2.06 μΩ-cm, which is 8% decrease from 1.90 μΩ-cm for 200 nm thick film. FIB/SEM analysis of 60 nm and 140 nm thick copper films shows their grain sizes are almost the same as shown in Figure 7(a) and Figure 7(b).

Comparing these two sets of samples as shown in Figure 8, small grain size and surface scattering both contribute to the resistivity increase in PVD copper films, while the resistivity of large ECP with large seed grain and large ECP copper grain are much reduced primarily due to the minimization of grain boundary scattering. The discrepancy in resistivity is more severe as the thickness decreases down to 40 nm. This study points out that future directions of resistivity reduction beyond 65 nm technology can be achieved primarily through the control of grain size including the seed grain, which, in turn, will slow down the increase of RC delay in the backend interconnects.

IV. Conclusion

SRP technique is first employed to study the resistivity of various thicknesses at fixed grain size. Because of its limited thickness range (< 80 nm) from instrumentation and difficulties in the validation of assumptions, SRP measurement is dropped until better instrumentation and sample preparation become available. A novel and unique sample preparation methodology is developed by polishing back a thick film with large grain size after high-temperature anneal, then to desired thickness, thereby keep the grain size the same at various thicknesses. FFP measurement on a series of PVD copper thin films shows that copper resistivity increases significantly as thickness decreases below 100 nm. A 50% increase is seen for 30 nm thick film (3.0 μΩ-cm) as compared to that of 200 nm thick film (2.0 μΩ-cm), which is primarily dominated by grain boundary scattering. When large copper grain is used as seed in conjunction with large ECP copper grain (~1 μm), the resistivity increase is more gradual, for example, 8% increase vs. 15% increase at 80 nm from two different sample sets. In this case, resistivity increase is dominated by surface scattering with little effect from grain boundary scattering due to our control

of fixed in ECP copper films copper grain size. This study points out that future directions of resistivity reduction beyond 65 nm technology can be achieved primarily through the control of grain size including the seed grain, which, in turn, will slow down the increase of RC delay in the backend interconnects.

V. Future studies

We plan to complete another set of samples with small seed grain size for various ECP copper thickness at constant grain size to further elucidate the importance of seed layer and the impact of seed microstructure on copper resistivity. In addition, we plan to explore an efficient method for characterizing the resistivity of thin metal films at the constant grain structure because (1) FFP is time consuming in sample preparation and thickness calibration [16] and (2) SRP is not robust method for metal resistivity due to many hypotheses [17].

VI. Acknowledgements

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VII. References

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VIII. Figures and Captions

Figure 1 Schematic diagram of sample set#1

Figure 2 Schematic diagram of sample set#2

Figure 3 Schematic diagram of the spreading resistance probe (SRP).

Figure 4 Resistivity of PVD copper films as a function of thickness.

Figure 5(a) Focus ion beam (FIB) viewgraph of a 20 nm PVD Cu seed/80 nm PVD Cu stack. The average grain size in 100 nm PVD copper film is 600 nm.

Figure 5(b) Focus ion beam (FIB) viewgraph of a 20 nm PVD Cu seed/200 nm PVD Cu stack. The average grain size in 200 nm PVD copper film is 900 nm.

Figure 6 Resistivity of ECP copper films as a function of thicknesses.

Figure 7(a) Focus ion beam (FIB) viewgraph of a 20 nm CMP Cu seed/60 nm ECP Cu stack. The average grain size in 80 nm ECP copper film is 900 nm.

Figure 7(b) Focus ion beam (FIB) viewgraph of a 20 nm CMP Cu seed/120 nm PVD Cu stack. The average grain size in 140 nm ECP copper film is 900 nm.

Figure 8 Resistivity of PVD copper films and ECP copper films as a function of thickness.

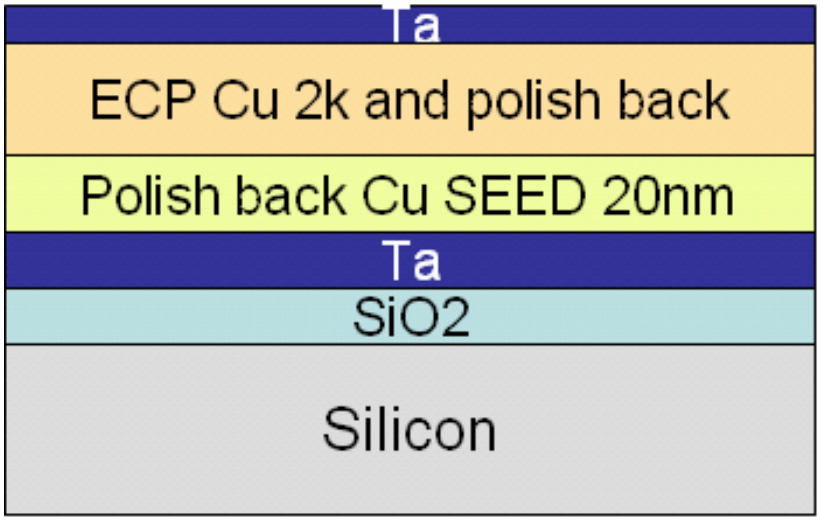

Figure 1 Schematic diagram of sample set#1

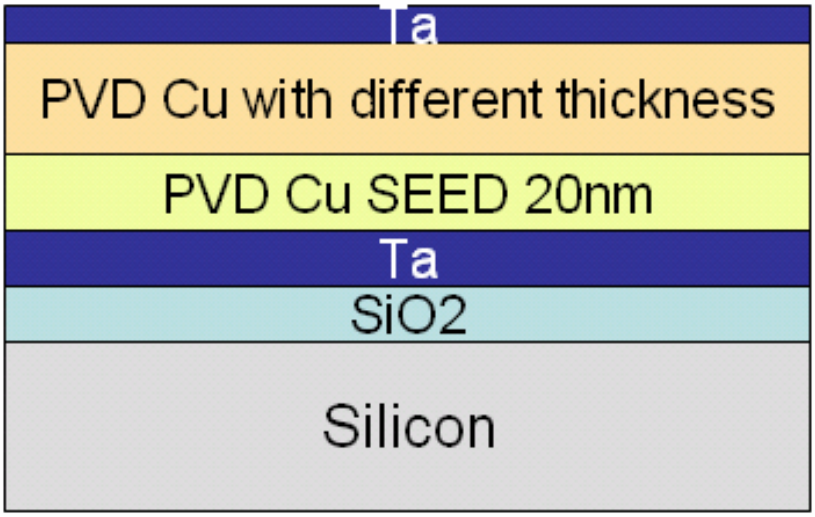

Figure 2 Schematic diagram of sample set#2

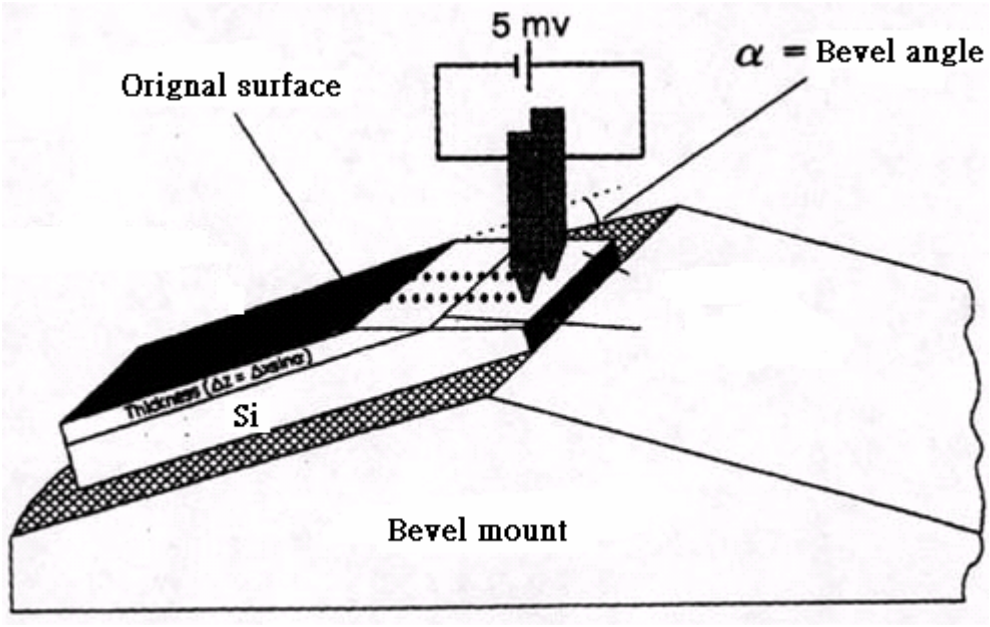

Figure 3 Schematic diagram of the spreading resistance probe (SRP).

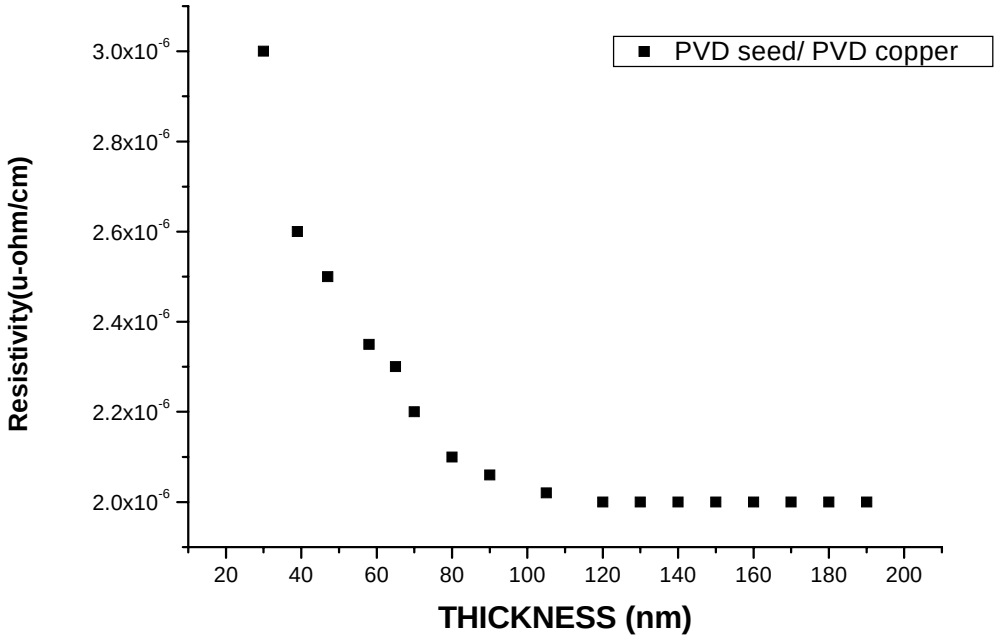

Figure 4 Resistivity of PVD copper films as a function of thickness.

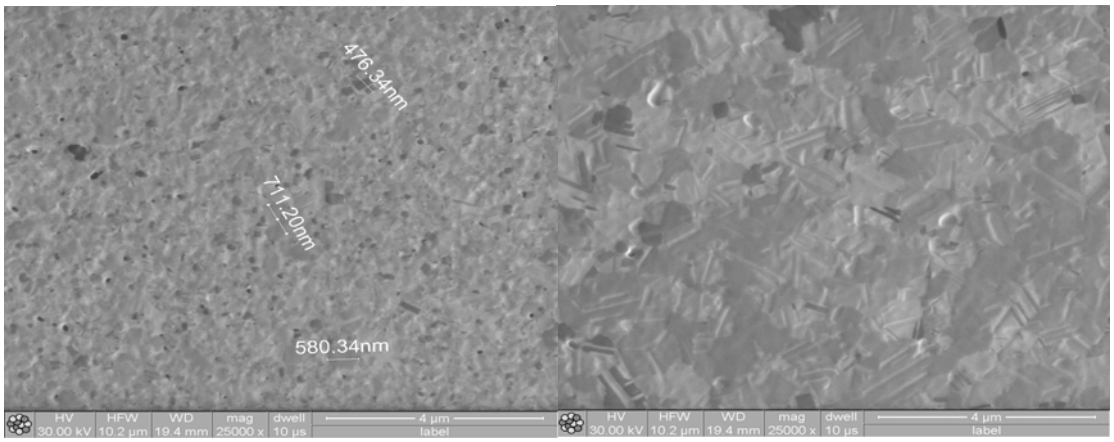

Figure 5(a) Focus ion beam (FIB) viewgraph of a 20nm PVD Cu seed/80nm PVD Cu stack. The average grain size in 100 nm PVD copper film is 600 nm.

Figure 5(b) Focus ion beam (FIB) viewgraph of a 20nm PVD Cu seed/200nm PVD Cu stack. The average grain size in 200 nm PVD copper film is 900 nm.

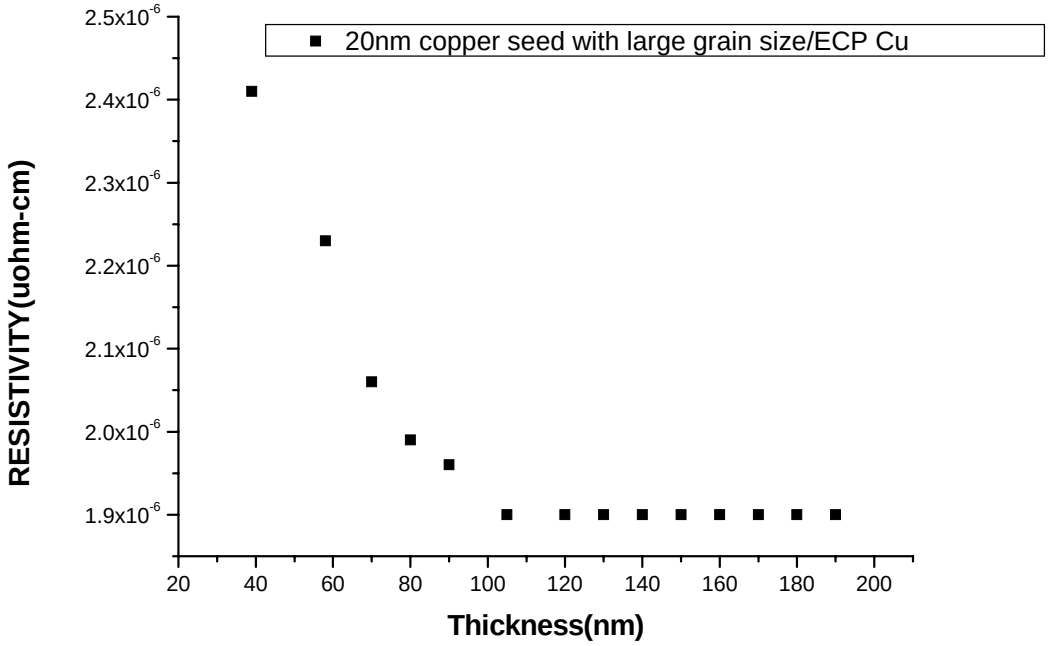

Figure 6 Resistivity of ECP copper films as a function of thicknesses

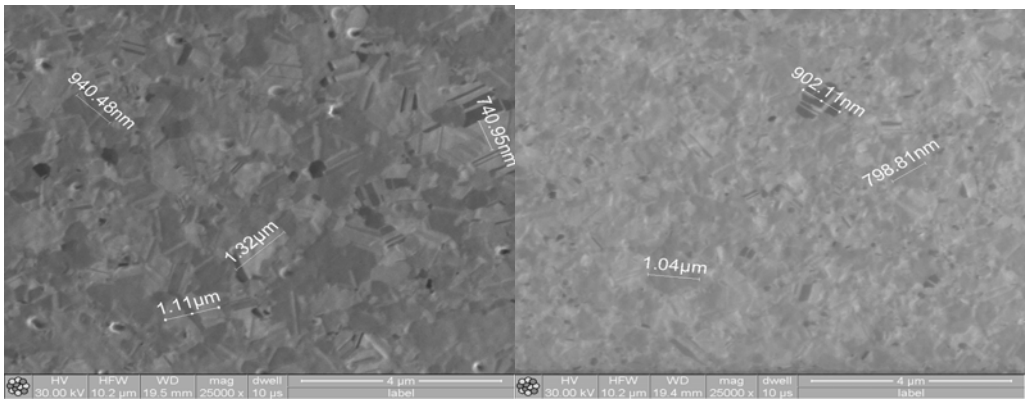

Figure 7(a) Focus ion beam (FIB) viewgraph of a 20nm CMP Cu seed/60nm ECP Cu stack. The average grain size in 80 nm ECP copper film is 900 nm

Figure 7(b) Focus ion beam (FIB) viewgraph of a 20nm CMP Cu seed/120nm PVD Cu stack. The average grain size in 140 nm ECP copper film is 900 nm.

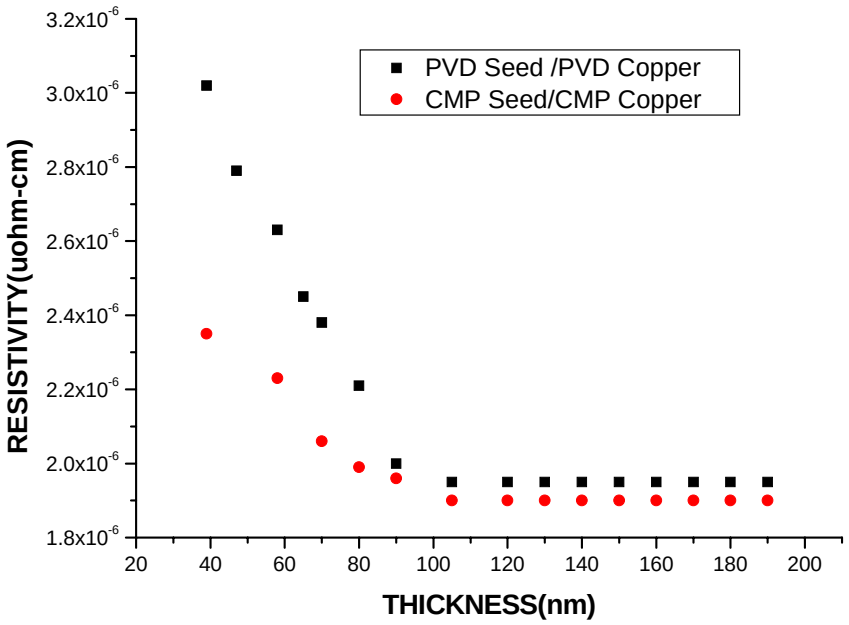

Figure 8 Resistivity of PVD copper films and ECP copper films as a function of thickness.