Interleaving Energy-Conservation Mode (IECM) Control in Single-Inductor Dual-Output (SIDO) Step-Down Converters With 91% Peak Efficiency

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***Abstract*—The proposed single-inductor dual-output (SIDO) converter with interleaving energy-conservation mode (IECM) control is designed using 65 nm technology to power the ultra-wide band (UWB) system. The energy-conservation mode (ECM) control generates four different energy delivery paths for dual buck outputs with only one inductor. In addition, the superposition technique is used to achieve a minimized inductor current level. The average inductor current is equal to the summation of two output loads. Moreover, the IECM control activates the interleaving operation through the current interleaving mechanism to provide large driving capability as well as to reduce the output voltage ripple. As a result, 91% peak efficiency is derived and the output voltage ripple appears notably minimized by 50% using current interleaving at heavy load. The test chip occupies 1.44 mm^2 in 65 nm CMOS and integrates with a three-dimensional (3-D) architecture for inductor integration.**

***Index Terms*—Current interleaving, DC-DC converter, energy delivery path, output voltage ripple, power conversion efficiency, single-inductor dual-output (SIDO) converter, ultra-wide band (UWB) system.**

I. Introduction

In battery-powered mobile systems, a power IC should simultaneously have high efficiency, satisfactory regulation, small volume, and robustness. These characteristics are essential in ultra-wide band (UWB) applications, such as the wireless universal serial bus (USB) that has the advantage of speed over other wireless technologies. The single-inductor dual-output (SIDO) converter [1]–[10] has the capability to provide two high-quality output voltages for different function blocks by using a single inductor. It can reduce the print-circuit-board (PCB) area compared to the single-inductor single-output (SISO) converter [11]–[15] when multi-output supply voltage is requested in power management. The comparator-controlled technique with a simple control scheme for power distribution can minimize power consumption to improve efficiency [1], [2], but it sacrifices regulation performance and needs to be redeemed by a post-regulator. The discontinuous conduction mode (DCM) [3] control can distribute the energy into the two outputs of SIDO converter to minimize the cross regulation. However, at heavy loads, an increase in inductor peak current causes a large output voltage ripple. The tri-state control [15] utilizes the freewheel stage to reset the inductor current to a default value at the beginning of every switching cycle. The pseudo-continuous conduction mode (PCCM) [4] combines the advantages of continuous conduction mode (CCM) and DCM, but results in large power loss due to high inductor current level. In addition, to improve efficiency, the energy delivery paths must be well arranged [5]–[7]. Thus, the number of power switches can be decreased [8], but the flexibility is reduced because the outputs must include at least one step-up regulation to release the inductor current for system stability. The energy distribution method in [9] leads to cross talk effect since the inductor charging scheme is controlled by the load condition from one specific output. Fortunately, the CCM operation in [10] solves transient cross regulation and voltage spike by using a flying capacitor. However, the bulk capacitor increases the cost in a real system application.

In conclusion, the essential design issues of the SIDO converter are low output voltage ripple, minimized cross regulation, and high power conversion efficiency. To meet the power requirements of UWB system, the proposed SIDO converter adopts the buck operation that steps down the battery power to dual low voltages. The interleaving energy-conservation mode (IECM) control can achieve the power management function through the demand of four power switches. These four power switches in one SIDO converter constitute the proper energy delivery paths for dual step-down outputs. In addition, a minimum inductor current level is maintained in the proposed control to improve efficiency and provide low ripple, minimized cross regulation, and step-down outputs with a compact 3-D package at the same time.

Fig. 1 shows the proposed SIDO modules constituting the power management function to supply the UWB system with different operation modes. The integration of the two SIDO modules can supply four distinct output voltages, namely, V_{OA},

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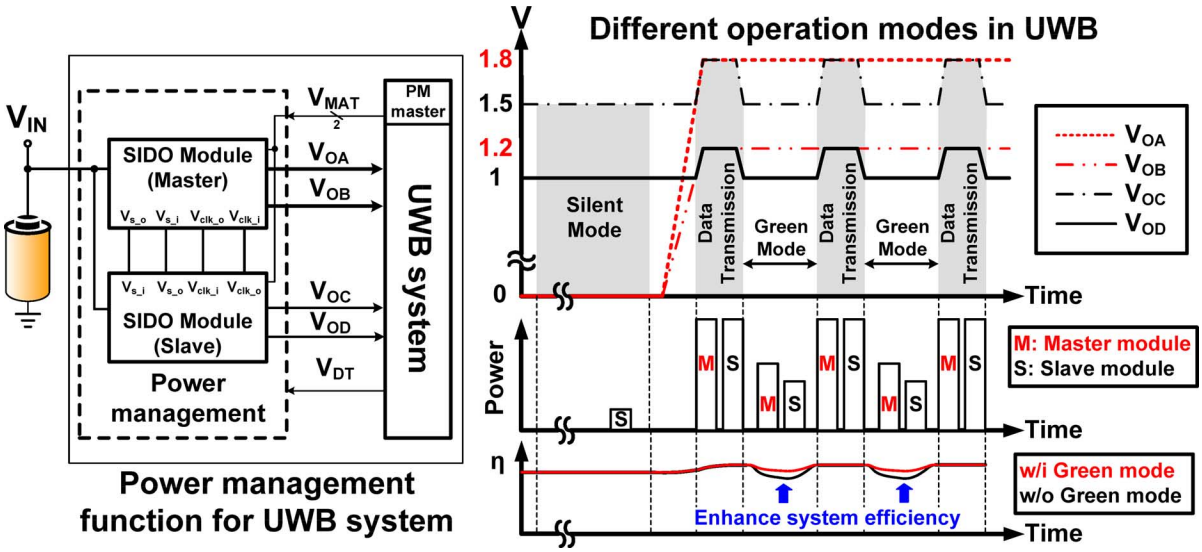


Fig. 1. The proposed SIDO modules form the power management function to supply the UWB system with different operation modes for enhancing the total system efficiency containing power management and UWB.

V_{OB}, V_{OC}, and V_{OD}. The two-bit signal V_{MAT} is used to indicate the supply function of the two SIDO modules. The single-phase operation of the two SIDO modules is achieved by the energy-conservation mode (ECM) control, whereas the interleaving-ECM (IECM) control is activated in the data transmission period enabled by the signal V_{DT} generated from the UWB system. The IECM control also provides large supply power and minimizes output voltage ripple through the current interleaving mechanism.

Power management can vary the supply voltages to meet the distinct power requests in the UWB system with different operation modes according to the throughput constraint. During the silent mode, there are no data in the vacant transmission time slot. Thus, the power request is low, and only the slave SIDO module operates in order to reduce power dissipation as well as shutdown the master SIDO module to extend battery life. The voltages V_{OC} and V_{OD} generated from the slave module are set to 1.5 V and 1 V, respectively, to supply the awaiting circuit in the UWB system. The master module is activated in the upcoming period of data transmission. The output voltages, V_{OA} and V_{OB}, are raised to 1.8 V and 1.2 V to supply the radio frequency (RF) circuits and digital circuits, respectively. The voltages, V_{OC} and V_{OD}, yielded from the slave module can be raised up to 1.8 V and 1.2 V, respectively, to form an interleaving operation for large driving capability. The current balance mechanism can guarantee the current matching to ensure the equivalent power delivery ability of the two SIDO modules. Aside from this, a green-mode operation is implemented to decrease power dissipation of UWB. According to the UWB protocol for supporting multiple low-power modes, the standby and hibernate modes can be used during data transmissions. Thus, the slave SIDO module can scale down the output voltages, V_{OC} and V_{OD}, back to 1.5 V and 1 V, respectively, for some low-power blocks. In the proposed power management design, green-mode would be activated if the interval between two data transmission period in UWB is shorter than 1 ms since the re-startup procedure of the proposed SIDO module needs the response time about 0.1 ms. Moreover, it can enhance the system efficiency containing the power management and UWB owing to the reduction of the power consumption.

The brief comparison of the power management implementation is listed in Table I. The proposed SIDO module with the single phase ECM control and the interleaving operation derived from IECM is a suitable solution to supply the UWB system under the different operation modes. In this paper, the structure of a SIDO converter is described in Section II. The ECM controlled single-phase and interleaving operations with the IECM control are illustrated in Section III. Detailed circuit implementations of the SIDO converter are discussed in Section IV. Experimental results and the 3-D inductor integration are presented in Section V. Finally, the conclusion is given in Section VI.

II. Proposed SIDO Converter Structure

The structure of the proposed SIDO converter is shown in Fig. 2. The control circuits in the proposed SIDO converter are all implemented using 65 nm deep-submicron devices with a 1.2 V voltage supply [16], V_{core}. Thus, low power consumption and small silicon area are achieved.

The power stage is composed of four power switches, M_{S1}–M_{S4}, for the dual step-down outputs. These power switches are implemented by the I/O devices in 65 nm process for high voltage tolerance. It has four different energy delivery paths to transfer energy from the battery, $V_{\rm IN}$, to the dual outputs with only one inductor used. Sensor gains are decided by two voltage dividers that contain R_{A1}, R_{A2}, R_{B1}, and R_{B2} for the feedback of output voltage information to the two cascade error amplifiers [16], which yields high DC voltage gain under the low voltage operation. The two error current signals, I_{EA} and I_{EB}, generated by voltage-to-current (V-to-I) converters at the output of two EAs, are sent to the ECM controller to decide the duty ratio of the dual outputs. The current I_{EAB}, which is the summation of I_{EA} and I_{EB}, indicates the peak

TABLE I
BRIEF COMPARISON OF THE POWER MANAGEMENT IMPLEMENTATIONS FOR UWB SYSTEM

Power management for UWB system		SISO (Current-mode)	**SIDO (ECM or IECM)**	SIDO (PCCM)
Outputs type		Buck	**Buck**	Buck
Required outputs	Key Specifications			
4 Outputs (Green-mode) (Light load)	Num. of off-chip inductor	4	**2**	2
	Num. of off-chip capacitor	4	**4**	4
	Output voltage ripple	Small	**Small**	Medium
	Driving capability for outputs	Large	**Medium**	Medium
2 Outputs (Data transmission) (Heavy load)	Num. of off-chip inductor	2	**2**	1
	Num. of off-chip capacitor	2	**2**	2
	Output voltage ripple	Small	**Small**	Large
	Driving capability for outputs	Large	**Large**	Medium

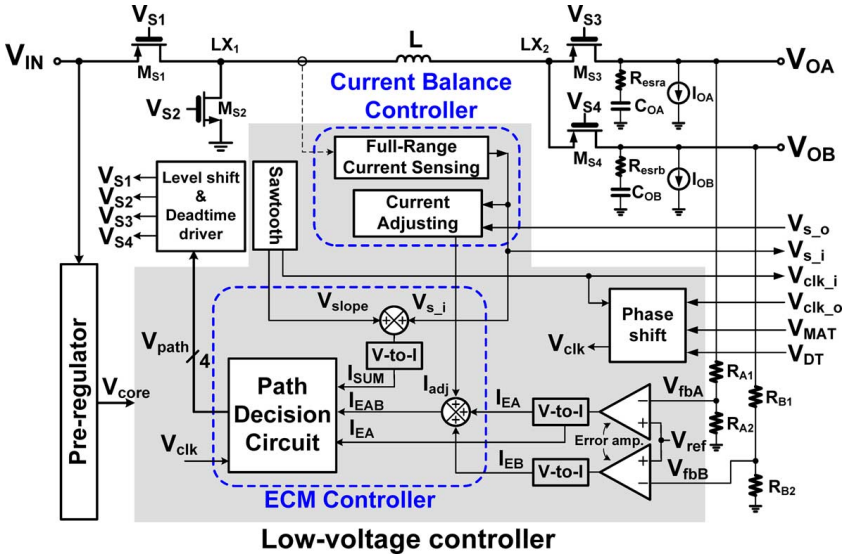


Fig. 2. Structure of the proposed SIDO converter with the IECM control.

inductor current as well as the required energy in one switching cycle through the ECM control. Therefore, by using the ECM controller, the average inductor current is lowered to equal the summation of the two output load currents. In addition, I_{EAB} is adjusted by the current adjusting signal I_{adj} to ensure the current matching in the IECM control with the interleaving operation. I_{adj} is generated from the current adjusting circuit in the current balance controller. It can adjust the inductor current levels of each SIDO module in the interleaving operation.

The current sensing signal, V_{s_i}, generated from the current sensing circuit is added to a slope compensation signal, V_{slope}, to avoid sub-harmonic oscillation [17]. Hence, the currents, I_{SUM}, I_{EAB}, and I_{EA} are used to determine the four-bit signal, V_{path}, in the path decision circuit. Additionally, the current sensing signal V_{s_o}, which is derived from the current sensing of the other SIDO module, and V_{s_i} are used to achieve the current balance when the IECM control is activated. Moreover, V_{clk_i} is generated from the sawtooth circuit, and V_{clk_o} is derived from the other SIDO converter. Thus, the phase shift circuit can generate system clock V_{clk} to accomplish the interleaving operation. The level-shift and deadtime driver circuit produces the control signals, V_{S1}-V_{S4}, from the four-bit signal V_{path} to drive the power switches due to the use of low-voltage controller. The level-shift circuit can enhance the driving ability of power switches by increasing the gate driving voltages. The deadtime circuit can prohibit the simultaneous on-state to avoid the shoot-through current between power switches M_{S1} and M_{S2}.

III. IECM OPERATION

For high efficiency operation in the UWB system, single-phase and interleaving operations are included in the proposed SIDO converter. Thus, the integration of the two SIDO converters can provide either four different output voltages in the green-mode period or two distinct output voltages with high driving capability in the data transmission period.

A. Single-Phase Operation – ECM Control

Fig. 3 shows the energy delivery paths of the SIDO converter. The four energy delivery paths, path-I to path-IV, constitute distinct inductor current slopes. Path-I and path-III indicate the inductor charging path and deliver energy from the input to the outputs V_{OA} and V_{OB}, respectively. Path-II and path-IV indicate the inductor discharging path and deliver energy from the inductor to the outputs V_{OA} and V_{OB}, respectively. The proposed ECM control, which uses one of the combinations of these possible energy delivery paths, can achieve the CCM dual buck operations with a minimum average inductor current level.

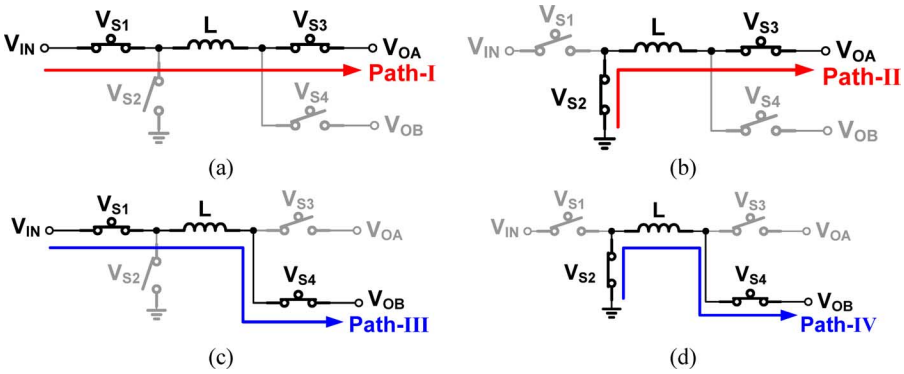


Fig. 3. Energy delivery paths in the power stage of the SIDO converter.

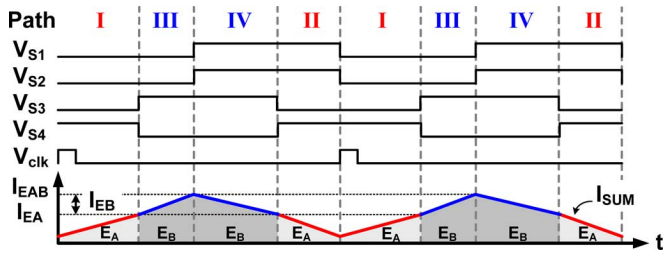


Fig. 4. The time diagram of the proposed ECM control.

Fig. 4 shows the time diagram of the ECM control with the order of path-I, path-III, path-IV, and path-II. This ordered sequence circulates by the triggering of the system clock, V_{clk}. I_{EAB}, which is decided by the summation of the two error signals, I_{EA} and I_{EB}, indicates the peak inductor current. The error signal I_{EA} determines the transitions from path-I to path-III and from path-IV to path-II. That is, the Path-I and Path-II are decided by I_{SUM} and I_{EA} for the output V_{OA}. Similarly, the Path-III and Path-IV are decided by I_{SUM} and I_{EB}, which is the difference between I_{EAB} and I_{EA}. The ECM control can achieve the separated dual step-down operations with the superposition scheme. Thus, each output can receive battery power in one PWM switching period through the ECM control. Besides, each power switch, M_{S1} to M_{S4}, would switch twice in the period of one switching cycle time with the ordered energy delivery paths.

Fig. 5 illustrates the inductor current waveform under different load conditions with the ECM control. The combination of the two separated step-down operations in ECM control results in the average inductor current, I_{L,avg_ECM}, to be equal to the summation of the two output loads. The value of I_{L,avg_ECM} is lower than that of I_{L,avg_PCCM} derived from the PCCM control, which needs a freewheel stage to regulate the inductor current. As such, the ECM control can yield a low average inductor current level to reduce conduction loss and enhance efficiency by removing the freewheel stage. Moreover, the duty cycle of each regulated output voltage varies depending on the loading in the ECM control. For example, if the load current I_{OB} of the output voltage V_{OB} increases and the load current I_{OA} of the output voltage V_{OA} is fixed, there would be an increase in total output power. Thus, the average inductor current of the ECM control I_{L,avg_ECM} arises to reflect the heavy load condition. The total energy E_A for V_{OA} in Fig. 5 must keep constant at both light load and heavy load conditions since I_{OA} would not change. On the other hand, the total energy E_B for V_{OB} should be increased to provide a sufficient power owing to the increase of I_{OB}. As a result, the periods of path-I and path-II are reduced, but the periods of path-III and path-IV are extended because of the increase in I_{L,avg_ECM}. Moreover, the effect from PVT condition to the proposed ECM control can be minimized since the high gain error amplifiers [16] are used to compensate these variations. They modulate the error signals properly to ensure the correct function of ECM control. Consequently, adequate energy is delivered to the outputs to satisfy the output loads. In other words, the low value of I_{L,avg_ECM} greatly enhances the power conversion efficiency in ECM control owing to the use of superposition technique. Furthermore, the derivation of the minimum average inductor current level helps reduce the output voltage ripple to better the supply quality of the proposed SIDO converter.

B. Interleaving Operation – Interleaving ECM (IECM) Control

The increase in load current can cause a large output voltage ripple due to the discontinuous inductor current derived at the output nodes of the SIDO converter. Thus, to better enhance the performance at heavy loads, the IECM control is utilized for a power management function to the UWB system. That is, the interleaving operation focuses on providing a large power supply during the data transmission period. The interleaving scheme for the UWB system is depicted in Fig. 1. When the interleaving operation is enabled during the data transmission period, V_{OC} is paralleled to V_{OA} to provide a large supply power to the RF PA and Mixer circuit in the UWB system. Similarly, V_{OD} is paralleled to V_{OB} to simultaneously deliver energy to the digital circuit in the UWB system. The power management (PM) master in the UWB processor activates the interleaving operation of the two SIDO modules and decides the power management functions according to the demand with different UWB operation modes.

The interconnection of the control signals between the two SIDO modules is also shown in Fig. 1. To achieve current matching and output voltage ripple minimization, some control signals between the two SIDO modules should be adequately

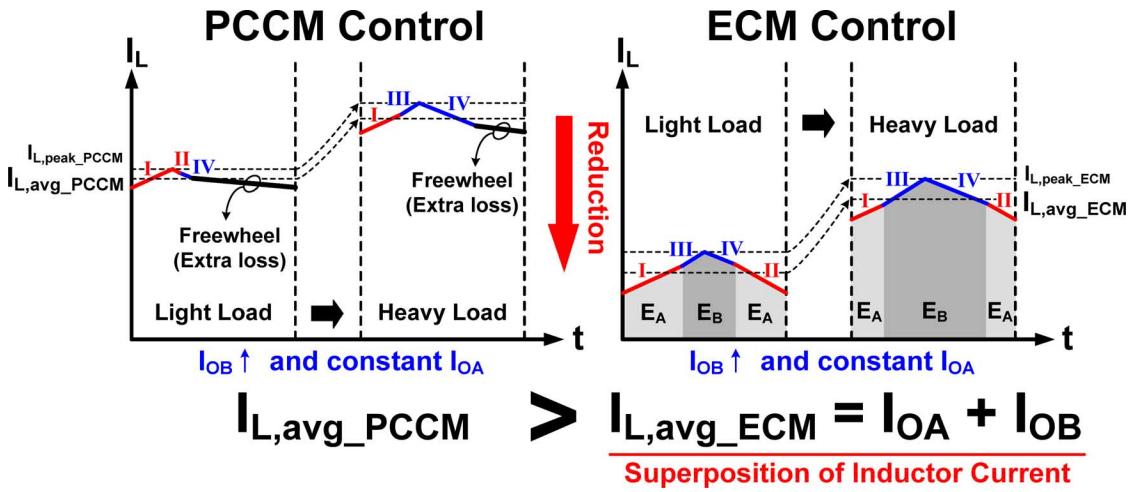


Fig. 5. The inductor current waveform under different load conditions with different control methods.

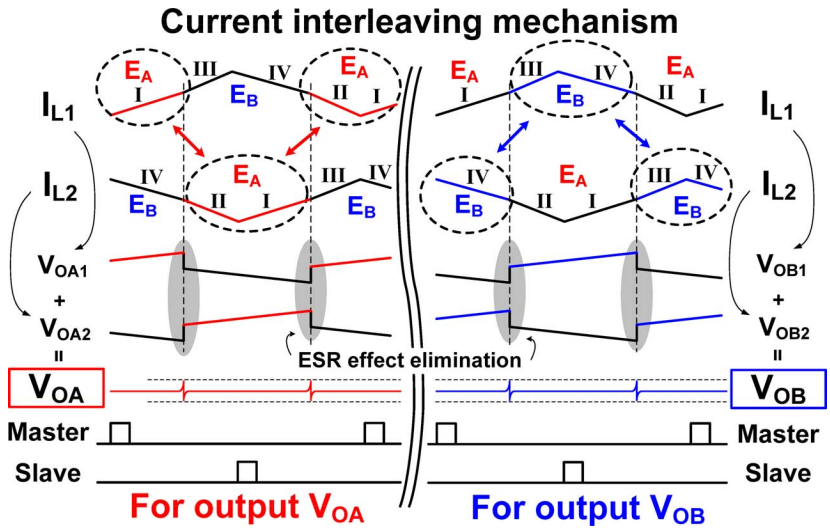


Fig. 6. The current interleaving mechanism in the proposed IECM control during the interleaving operation.

linked together to achieve the interleaving operation. Two signals of V_{s_i} and V_{s_o} generated from different current sensing circuits are used to achieve the current balance. In each SIDO module, the V_{s_i} signal indicates the current sensing signal of the SIDO module itself, whereas the V_{s_o} signal represents the current sensing signal generated from the other SIDO module. Similarly, the signal, V_{clk_i} obtained from the SIDO module itself and V_{clk_o} obtained from the other SIDO module, are utilized to adjust the phase difference between the two SIDO modules.

The detailed current interleaving mechanism in the interleaving operation is shown in Fig. 6. I_{L1} is the inductor current of the master module, whereas I_{L2} is the inductor current of the salve module. The single-phase SIDO converter has to provide energy for two output nodes, which results in a discontinuous inductor current at each output nodes. Through the interleaving operation of the two proposed SIDO modules, the two separated inductor currents interleave with each other so that the output current appears to be a continuous function. That is, with the current interleaving mechanism, V_{OA} derives energy from I_{L1} and I_{L2} through the different phase operations. It helps inductor current be continuous at the node V_{OA}. Furthermore, the existence of the parasitic equivalent series resistance (ESR) in the output capacitor also causes a large output voltage ripple due to the discontinuous inductor current in the single-phase operation. Nevertheless, the interleaving operation can produce the continuous inductor current by current interleaving to minimize the output voltage ripple. The glitches carried out by the ESR can also be cancelled naturally. Additionally, if the load I_{OA} increases during the interleaving operation, the error signals I_{EA} and the peak signals I_{EAB} in each SIDO modules are also increased. Thus, both of the average inductor current in each SIDO module is raised to supply the output load simultaneously. Moreover, the current adjusting circuit in the current balance controller shown in Fig. 2 ensures the current matching in the interleaving operation. The current adjusting signal I_{adj} is used to slightly adjust the inductor current level of the two SIDO modules for guaranteeing the current matching. As a result, the interleaving operation is a way of suppressing the output voltage ripple as well as of providing high power driving capability to supply the UWB system.

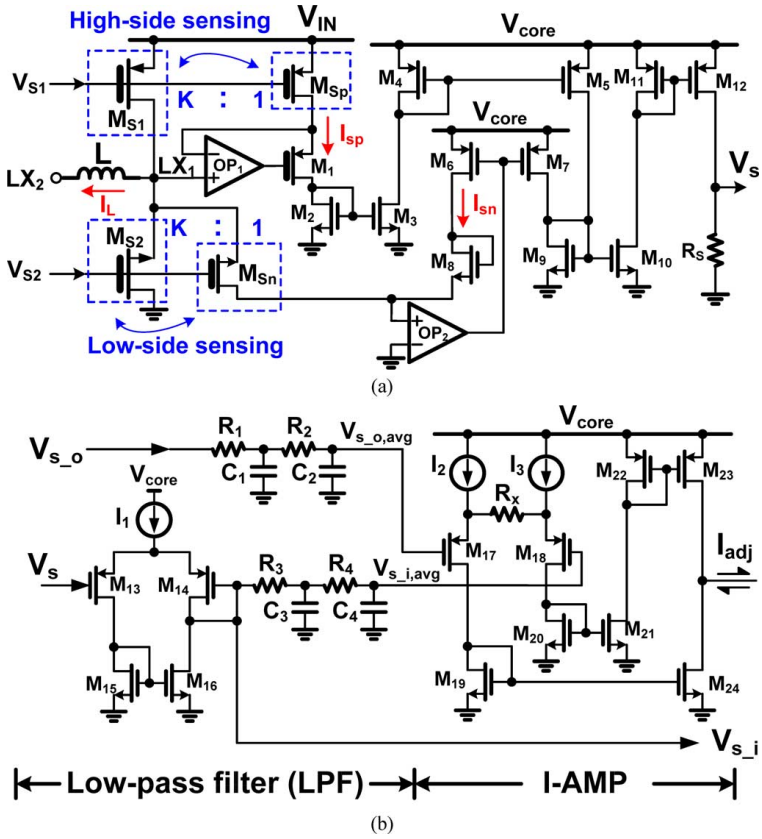


Fig. 7. The current balance controller circuit. (a) Full-range current sensing circuit. (b) Current adjusting circuit.

IV. Circuit Implementation

A. Current Balance Controller

Fig. 7 shows the current balance controller containing the full-range current sensing circuit and the current adjusting circuit. The inductor current information is necessary for ECM or IECM control owing to the current-mode operation. The full-range current sensing is utilized to achieve the four different energy delivery paths with the superposition technique in the proposed SIDO converter.

Fig. 7(a) shows the schematic of the full-range current sensing circuit. I_L is the current flowing through the inductor and K is the sensing factor of both M_{S1} to M_{Sp} and M_{S2} to M_{Sn}. These four transistors are all implemented by I/O devices for high voltage tolerance. The transistor M_{Sp} produces the sensing current during the turn-on period of the high-side power switch M_{S1}. The source-to-drain voltages of M_{S1} and M_{Sp} are approximately equal because of the closed-loop generated by the operational amplifier OP_1. Accordingly, the current I_{sp} flowing through the transistors M_{Sp} becomes proportional to the current flowing through the M_{S1}, thus achieving the high-side current sensing. Identically, the transistor M_{Sn} produces the inductor current information during the low-side turn-on period. The closed-loop generated by the operational amplifier OP_2 carries out a sensing current I_{sn} flowing through the transistor M_6 and the sensing transistor M_{Sn}. Therefore, the full-range current sensing signal V_s, which is the voltage across the sensing resistor R_s, is generated through the summation of the two sensing currents, I_{sp} and I_{sn}. The description is shown in (1).

$$V_s = (I_{sp} + I_{sn})R_S = \frac{I_L}{K}R_S. \tag{1}$$

Current balance mechanism between the two SIDO modules is implemented to ensure equivalent driven capability when the IECM control is activated for interleaving operation. As shown in Fig. 7(b), the current adjusting circuit, which is composed of the low-pass filter (LPF) and the current amplifier (I-AMP), is adopted to adjust the inductor current level of the two interleaved SIDO modules. The full-range current sensing signal V_s is buffered for transmission to the other SIDO module through the signal, V_{s_i}. Similarly, the sensing signal V_{s_o} is generated from the other SIDO module. The buffer stage eliminates the load effect and also filters out the switching noise. Hence, these two full-range current sensing signals are filtered by the LPF to obtain the average inductor current of each SIDO module in the interleaving operation. Additionally, the capacitors, C_1 to C_4, in the LPF are implemented by the capacitor multiplier technique to achieve the fully on-chip integration [11]. The average inductor current information of the two SIDO modules, $V_{s\_i,avg}$ and $V_{s\_o,avg}$, are sent to the I-AMP circuit to generate an adjusting current I_{adj} to achieve the current balance when the IECM control is activated. An auxiliary resistor R_x in the I-AMP circuit can strengthen the linearity of I_{adj}. The illustration of the absolute value of I_{adj} is shown in (2).

$$|I_{adj}| = 2 \cdot \frac{V_{s\_i,avg} - V_{s\_o,avg}}{R_x}. \tag{2}$$

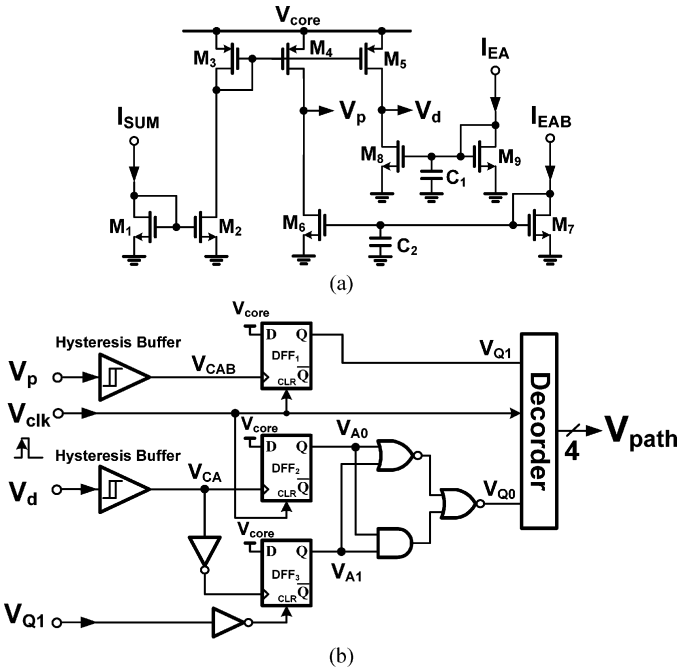


Fig. 8. The path decision circuit. (a) Current comparator. (b) Path decision logic.

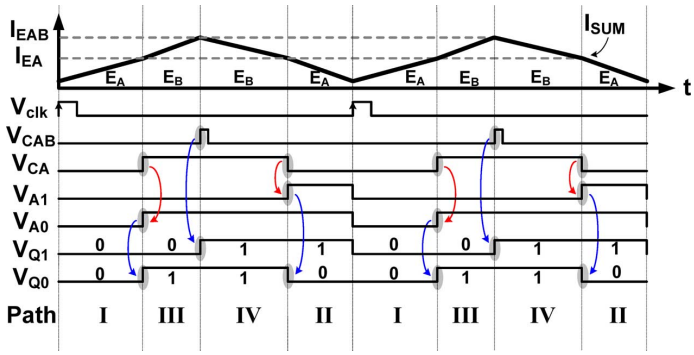


Fig. 9. Timing diagram of the path decision circuit.

B. ECM Controller

As shown in Fig. 8, the path decision circuit in the ECM controller, which contains the current comparator and the path decision logic, generates duty cycles to the two outputs in one SIDO module. The current comparator shown in Fig. 8(a) operates with I_{EA}, I_{EAB} and I_{SUM}. The values of V_p and V_d used to indicate the transition of energy delivery paths are decided by the intersection of I_{SUM} with I_{EAB} and I_{EA}, respectively.

The path decision logic depicted in Fig. 8(b) generates the four-bit V_{path} signal to achieve the energy delivery paths. The hysteresis buffer enhances the noise immunity of the current comparator to get a robust ECM control. As the illustration of timing diagram shows in Fig. 9, V_{clk} triggers the PWM switching as well as energy delivery path-I. V_{CA} is set to high when I_{SUM} intersects I_{EA} during the inductor charging period. Thus, the energy delivery path is changed from path-I to path-III. In addition, V_{CAB} is triggered to realize the path transition from path-III to path-IV when I_{SUM} reaches I_{EAB}. Moreover, path-II is carried out when I_{SUM} intersects I_{EA} again. The energy delivery path is swapped from path-IV to path-II with a negative edge voltage trigger provided by V_{CA}. Finally, path-II appears until the occurrence of the next V_{clk}, thus initialing the next PWM switching. The stages of the current comparator are minimized by using D-flip-flops due to the path decision logic. Furthermore, V_{Q1} and V_{Q0} indicate the energy delivery paths with binary code, which can be decoded through the decoder to generate a four-bit V_{path} signal to achieve the ECM control.

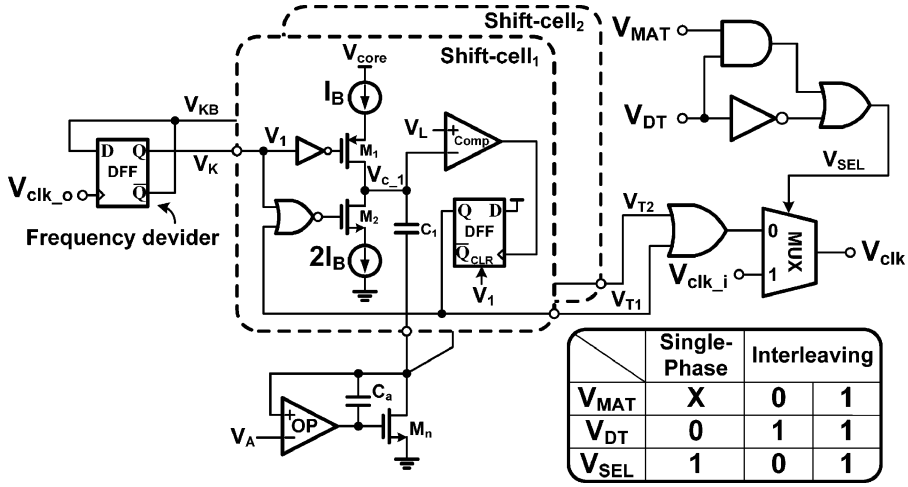
C. Phase Shift Circuit

The IECM control interconnects the two SIDO modules to provide a large power supply and minimize the output voltage ripple simultaneously. Thus, the system clocks in the two SIDO modules must be out of phase to achieve the current interleaving mechanism effectively. The proposed phase shift circuit shown in Fig. 10 produces the system clock V_{clk}, which is relative to the interconnected signals, V_{clk_i} and V_{clk_o}, generated from the two distinct SIDO modules. In addition, once V_{DT} activates the interleaving operation, V_{MAT} from the PM master in the UWB system will indicate either the master or slave function to each SIDO modules.

Fig. 11 shows the timing diagram of the phase shift circuit. In a single-phase operation, V_{DT} is set to low, and V_{clk} is derived from V_{clk_i} through the selection of a multiplexer. V_{clk} is also directly obtained from V_{clk_i} when one SIDO converter is utilized as the power management master in the interleaving operation. The V_{MAT} signal is set to high to indicate the master power management module. However, the SIDO module is pronounced a slave module if the V_{MAT} is set to low. V_{clk} is generated from the two shift-cells in order to obtain an out-of-phase operation to reduce the output voltage ripple. That is, V_{clk_o} is linked to the system clock V_{clk} of the master module through the interconnections and generates the signals V_K and V_{KB} by the frequency divider. V_K and V_{KB} trigger the shift-cells and acquire the sawtooth waveforms, V_{c_1} and V_{c_2}. When the signal V_K is set to high, the switch M_1 in the $shift\text{-}cell_1$ circuit is on in order to charge the capacitor C_1 with a fixed current I_B. On the contrary, C_1 is discharged with the current $2I_B$, until the V_{c_1} reverts to the value of V_L. The amplitude of the sawtooth waveform is V_{pp}. This operation is illustrated in (3).

$$T = \frac{C_i V_{pp}}{I_B} \text{ and } t_i = \frac{C_i V_{pp}}{2I_B} \text{ where } i = 1, 2. \quad (3)$$

The D-flip-flop detects when the discharge period is over. V_{T1} is set to high at the half period location with V_{clk_o}. Similarly, V_{T2} is produced through the identical operation mechanism in the $shift\text{-}cell_2$ circuit triggered by V_{KB}. By the equations shown in (3), t_1 and t_2 are equal to $T/2$, which is used to assure the interleaving operation. Finally, V_{clk} is carried out by the OR operation from V_{T1} and V_{T2} in the slave SIDO module to achieve the interleaving operation. Moreover, the bottom plates of capacitor C_1 in each shift-cell are fixed to a constant voltage V_A decided by the buffer stage, which is composed of the operational amplifier and the transistor M_n. This design helps avoid the voltage nonlinear phenomenon in the charging and discharging periods owing to the MOSFET as a capacitor. The interleaving operation with IECM control is shown in Fig. 12 that demonstrate the



	Single-Phase	Interleaving	
V_{MAT}	X	0	1
V_{DT}	0	1	1
V_{SEL}	1	0	1

Fig. 10. The phase shift circuit for interleaving operation.

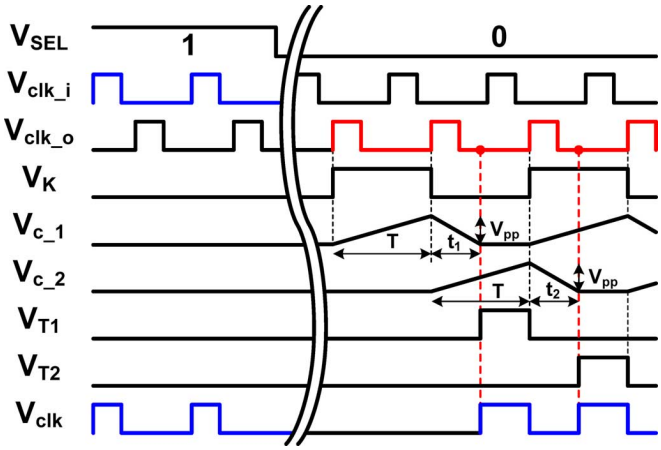


Fig. 11. Timing diagram of the phase shift circuit.

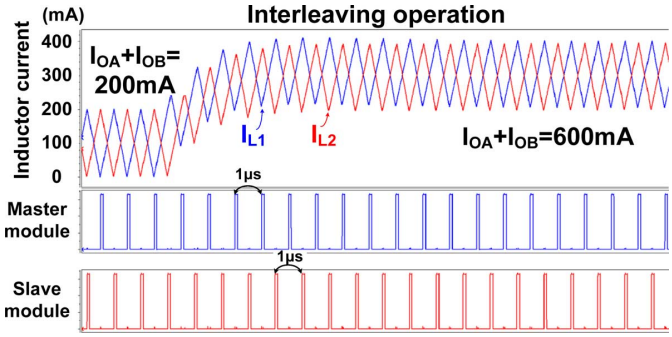


Fig. 12. The interleaving operation with the IECM control in the proposed SIDO modules.

current matching in load transient response and the operation of the phase shift circuit.

V. Experimental Results

This proposed SIDO converter with the IECM control was fabricated by 65 nm CMOS technology. The measured waveforms of the single-phase operation are shown in Figs. 13–15. Fig. 13 demonstrates the single-phase operation in steady-state with V_{OA} of 1.8 V and V_{OB} of 1.2 V. The energy delivery paths

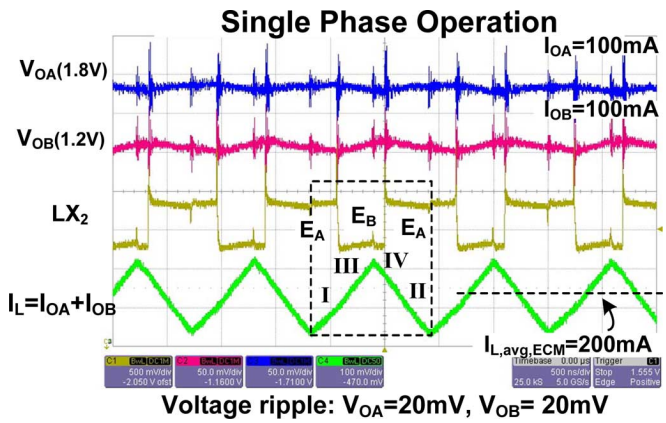


Fig. 13. Measured single-phase operation of ECM control with $I_{OA} = 100$ mA and $I_{OB} = 100$ mA.

in the ECM control are verified through the occurrence of path-I, path-III, path-IV, and path-II in sequence. With a load current of 100 mA at each output, the average inductor current is continuously maintained at 200 mA, which is equal to the summation of the two output loads. The output voltage ripple is about 20 mV at each output due to the discontinuous inductor current. When each output has 200 mA load current, the measured single-phase operation with the ECM control is also achieved through the ordered energy delivery paths shown in Fig. 14. Similarly, the average inductor current is equal to the summation of the two output load currents. The output voltage ripple is about 30 mV at each output. Fig. 15 shows the measured load transient response in single-phase operation. The largest output drop voltage is about 80 mV, whereas the largest overshoot voltage is about 60 mV. The voltage recovery time is derived within 30 μs. In addition, good voltage regulation and fast transient response are also achieved because of the high dc loop gain and bandwidth. The average inductor current is always equal to the summation of two output loads by the ECM control. Thus, the minimum inductor current level is achieved through the superposition technique to enhance the power conversion efficiency and reduce the output voltage ripple.

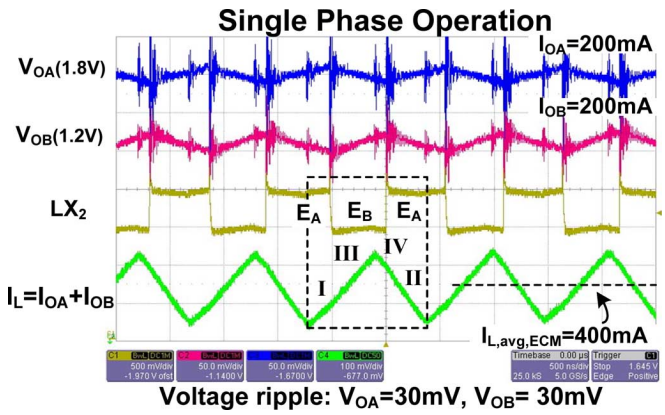


Fig. 14. Measured single phase-operation of ECM control with $I_{OA} = 200$ mA and $I_{OB} = 200$ mA.

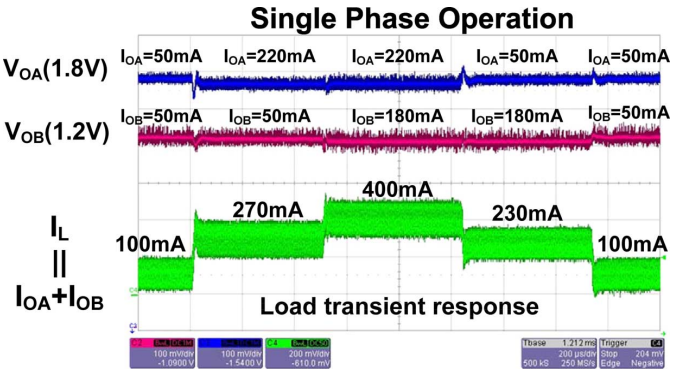


Fig. 15. Measured single-phase operation in case of load transient response.

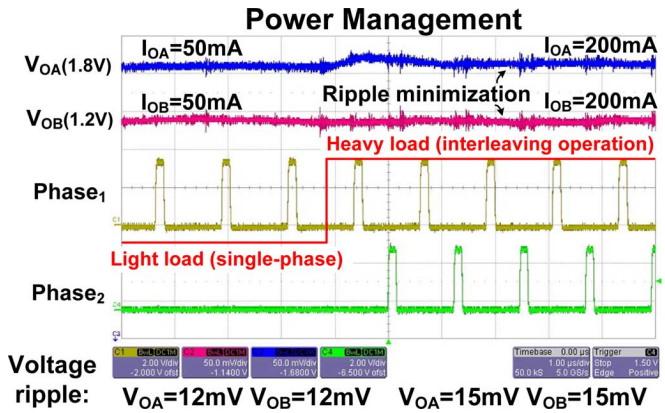


Fig. 16. Measured interleaving operation of the power management integration.

Fig. 16 shows the measured waveform of the power management function. When the UWB system enters the data transmission period, an increase in the power request activated the IECM control to provide a large driving capability simultaneously from the two interleaving SIDO modules. Moreover, owing to the current interleaving mechanism, the output voltage ripple is greatly reduced, and the voltage spike resulting from the ESR is nearly eliminated. The output voltage ripple is reduced to 15 mV at each output with 200 mA output load current.

The measured power conversion efficiency of the single-phase operation is shown in Fig. 17. The conduction loss of the power switches can be greatly reduced owing to the proposed ECM control. Peak efficiency increases to 91%, where the 80% efficiency is achieved by today's commercial products with four power switches. The comparison of the output voltage ripple with different loads is shown in Fig. 18. Output voltage ripple in the ECM control decreases by as much as 36% compared with that in the PCCM control. Specifically, a 50% reduction in the output ripple is presented at heavy loads because of the current interleaving with the IECM control. The design specifications of the proposed SIDO converter are listed in Table II. Moreover, the comparisons of the prior SIDO methodologies are shown in Table III.

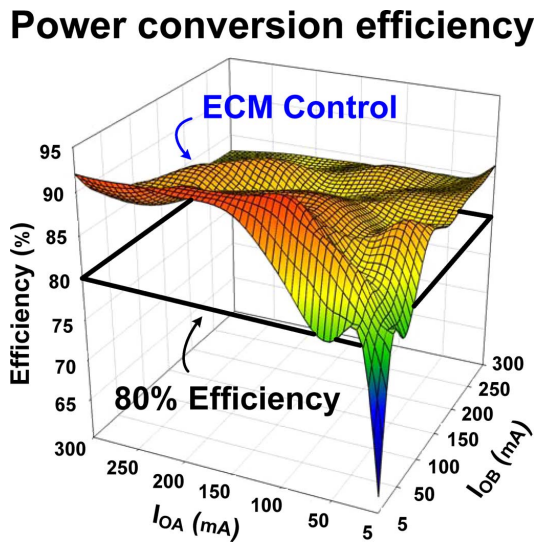


Fig. 17. Measured power conversion efficiency in the single-phase operation with $V_{IN} = 3.3$ V, $V_{OA} = 1.8$ V, and $V_{OB} = 1.2$ V.

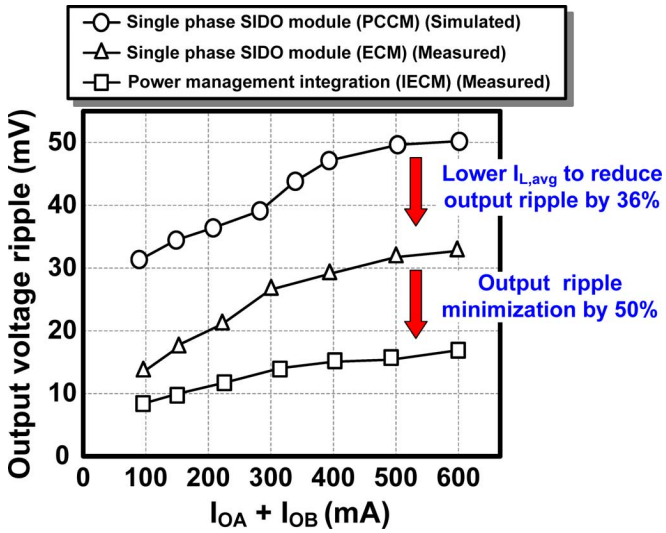


Fig. 18. The comparison of the output voltage ripple by using different control methods with $V_{IN} = 3.3$ V, $V_{OA} = 1.8$ V, and $V_{OB} = 1.2$ V.

Fig. 19 shows a chip micrograph and the illustration of a 3-D package. The occupied silicon area of the single SIDO module is 1.44 mm^2. The inductor is placed on the top of the power management ICs to shorten the distance of the bounding wire. The performance is enhanced through the alleviation of the bond wire effect since the length of the bonding wire is short-

TABLE II
DESIGN SPECIFICATIONS OF THE PROPOSED SIDO CONVERTER

Process	65 nm CMOS process			
Input voltage	2.7 V – 3.6 V			
Switching frequency	1 MHz (nominal)			
Chip size (SIDO module)	1600 µm x 900 µm			
Modules	Master module		Slave module	
Inductor / DCR	4.7 µH / 250 mΩ (nominal)		4.7 µH / 250 mΩ (nominal)	
Outputs	V_{OA} = 1.8 V	V_{OB} = 1.2 V	V_{OC} = 1.5 V	V_{OD} = 1 V
Output capacitor / ESR	4.7 µF / 30 mΩ	4.7 µF / 30 mΩ	4.7 µF / 30 mΩ	4.7 µF / 30 mΩ
Cross Regulation	0.1 A ➔ 0.3 A 0.3 A ➔ 0.1 A	10 mV 8 mV	0.1 A ➔ 0.3 A 0.3 A ➔ 0.1 A	12 mV 6 mV
	12 mV 15 mV	0.1 A ➔ 0.3 A 0.3 A ➔ 0.1 A	11 mV 12 mV	0.1 A ➔ 0.3 A 0.3 A ➔ 0.1 A
Output ripple (Single phase)	< 32 mV			
Output ripple (Interleaving operation)	< 16 mV			

TABLE III
COMPARISON OF THE PREVIOUS SIDO (SIMO) METHODOLOGIES

	This work (ECM control)	CICC 2009 [3]	JSSC 2003 [4]	JSSC 2009 [8]	CICC 2009 [10]
Technology	65 nm CMOS	0.35 µm CMOS	0.5 µm CMOS	0.25 µm CMOS	0.25 µm CMOS
Supply voltage	2.7 – 3.6 V	1.8 – 2.4 V	1.25 – 2.25 V	1.8 – 2.2 V	2.7 – 5 V
Switching frequency	1 MHz	1.25 MHz	1 MHz	660 kHz	1.3 MHz
Outputs	2 Buck	2 Boost	2 Boost	2 Buck, 2 Boost	2 Buck
Inductor	4.7 µH	1 µH	1 µH	10 µH	4.7 µH
Output capacitor	4.7 µF	4.7 µF	33 µF	33 µF	47 µF
Output voltage ripple	< 32 mV	< 160 mV	< 25 mV	< 22 mV	< 30 mV
Load current (max.)	0.3A / 0.3A	0.4A / 0.2A	0.12A / 0.1A	N/A	0.25A / 0.26A
Transient voltage drop	80 mV (ΔI_{load}=0.17A)	500 mV (ΔI_{load}=0.2A)	N/A	N/A	36 mV (ΔI_{load}=0.27A)
Transient settling time	25 µs / (ΔI_{load}=0.17A)	100 µs (ΔI_{load}=0.2A)	N/A	N/A	10 µs (ΔI_{load}=0.27A)
Load-regulation	< 10 %	< 20 %	N/A	< 2 %	< 5%
Cross-regulation	< 8 %	< 10 %	N/A	< 0.35 %	< 5%
Peak efficiency	91 %	87.8 %	89.4 %	93 %	87 %
Chip area	1.44 mm^2	2.21 mm^2	4.25 mm^2	3.78 mm^2	5.29 mm^2

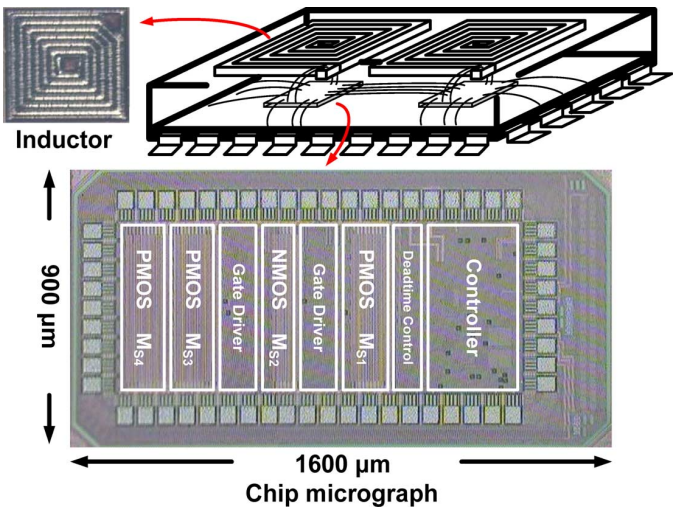


Fig. 19. The chip micrograph and the illustration of inductor integration.

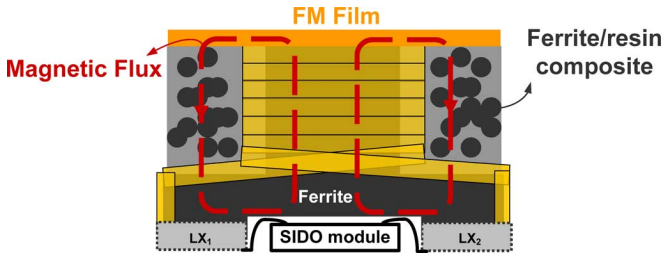


Fig. 20. The details of the inductor integration.

ened as well as the equivalent bond wire inductance. It minimizes the switching noise and voltage spike resulting from the power stage. The details of the inductor integration are given in Fig. 20. Chip function is affected by the magnetic flux generated from the inductor. However, a magnetic flux produced by conductive coil cannot be blocked by insulating it from its surrounding materials [18]. Nevertheless, the magnetic field can be a short-circuited in place of the high permeability magnetic material, which provides an easy path with low reluctance for the return magnetic flux to form a closed magnetic circuit. Therefore, the magnetic flux would propagate along the high permeability material, which is composed of the ferrite and fer-

rite-magnet (FM) film and ferrite/resin composite, to largely decrease the interference to the chip function. In addition, relative to the ferrite and FM material, the permeability of air is low. Thus, the leakage flux and the magnetic field interference from the inductor can be minimized. Consequently, the integration of the inductor with the proposed SIDO converter achieves the area-efficient power management module and enhances the competitiveness to the UWB system or other system-on-a-chip applications.

VI. Conclusion

The proposed SIDO converter with IECM control was fabricated by 65 nm CMOS technology. The ECM control is achieved through the ordered energy delivery paths to power the UWB system. Besides, the superposition technique helps derive a minimum average inductor current, which is equal to the summation of two output loads. In addition, ICEM control is activated to realize the interleaving operation with current interleaving. Thus, a larger supply power can be provided during the data transmission period, and the output voltage ripple can be reduced owing to the current interleaving mechanism. Experimental results demonstrate the single-phase and interleaving operations of the proposed SIDO converter. A peak efficiency of 91% is achieved and the output voltage ripple appears notably minimized by over 50% through current interleaving at heavy load. The test chip occupies 1.44 mm^2 and integrates with a 3-D architecture for inductor integration.

References

[1] H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, and G.-H. Cho, "A single-inductor switching DC-DC converter with five outputs and ordered power-distributive control," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2076–2714, Dec. 2007.

[2] K.-S. Seol, Y.-J. Woo, G.-H. Cho, G.-H. Cho, J.-W. Lee, and S.-I. Kim, "Multiple-output step-up/down switching DC-DC converter with vestigial current control," in *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 442–443.

[3] X. Jing, P. K. T. Mok, and M. C. Lee, "A wide-load-range single-inductor dual-output boost regulator with minimized cross-regulation by constant-charge-auto-hopping (CCAH) control," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2009, pp. 299–302.

[4] D. Ma, W.-H. Ki, and C.-Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

[5] M.-H. Huang and K.-H. Chen, "Single-inductor dual buck-boost output (SIDBBO) converter adaptive current control mode (ACCM) and adaptive body switch (ABS) for compact size and long battery life in portable devices," in *IEEE Symp. VLSI Circuits Dig.*, 2009, pp. 164–165.

[6] M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovati, F. Maloberti, T. Peltola, and T. Teppo, "A 4-output single-inductor DC-DC buck converter with self-boosted switch drivers and 1.2 A total output current," in *IEEE ISSCC Dig. Tech. Papers*, 2008, pp. 444–445.

[7] C.-S. Chae, H.-P. Le, K.-C. Lee, G.-H. Cho, and G.-H. Cho, "A single-inductor step-up DC-DC switching converter with bipolar outputs for active matrix OLED mobile display panels," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 509–524, Feb. 2009.

[8] M.-H. Huang and K.-H. Chen, "Single-inductor multi-output (SIMO) DC-DC converters with high light-load efficiency and minimized cross-regulation for portable devices," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1099–1111, Apr. 2009.

[9] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, "A 200 mA 93% peak efficiency single-inductor dual-output DC-DC buck converter," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 526–527.

[10] W. Xu, Y. Li, X. Gong, Z. Hong, and D. Killat, "A single-inductor dual-output switching converter with low ripples and improved cross regulation," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2009, pp. 303–306.

[11] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008.

[12] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, Jan. 2004.

[13] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering skip modulation, width and dead time controllers in highly efficient DC-DC converters for system-on-chip applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2451–2465, Nov. 2007.

[14] Y. Qiu, X. Chen, and H. Liu, "Digital average current-mode control using current estimation and capacitor charge balance principle for DC-DC converters operating in DCM," *IEEE Trans. Power Electron.*, vol. 25, pp. 1537–1545, Jun. 2010.

[15] K. Viswanathan, R. Oruganti, and D. Srinivasan, "A novel tri-State boost converter with fast dynamics," *IEEE Trans. Power Electron.*, vol. 17, pp. 677–683, Sep. 2002.

[16] Y.-H. Lee, Y.-Y. Yang, K.-H. Chen, Y.-H. Lin, S.-J. Wang, K.-L. Zheng, P.-F. Chen, C.-Y. Hsieh, Y.-Z. Ke, Y.-K. Chen, and C.-C. Huang, "A DVS embedded power management for high efficiency integrated SoC in UWB system," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2227–2238, Nov. 2010.

[17] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[18] C. H. Ahn and M. G. Allen, "Micromachined planar inductors on silicon wafers for MEMS applications," *IEEE Trans. Ind. Electron.*, vol. 45, no. 6, pp. 866–876, Dec. 1998.

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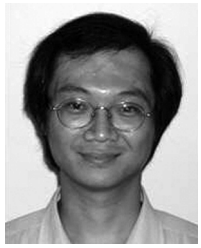

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