A 1-V, 16.9 ppm/°C, 250 nA Switched-Capacitor CMOS Voltage Reference

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***Abstract*—An ultra low-power, precise voltage reference using a switched-capacitor technique in 0.35-μm CMOS is presented in this paper. The temperature dependence of the carrier mobility and channel length modulation effect can be effectively minimized by using 3.3 and 5 V N-type transistors to operate in the saturation and subthreshold regions, respectively. In place of resistors, a precise reference voltage with flexible trimming capability is achieved by using capacitors. When the supply voltage is 1 V and the temperature is 80 °C, the supply current is 250 nA. The line sensitivity is 0.76%/V; the PSRR is −41 dB at 100 Hz and −17 dB at 10 MHz. Moreover, the occupied die area is 0.049 mm^2.**

***Index Terms*—CMOS voltage reference, nanocurrent, switched-capacitor.**

I. Introduction

HIGH-PRECISION and stable reference voltage circuits are widely used in digital and analog circuits like analog-to-digital converters, voltage regulators, DRAMs, flash memories, and other communication devices. The demands for smaller area, lower power consumption, and lower sensitivity to variations in supply voltage and temperature are increasing. The base-emitter voltage of bipolar transistors or the forward voltage of a pn-junction diode exhibits a negative TC. In addition, when two bipolar transistors operate at unequal current densities, the difference between their base-emitter voltages of bipolar transistors generate (is) directly proportional to the absolute temperature (PTAT). Thus, conventional reference voltage, which is about 1.2 V, exhibits little dependence on temperature while negative and positive temperature coefficients are added with proper weighting generated by resistors. The area of resistors, the noise from resistors, and the variations of resistors with temperature can influence the performance of reference voltage circuit. Furthermore, the supply voltage is necessary to be larger than 1.2 V to provide a traditional reference voltage circuit. Recently, several voltage reference circuits operating with low power supplies were published [1]–[5]. The reversed bandgap principle can effectively scales down the reference voltage to reduce the supply voltage. This structure requires parasitic BJTs and resistors that occupy large silicon area. To overcome these problems, the methods of utilizing MOS transistors operated in subthreshold region instead of BJTs to generate the voltage reference were invented to compensate the temperature coefficient and reduce the power dissipation [3]–[9]. However, when process variations are considered, some reference voltages produced by nanopower structures have significant temperature coefficients because trimming procedures have not been invented for these structures [7]–[9].

In general, switched-capacitor (SC)-based technique is one popular technique to eliminate the usage of large resistors and reduce the effect of offset voltage of operational amplifier. Fig. 1 shows a modified reference voltage by SC-based technique [10]. When $\varphi_1 = 1$ and $\varphi_2 = 0$, the equivalent circuit of Fig. 1 is described in Fig. 1(a). At node X, the charge transfer equation is shown as (1)

$$V_{BE2}(k+1)C_1 = -V_{\rm ref}C_3. \tag{1}$$

Similarly, when $\varphi_1 = 0$ and $\varphi_2 = 1$, the charge transfer equation of node X in Fig. 1(b) is derived as (2)

$$V_{BE1}kC_1 = -V_{\rm ref}C_2. \tag{2}$$

Combining (1) and (2), the $V_{\rm ref}$ voltage is written as (3)

$$V_{\rm ref} = \frac{C_1}{C_2 - C_3}\left(V_{BE2} + kV_T \ln\left(\frac{I_2}{I_1}\right)\right). \tag{3}$$

In this SC-based voltage reference circuit, the bipolar transistors are used to generate both temperature coefficients at the sacrifice of large silicon area. In addition, it needs eight switches and four capacitors to implement it and the switching power loss reduces the power efficiency of this reference voltage circuit. Therefore, this paper proposed a switched-capacitor voltage reference (SCVR) using pure CMOS to minimize the silicon area and temperature coefficient of the reference voltage. Furthermore, this circuit only needs nanoampere supply current, and the power supply voltage can be scaled down to 1 V. In Section II, the operating principle of the proposed SCVR circuit is described. Section III presents the detailed circuit implementation, including the biasing circuit and the op-amp circuit with the auto-zeroing. Design considerations are described in Section III. Trimming flexibility is discussed in Section IV, and measured results are shown in Section V to validate the design concept and performance. Finally, a conclusion is made in Section VI.

II. Operating Principle of Proposed SCVR Circuit

The structure of the SCVR circuit shown in Fig. 2 is composed of a low-power biasing circuit [8], a core circuit, switched capacitors, and an operational transconductance

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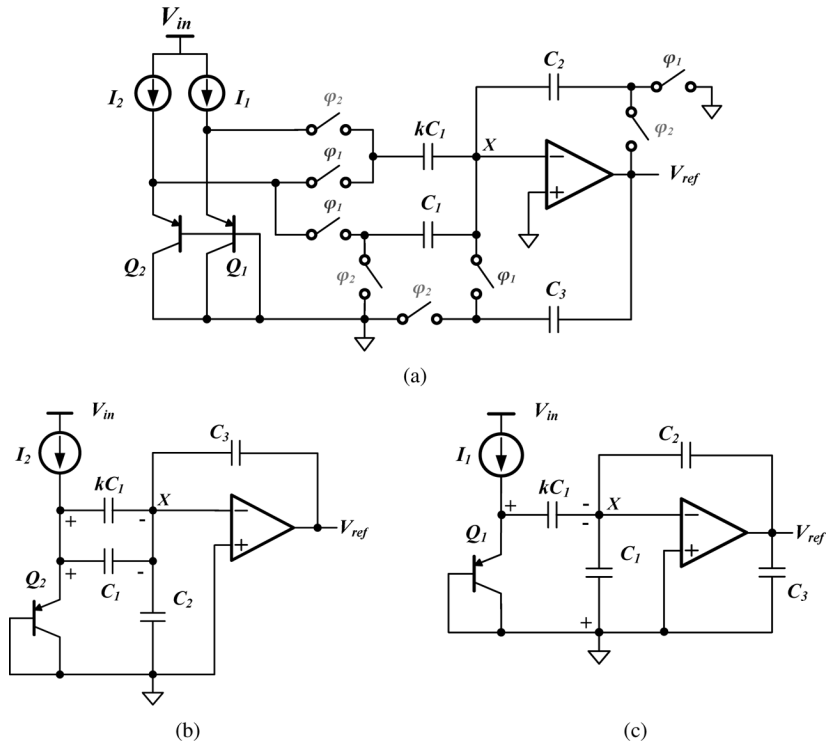

Fig. 1. (a) Prior art of switched-capacitor voltage reference. The equivalent circuits can be simplified as (b) when $\varphi_1 = 1$ and $\varphi_2 = 0$ and (c) when $\varphi_1 = 0$ and $\varphi_2 = 1$.

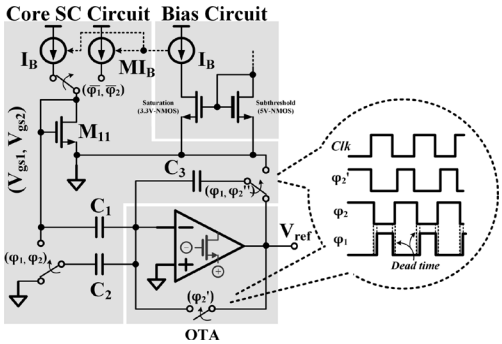

Fig. 2. Low power switched-capacitor voltage reference.

amplifier (OTA) [11] that uses the auto-zeroing technique to become insensitive to the offset voltage. The nonoverlapping clock signals (φ_1, φ_2, φ_2') are generated by the circuit in Fig. 3 to produce dead-time regions to avoid switching leakage for achieving high precision. The core circuit inputs V_{GS1} and V_{GS2} to the OTA during $\varphi_1 = 1$ and $\varphi_2 = 1$, respectively. The equivalent schematics of the SCVR circuit are shown in Fig. 4(a) and (b) when $\varphi_1 = 0$, $\varphi_2 = 1$ and $\varphi_1 = 1$, $\varphi_2 = 0$, respectively. In the first phase ($\varphi_1 = 0$ and $\varphi_2 = 1$), the current flowing through transistor M_{11} is $M \times I_B$ and the gate-source voltage V_{GS2} corresponding to a current $M \times I_B$ is stored on capacitors C_1 and C_2. The M is the current ratio of the different phases. In the second phase ($\varphi_1 = 1$ and $\varphi_2 = 0$), the current flowing through transistor M_{11} is equal to I_B, and the gate-source voltage V_{GS1} corresponding to current I_B is connected to C_1 while C_2 is grounded and C_3 is put into the negative feedback loop. From charge conservation, the OTA output express as (4)

$$V_{\text{ref}} = \frac{C_1}{C_3}\left(\left(1+\frac{C_2}{C_1}\right)V_{GS2} - V_{GS1}\right) = \frac{C_2}{C_3}V_{th} + \sqrt{\frac{2I_B}{u_n C_{ox}\left(\frac{W_{11}}{L_{11}}\right)}} \times \left(\frac{C_1(\sqrt{M}-1)+C_2\sqrt{M}}{C_3}\right). \tag{4}$$

V_{th} is the threshold voltage of transistor M_{11}, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, and W_{11} and L_{11} are the width and length of transistor M_{11}, respectively. Since the reference voltage appears in the second phase, the SCVR circuit uses a sample and hold circuit to store the reference voltage. In general, the threshold voltage V_{th} has negative temperature coefficient. That implies that the biasing current I_B has to be proportional to the square of the absolute temperature (PTAT^2) and cancel the temperature characteristic of electron mobility μ_n to compensate the temperature coefficient. Furthermore, the current is designed as a nanoampere current for reducing power consumption and the zero temperature coefficients can be achieved by carefully adjusting the values of capacitors C_1-C_3. The nanoampere current with PTAT^2 characteristic is discussed in detail in Section III.

III. Circuit Description

The proposed SCVR circuit is illustrated in Fig. 5. The biasing circuit formed by transistors M_1-M_8 exploits N-type transistors operating in different regions to produce the PTAT^2 current. Also, the biasing current is nearly independent of

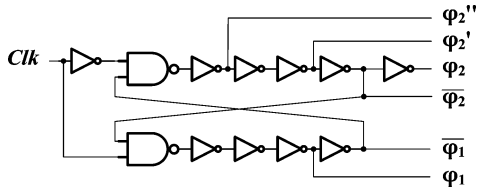

Fig. 3. Nonoverlapping control circuit.

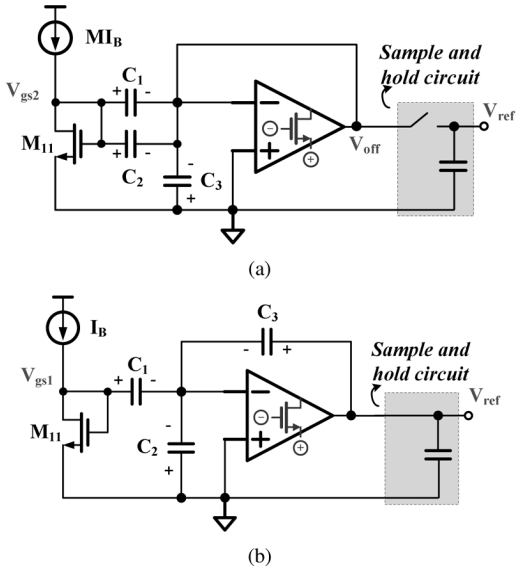

Fig. 4. Equivalent schematic of SCVR circuit. (a) When $\varphi_1 = 0$ and $\varphi_2 = 1$ (b) When $\varphi_1 = 1$ and $\varphi_2 = 0$.

supply voltage. Moreover, the core circuit utilizes transistors M_9 and M_{10} with different aspect ratios to generate different gate-source voltages of the N-type transistor M_{11} with the positive temperature coefficient characteristic. In addition, the SCVR circuit with auto-zeroing stores the offset voltage of the op-amp on capacitors C_1-C_3 in the first phase to reduce the effect from input offset voltage.

A. Nanoampere Biasing Current Circuit With PTAT^2 *Property*

Transistors M_{C1}-M_{C3} work as a startup circuit. The biasing circuit consists of four current paths to suppress the channel-length modulation effect. Because the biasing current circuit is composed by the positive close loop, the product of transconductances $(g_{m1} \times g_{m4} \times g_{m6} \times g_{m7})$ is designed to be smaller than the product of transconductances $(g_{m2} \times g_{m3} \times g_{m5} \times g_{m8})$. Transistors M_1 and M_3 are 5 V N-type transistors with a higher threshold voltage (~ 0.75 V) and operate in the subthreshold region. Transistors M_2 and M_4 are 3.3 V N-type transistors with a lower threshold voltage (~ 0.55 V) and operate in the saturation region in order to get a low PTAT^2 quiescent current. The drain current of an N-type transistor that operates in saturation and subthreshold region can be approximated by (5) and (6), respectively

$$I_{D(\mathrm{Sat})} = \frac{2}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2 \times (1+\lambda V_{DS}) \tag{5}$$

$$I_{D(\mathrm{Subthreshold})} = \mu_n V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS}-V_{th}}{mV_T}\right) \times \left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{6}$$

where m is the subthreshold swing parameter, V_T is the thermal voltage, and W_x and L_x are the width and length of transistor x, respectively. When the channel-length modulation effect is neglected, the bias current with positive temperature coefficient is

$$I_B = \frac{\mu_n C_{ox}\left(\frac{W_4}{L_4}\right)}{2(N-1)^2} m^2 V_T^2 \ln^2\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{W_1}}\right) \tag{7}$$

where $N = \sqrt{(W_4/L_4)(W_2/L_2)}$. According to (7), the biasing current has PTAT^2 characteristic. Furthermore, since the operating current in the subthreshold region is very small and no resistors are used in this design [8], a nanoampere of biasing current can be achieved. The current injects into the N-type transistor M_{11} in the core circuit. As a result, substituting (7) into (4) and the $\mu_n C_{ox}$ can be eliminated, the reference voltage V_{ref} is

$$V_{\mathrm{ref}} = \frac{C_2}{C_3}V_{th} + \left(\frac{C_1(\sqrt{M}-1)+C_2\sqrt{M}}{C_3(N-1)}\right) \times mV_T\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{11}}{L_{11}}}}\ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right). \tag{8}$$

Assume that the first-order negative temperature coefficient of threshold voltage V_{th} is α. The temperature coefficient of the thermal voltage V_T is PTAT. Thus, the temperature dependence of the reference voltage can be obtained by differentiating both sides of (8) with respect to temperature and is given by (9)

$$\frac{\partial V_{\mathrm{ref}}}{\partial T} = -\alpha\frac{C_2}{C_3} + \left(\frac{C_1(\sqrt{M}-1)+C_2\sqrt{M}}{C_3(N-1)}\right) \times \frac{mk_B}{q}\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{11}}{L_{11}}}}\ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right) \tag{9}$$

where k_B is the Boltzmann constant and q is the electron charge. By setting (9) equal to zero, the relation of capacitor C_1 and C_2 can be found as follows:

$$C_2 \times (\sqrt{M}\beta_p - \alpha) + C_1 \times (\sqrt{M}-1)\beta_p = 0$$

where

$$\beta_p = \frac{mk_B}{q(N-1)}\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{11}}{L_{11}}}}\ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right). \tag{10}$$

In general, the negative temperature coefficient α in our technology is about 0.82 mV/°C and the positive temperature coefficient β_p can be altered through the width and length of transistors and other coefficients. Hence, the sizes of capacitors C_1 and C_2 can be chosen to get a zero temperature coefficient at node V_{ref}.

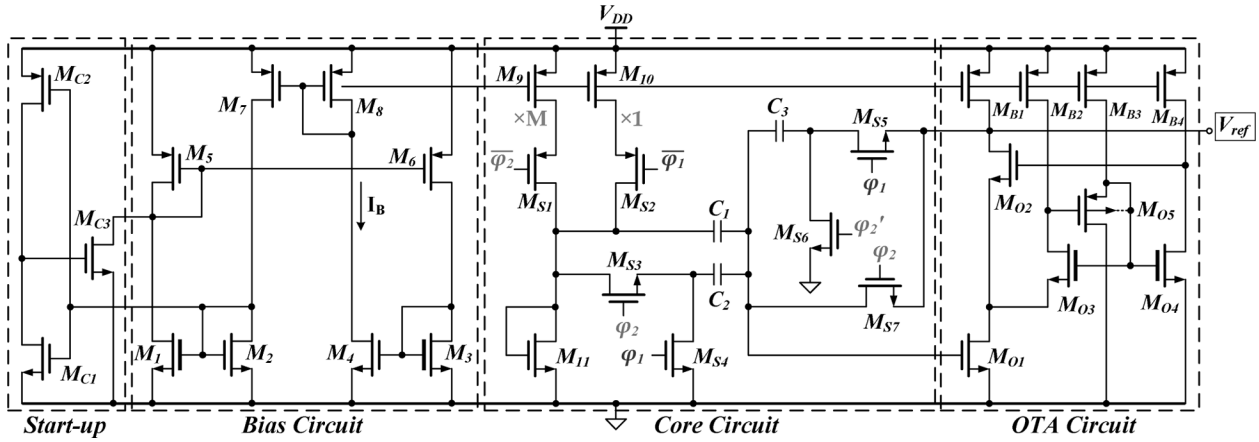

Fig. 5. Circuit of switched-capacitor voltage reference.

B. Proposed 1-V OTA Circuit and Auto-Zeroing

The proposed 1-V OTA circuit is composed of transistors M_{O1}-M_{O5} and M_{B1}-M_{B4} as depicted in Fig. 5. The input stage only uses an N-type transistor M_{O1} as common source amplifier to save power consumption. The feedback loop (M_{O3} and M_{O4}) increases the output impedance and boosts the gain of OTA circuit. In order to operate with low supply voltage, transistor M_{O5} biases the gate voltage of transistor M_{O3} so that it can still operate in the saturation region. Thus, transistors M_{O3} and M_{O4} are 5 V-N-type transistors with larger threshold voltage ($\sim$0.75 V) for operating in saturation region while transistor M_{O5} is in subthreshold region ($V_{SG(Mo5)} \leqq V_{th(Mo5)} \approx$ 0.7 V). That implies that the gate-source voltage of transistor M_{O5} is less than the threshold voltage of M_{O3} and the related derivation is

$$\begin{aligned} V_{DS(Mo3)} &= V_{GS(Mo3)} - V_{SG(Mo5)} \\ &> V_{GS(Mo3)} - V_{th(Mo3)}, \\ \text{when } V_{SG(Mo5)} &\leq V_{th(Mo5)} < V_{th(Mo3)}. \end{aligned} \tag{11}$$

When $V_{SG(Mo5)} \leqq V_{th(Mo5)} < V_{th(Mo3)}$. Thus, the minimum supply voltage of the OTA is given by $V_{DD(\min)} = V_{DS(Mo1)} + V_{GS(Mo3)} + V_{DS(MB3)} 0.1 + 0.8 + 0.1 \approx 1$ V. With the minimum supply voltage, transistor M_{O3} can still operate in the saturation region and the SCVR circuit can generate the desired reference voltage. Fig. 6 shows the Bode plot of the proposed OTA circuit from simulation when supply voltage V_{DD} varies from 1 to 4 V. The op-amp has largest gain of about 70 dB when V_{DD} varies from 2 to 4 V at room temperature and lowest gain when V_{DD} is 1 V owing to the suppression of the drain-source voltage of transistor M_{B1}. Also, the phase margin is always larger than 60°, ensuring the stability of this OTA circuit. However, because of asymmetries and process variation of this design, the influence of input offset voltage on the reference voltage [12] is greater than that from gain. As a result, the proposed SCVR circuit employs auto-zeroing shown through four timing conditions in Fig. 7(a)–(d) [10] to decrease the effect from input offset voltage. Fig. 7(a) and (d) show the equivalent schematics of SCVR circuit in phases $\varphi_1 = 1$ and $\varphi_2 = 1$, respectively. Moreover, Fig. 7(b) shows

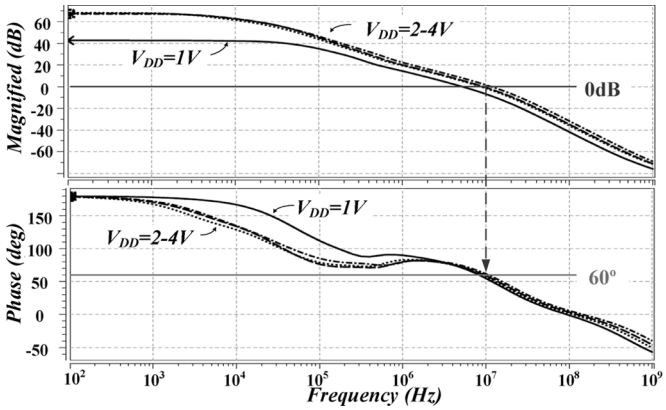

Fig. 6. Simulated Bode plot of proposed 1-V OTA as V_{DD} varies from 1 to 4 V at temperature = 25 °C.

that switch M_{S6} is turned off earlier than switch M_{S7} in Fig. 4 to avoid charge injection from the switch M_{S6} affecting the charge on the capacitors C_1-C_3. After switch M_{S6} is off, the gate-source voltage V_{GS2} is determined by the biasing current MI_B and the offset voltage is sampled and stored on the capacitor C_1-C_3. On the other hand, if the switch M_{S7} were turned off before M_{S6}, the voltages stored on the capacitors C_1-C_3 would be affected by the charge injection of the switch M_{S6}. Furthermore, the switch M_{S7} is off ahead of M_{S3} to reduce the input-dependence of charge injection effects from φ_2' to φ_1 in Fig. 7(c). According to the four timing sequences, the offset voltage can be precisely stored on the capacitors C_1-C_3 in the different phases. Considering the offset voltage, the charge of each capacitor is derived as (12)–(14)

$$\begin{aligned} \Delta Q_{C1} &= C_1(V_{GS2} - V_{\text{off}}) - C_1(V_{GS1} - V_{\text{off}}) \\ &= C_1(V_{GS2} - V_{GS1}) \end{aligned} \tag{12}$$

$$\Delta Q_{C2} = C_2(V_{GS2} - V_{\text{off}}) - C_2(-V_{\text{off}}) = C_2 V_{GS2} \tag{13}$$

$$\Delta Q_{C3} = C_3(-V_{\text{off}}) - C_3(V_{\text{ref}} - V_{\text{off}}) = -C_3 V_{\text{ref}}. \tag{14}$$

The difference charges $\Delta Q_{C1} - \Delta Q_{C3}$ are not affected when the offset voltage V_{off} is exactly stored on the capacitors from φ_2 to φ_1. Therefore, since the proposed SCVR circuit has auto-zeroing, the effect from offset voltage can be reduced to generate

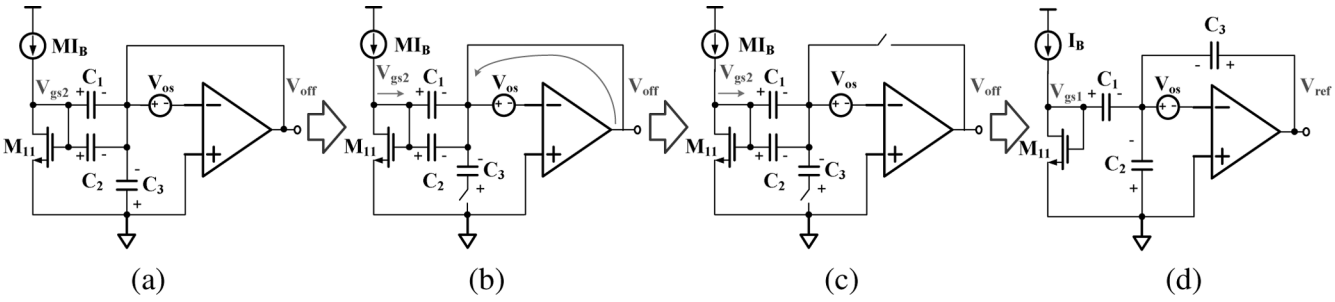

Fig. 7. Offset cancellation. (a) When $\varphi_1 = 0$ and $\varphi_2 = 1$. (b) The control signal φ_2'' is designed to open the switch earlier than φ_2 and φ_2' for avoiding the charge injection to store on the capacitors C_1-C_3. (c) The control signal φ_2' is designed to open the switch earlier than φ_2 for reducing the input-dependence the charge injection. (d) When $\varphi_1 = 1$ and $\varphi_2 = 0$.

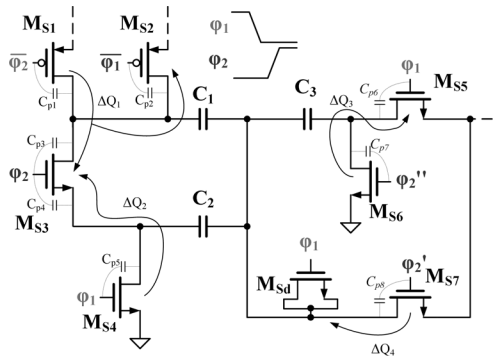

Fig. 8. Cancellation diagram of the clock feedthrough and charge injection.

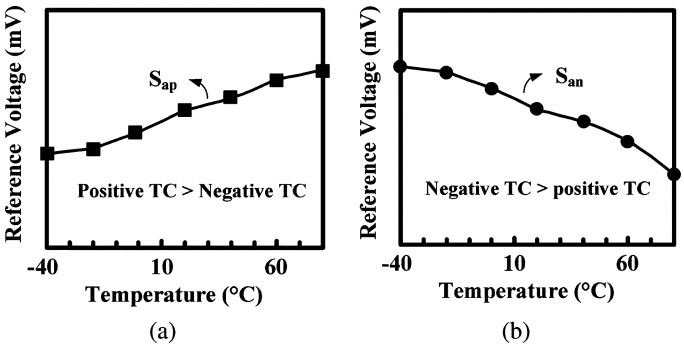

Fig. 9. (a) Positive TC of reference voltage. (b) Negative TC of reference voltage.

the accurate reference voltage in the second phase and thereby it is no longer critical to maintain the high dc gain of the OTA.

IV. Design Consideration

A. Channel Length Modulation Effect

The power supply variation of the proposed switched-capacitor CMOS voltage reference can be derived from (8). From Fig. 5, because transistors M_2, M_3, M_5, M_8, and M_{11} are diode-connected, almost all the variation of the supply voltage drops on the drain-source voltages of transistors M_1, M_4, M_6, M_7, M_9, and M_{10}. Therefore when the supply voltage varies, the biasing current I_B varies because of channel-length modulation [10]. To reduce this problem, the biasing circuit uses transistors with large channel lengths.

However, channel length modulation of M_1, M_4, M_7, M_9, and M_{10} still slightly affects the biasing current. Transistor M_1 operates in the subthreshold region. Since its drain-source voltage is larger than $4V_T$, the variation of the voltage $V_{DS(M1)}$ as shown in (6) can be neglected. Transistors M_4, M_7, M_9, and M_{10} operate in the saturation region. The channel length modulation of transistors M_7, M_9, and M_{10} are treated in the same way owing to the current mirror structure. Including channel length modulation, (8) is modified as follows:

$$V_{\text{ref}} = \frac{C_2}{C_3}V_{th10} + \frac{C_2\sqrt{M} + C_1(\sqrt{M}-1)}{C_3} \times \frac{mV_T \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right)\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{10}}{L_{10}}}\left[1+\lambda(V_{DD}-V_{GS2})\right]}}{N-\left[1+\lambda(V_{DD}-V_{GS8})\right]^{-1/2}}. \quad (15)$$

Differentiating the (15) with respect to supply voltage gives (16), shown at the bottom of the page. The value of $N = \sqrt{(W_4/L_4)(W_2/L_2)}$ is close to 1.3 in this design. Then, $\partial V_{\text{ref}}/V_{DD}$ has a small and negative value which is about -1.2

$$\frac{\partial V_{\text{ref}}}{\partial V_{DD}} = \beta_{VDD} \times \frac{\lambda\left\{N\sqrt{\left[1+\lambda(V_{DD}-V_{GS8})\right]} - \frac{\sqrt{\left[1+\lambda(V_{DD}-V_{GS2})\right]}}{2} - 1\right\}}{(N^2-1) + \left[\lambda(V_{DD}-V_{GS8})\right] + 2N\sqrt{\left[1+\lambda(V_{DD}-V_{GS8})\right]}}$$

$$\text{when } \beta_{VDD} = mV_T \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right)\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{10}}{L_{10}}}}\frac{C_2\sqrt{M} + C_1(\sqrt{M}-1)}{C_3} \quad (16)$$

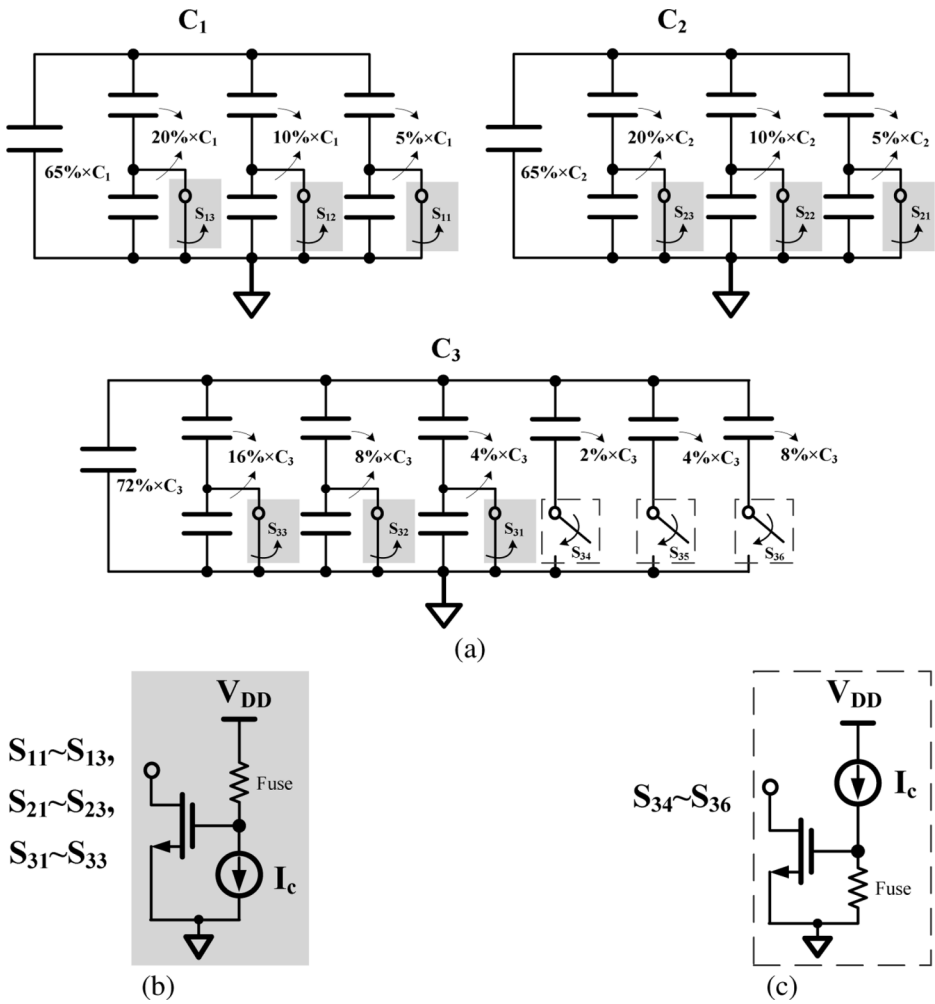

Fig. 10. (a) Implementation of trimming network for C_1, C_2, and C_3. (b) Implementation of switch $S_{11} \sim S_{13}$, $S_{21} \sim S_{23}$, and $S_{31} \sim S_{33}$. (c) The implementation of switch $S_{34} \sim S_{36}$.

mV/V. It implies that the reference voltage decreases with the rise of supply voltage and has small variation while the input voltage varies. In addition, differentiating the (15) with respect to temperature can get

$$\frac{\partial V_{\text{ref}}}{\partial T} = -\alpha\frac{C_2}{C_3} + \left(\frac{C_1(\sqrt{M}-1)+C_2\sqrt{M}}{C_3(N-1)}\right)\frac{mk_B}{q} \times \ln\left(\frac{\frac{W_3}{L_3}}{\frac{W_1}{L_1}}\right)\frac{\sqrt{\frac{\frac{W_4}{L_4}}{\frac{W_{10}}{L_{10}}}\left[1+\lambda(V_{DD}-V_{GS2})\right]}}{N-\left[1+\lambda(V_{DD}-V_{GS8})\right]^{-1/2}}. \quad (17)$$

According to (17), the positive coefficient will slowly increase while the supply voltage is increasing.

B. Clock Feedthrough and Charge Injection Effects

Generally speaking, the clock feedthrough and charge injection effects [12], [13] influence on the accuracy of the reference voltage. To reduce this problem, the simplest method is to design the switched transistors with small width at the sacrifice of the conduction ability. Therefore, the small widths of switched-transistors in the design are chosen to be enough for conducting nanoampere current. Unfortunately, the clock feedthrough and charge injection effects still have influence on the reference voltage about 3–5 mV after adopting this simplest method. To further reduce charge injection effects, it is important to carefully design the size of each switch. The detail of the switched parallel-plate capacitors is illustrated in Fig. 8 for explaining the minimization of the effect of the clock feedthrough and the charge injection when the clock φ_1 is from high to low and the clock φ_2 is from low to high. When the size of switch M_{S1} is designed equal to the sum of the sizes of switches M_{S2} and M_{S3}, the clock feedthrough from C_{p1} and can be cancelled by the clock feedthrough effects from C_{p2} and C_{p3}. In addition, the charge injection effect ΔQ_1 is also decreased. The clock feedthrough effect of the capacitance C_{p4} is cancelled by that of the capacitance C_{p5} if switches M_{S3} and M_{S4} have the same size. By choosing switches M_{S5} and M_{S6} to have the same size, the clock feedthrough effects from capacitances C_{p6} and C_{p7} are eliminated. However, the clock feedthrough effect of the capacitance C_{p8} really has a small ripple for the capacitors C_1, C_2, and C_3. Hence, transistor M_{sd} is used as a dummy switch to cancel this effect. The other charge injections ΔQ_2, ΔQ_3, and ΔQ_4, also can be decreased

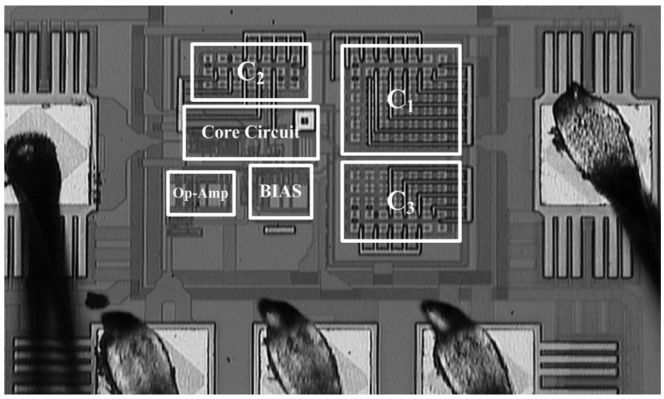

Fig. 11. Chip micrograph of the proposed SCVR circuit.

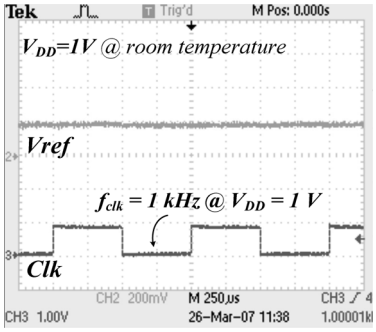

Fig. 12. Waveforms of the SCVR circuit.

by the switch arrangements as well. These methods alleviate the clock feedthrough and charge injection effects, and the accuracy of the reference voltage can be guaranteed.

C. Thermal and Flicker Noises

For some applications, the reference voltage circuits are needed to take account of noise performance because the values of the reference voltage are corrupted by thermal noise and flicker noise. The thermal noise and flicker noise from the OTA circuit is the most critical issue in this SCVR circuit. To dramatically reduce the thermal noise, transistor M_{o1} is designed to have the largest transconductance $g_{m(Mo1)}$ and the transistor M_{B1} is designed to have the smallest transconductance $g_{m(MB1)}$ since the thermal noise is proportional to $g_{m(MB1)}/g_{m(Mo1)}$. On the other hand, all the transistors in the OTA circuit have large width and length to effectively decrease the flicker noise since the flicker noise is inversely proportional to the product of width and length.

V. Trimming Flexibility

Owing to doping gradients, process variations, non-optimum layouts, and high stress areas of die, reference voltages with nonzero temperature coefficients are not accurate enough for sensitive analog circuits. Therefore, the values of the capacitors are adjusted to minimize the temperature coefficient of the reference voltage in this design. According to (9), if the temperature coefficient is not equal to zero, the temperature coefficient can be treated as a slope S_a, which is measured by the relationship

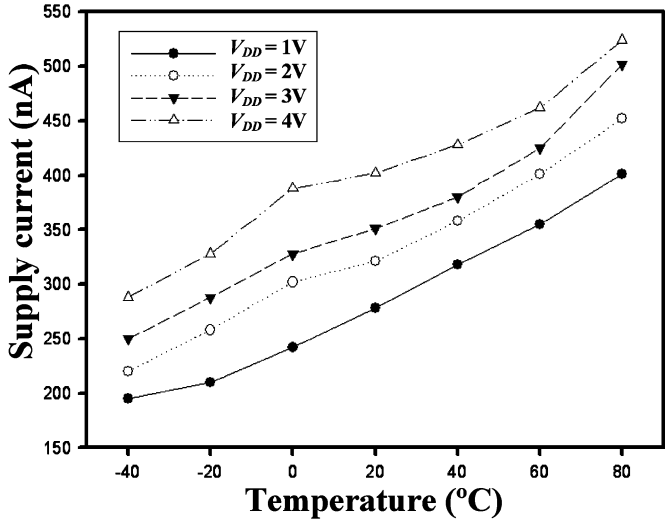

Fig. 13. Measured supply current versus the different supply voltage when temperature varies from $-40\,^{\circ}$C to $80\,^{\circ}$C.

TABLE I
Programmable Reference Voltage by 6 Bits Digital Code $S_{36} \sim S_{31}$

S_{36}	S_{35}	S_{34}	S_{33}	S_{32}	S_{31}	Reference Voltage (mV)
1	1	1	1	1	1	166.6
1	1	0	1	1	1	169.6
0	0	1	1	1	1	172.7
0	0	0	1	1	1	176
1	1	1	1	1	1	179.2
1	1	0	1	1	1	182.7
0	0	1	1	1	1	186.3
0	0	0	1	1	1	190.1
0	0	0	1	1	0	193.8
0	0	0	1	0	1	197.9
0	0	0	1	0	0	202.1
0	0	0	0	1	1	206.5
0	0	0	0	1	0	211
0	0	0	0	0	1	215.9
0	0	0	0	0	0	220.9

between the reference voltage and temperature. The slope S_a can be simplified from (10) and expressed as (18)

$$S_a = \frac{C_1}{C_3}(\sqrt{M}-1)\beta_p + \frac{C_2}{C_3}(\sqrt{M}\beta_p - \alpha). \tag{18}$$

Positive and negative temperature coefficients are eliminated by carefully adjusting the values of capacitors C_1 and C_2, respectively. In Fig. 9(a), if the measured temperature coefficient is positive, it means the value of positive coefficient is larger than that of negative temperature coefficient. The value of capacitor C_1 is decreased by the trimming procedure, and the decreased value ΔC_1 can be expressed as in (19). Similarly, decreasing the value of capacitor C_3 written as in (20) can reduce the negative temperature coefficient

$$\Delta C_1 = \frac{C_3 M_{ap}}{(\sqrt{M}-1)\beta_p} \tag{19}$$

$$\Delta C_2 = \frac{C_3 M_{an}}{(\sqrt{M}\beta_p - \alpha)}. \tag{20}$$

The trimming network for C_1 or C_2 uses three digital control bits to generate seven voltage levels for the trimming procedure

TABLE II
COMPARISON WITH OTHER VOLTAGE REFERENCES

	This work	Leung et al. [1]	G. Giustolisi et al. [3]	Leung et al. [4]	De Vita et al. [8]
Technology	0.35-μm CMOS	0.6-μm CMOS	1.2-μm CMOS	0.6-μm CMOS	0.35-μm CMOS
Supply Voltage (V)	1 to 4	0.98 to 1.5	1.2	1.4 to 3	0.9 to 4
Supply Current (μA)	0.25@1V 0.56@4V	< 18	3.6 @1.2V	< 9.7	0.04@0.9V 0.055@4V
Vref	190.1 mV	603 mV	295 mV	309.31mV	670 mV
TC (ppm/°C)	16.9	15	119±35.7	36.9	10
Line Sensitivity	0.76 %/V	0.73 %/V	NA	0.083 %/V	0.27 %/V
PSRR @100 Hz @10 MHz	V_{DD}=1 V -41 dB -17 dB	V_{DD}=0.98 V -44 dB -17 dB	V_{DD}=1.2 V -40 dB@5kHz	V_{DD}=1.4 V -47 dB -20 dB	V_{DD}=0.9 V -47 dB -40 dB
Die area (mm^2)	0.049	0.24	0.23	0.055	0.045
Trimming components	Capacitors	Resistors	Resistors	Resistors	N/A

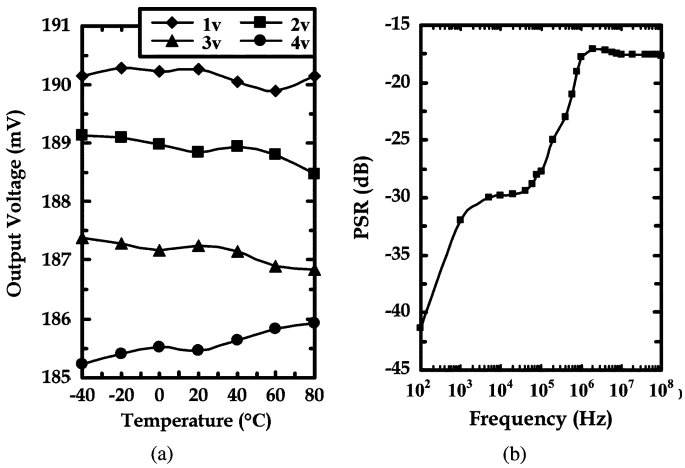

Fig. 14. Measurement results. (a) Output voltage versus temperature for different supply voltages. (b) PSRR at ($V_{DD} = 1$ V, $C_{\rm out} = 0$ °C and 25 °C).

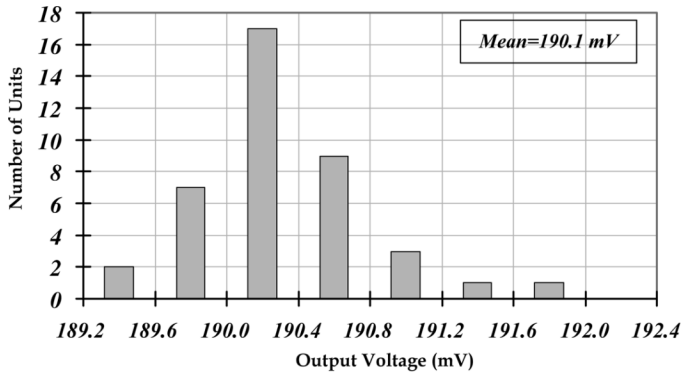

Fig. 15. Mean reference voltage from 40 tested samples.

as shown in Fig. 10. The resolution is about 2.5% and enough to accurately adjust the performance within 16.9 ppm/°C. Thus, the temperature coefficient can be reduced to near zero by trimming the values of capacitors C_1 and C_2 [14]. Similarly, a scalable voltage reference with 2% resolution can be achieved by adjusting the value of capacitor C_3 according to (8). Six digital control bits are used according to the requirement of increasing or decreasing the value of the reference voltage. The trimming implementation circuit also is shown in Fig. 10(a). The implementations of trimming switches are shown in Fig. 10(b) and (c). The advantages of the proposed SCVR circuit are that it uses capacitors with low temperature coefficient and the values of capacitors C_1-C_3 can be flexibly adjusted to achieve near zero temperature coefficient and scalable reference voltage value.

VI. EXPERIMENT RESULTS

The proposed SCVR circuit was implemented in TSMC double-poly quadruple-metal 0.35-μm CMOS technology. The values of capacitors C_1, C_2, and C_3 are set to about 1.5, 0.3, and 1 pF, respectively. The threshold voltages of N-type and P-type transistors are 0.55 and -0.65 V, respectively. The chip micrograph is shown in Fig. 11, and the active silicon area is 0.049 mm^2.

The measured waveforms are shown in Fig. 12 when clock frequency is equal to 1 kHz, the value of the output filter capacitor is about 20 pF, and the supply voltage V_{DD} is 1 V. The proposed voltage reference can not only operate at low supply voltage, but also has low power consumption and occupies a small area. At room temperature, the supply current is 250 nA at minimum supply voltage $V_{DD} = 1$ V and the supply current of bias circuit, core circuit, and OTA circuit are 90, 25, and 135 nA, respectively. When the supply voltage is at 4 V, the supply current is about 430 nA. The measured output voltage versus temperature for supply voltages over the range of 1 V to 4 V is shown in Fig. 13. Moreover, the measured temperature coefficient with $V_{DD} = 1$ V is 16.9 ppm/°C. Fig. 14(a) shows a plot of the measured reference voltage versus temperature over the range -40°C to 80 °C and the supply voltage varies from 1 to 4 V. The line regulation of reference voltage agrees with (13). The measured power-supply rejection ratio (PSRR) at minimum supply voltage (1 V) without any filtering capacitor is shown in Fig. 14(b). The PSRR is -41 dB at 100 Hz and -17 dB at 10

MHz. Furthermore, Fig. 15 shows the distribution of measured reference voltage as determined from 40 tested samples after the trimming procedure at room temperature and $V_{DD} = 1$ V. The mean value of the reference voltage is about 190.1 mV and reference voltage can be scalable from 166.6 to 220.9 mV by adjusting the value of capacitor C3. The measured programmable reference voltages are shown in Table I. Table II compares the proposed SCVR circuit with other reference voltage circuits. The results show that the power consumption and silicon area are smaller than those of published elsewhere [1], [3], [4], and [8]. Due to the trimming process, the SCVR circuit still can generate a reference voltage with a very low temperature coefficient even if the process has variations. Finally, it not only has lower sensitivity to variations in supply voltage and temperature, but also it can overcome process variations through the use of trimming.

VII. Conclusion

A switched-capacitor based CMOS voltage reference with nanoampere biasing current is proposed in this paper. The measured results show the temperature coefficient is 16.9 ppm/°C. An effective suppression of the temperature dependence of the carrier mobility and the channel-length modulation effect is achieved. Furthermore, the flexibility of trimming capacitors is an advantage of our proposed voltage reference for a precise CMOS reference voltage.

Acknowledgment

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