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子計畫五：低電壓差動信號傳輸接收器之設計與量測(3/3)

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計畫主持人：吳錦川

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計畫名稱：低電壓差動信號傳輸接收器之設計與量測(3/3)

執行單位：國立交通大學電子工程學系

計畫主持人：吳錦川 教授

編號：NSC92-2215-E009-035

1. Introduction

As the advancement of IC fabrication technology, the operation of processors has sped up. The amounts of data processed in each unit time become larger and larger as time goes by. The primary components of a data link are the transmitter, receiver, and cable [1]. In the first year, we had designed a CMOS serial link transmitter and receiver at a data rate of 480 Mb/s using LVDS (low voltage differential signal). In the second year, we had tried to increase the data rate to 1~1.2 Gb/s. In the last year of the research project, we had continued increasing the data rate at 2 Gb/s using RSDS by TSMC 0.35um 2P4M process with 3.3V supply. Three transmitters were designed; one were fabricated and measured. Two receivers were designed and simulated.

2. Transmitter

Fig.1 shows the block diagrams of the transmitter in this research. The transmitter consists of a PLL to produce the clock signals at 1 GHz frequency. There are two primary signal paths in the architecture of the transmitter. A 2-1 MUX and a CLK driver are used to deliver the clock information (TxC±) in the sampler path. Besides, the other path is compared with a PRBS circuit, a D-flip flop delay circuit, two 2-1 MUXs, a pre-emphasis circuit and a data driver.

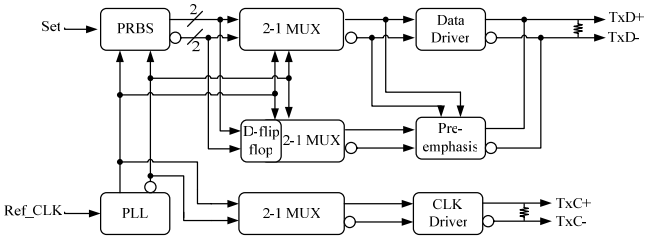

Fig. 1 Pre-emphasis transmitter block diagram

In order to achieve the goal of high speed and low power consumption, the two-stage ring oscillator architecture of the PLL is chosen [2][3]. However, a conventional differential delay cell fails to satisfy the oscillation conditions. If the conventional delay cell is used in a two-stage ring oscillator, the system will not oscillate because the gain is under 0dB at the frequency in which the absolute phase changes 90°(180°/N), causing the insufficient gain problem. Therefore, the circuit implementations of the proposed delay cells are shown in Fig. 2. The designed characteristics are obtained by means of the positive partial feedback.

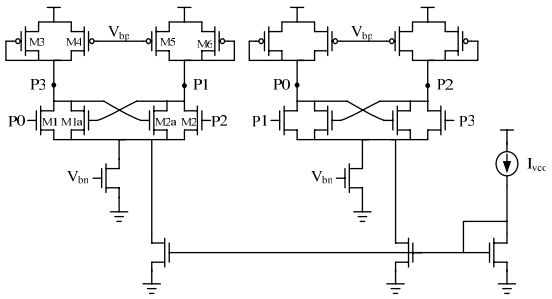

Fig. 2 Differential delay cells with partial positive feedback

With a 125 MHz reference frequency, the PLL can form a 1000MHz output with four uniformly distributed phases as clock signals for the multiplexer. Therefore we can achieve bit rates of 2 Gb/s.

The main issue of the data driver is the settling time control and it is also the bandwidth limitation of the driver. When the bit time of the data is smaller than the settling time of the data driver, the value of the previously transmitted signal will affect the current bit's waveform. The interference, called inter-symbol interference (ISI), reduces the maximum frequency at which the system can operate. Therefore, as shown in Fig. 3, a pre-emphasis driver is applied directly on the load resistance R_{T_T} to enhance the settling ability of the data driver.

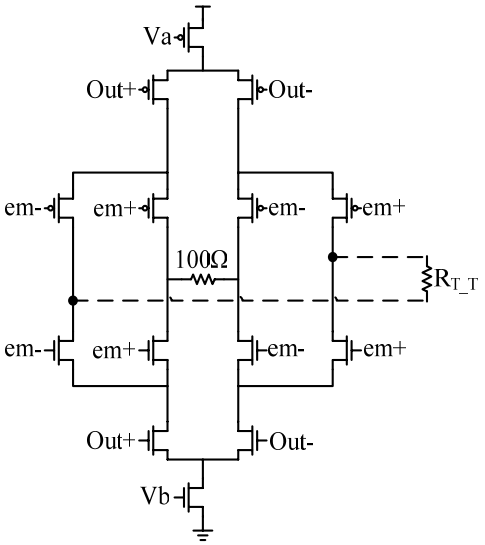

Fig. 3 Schematic of the pre-emphasis circuit

The Data Driver is designed with good driving ability and wide bandwidth to transmit data onto outside circuits. As shown in Fig. 4, the simplified RSDS transmitter outputs consist of a current source which drives the differential pair line. The implemented circuit uses the typical configurations with four MOS switches in bridge configuration to control the direction of current on the R_{T_T}. With M1 and M2 switched on, the polarity of the output current is positive together with the differential output voltage. On the contrary, the polarity of the output current and voltage is reversed if M1 and M2 are switched off. The differential load resistor R_T provides current-to-voltage conversion. In order to obtain the correct output offset voltage of the RSDS^{TM} Spec., a feedback loop across a replica of the transmitter circuit is used, but in this case the effect of component mismatches between the transmitters and replica should be carefully taken into account. [4]

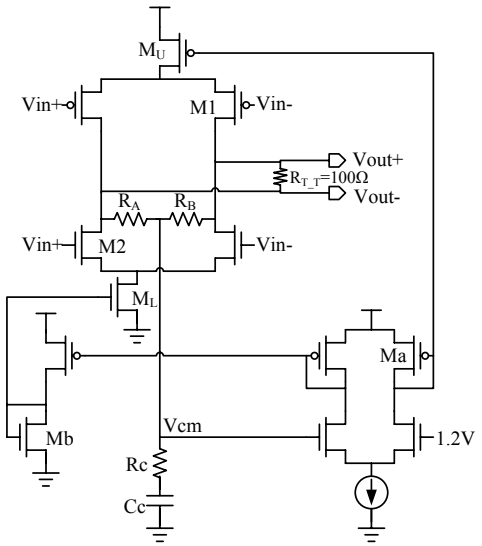

Fig. 4 Schematic of the transmitter driver and the closed-loop control circuit

The other kind architecture of the multiplexers used in transmitter architecture is shown as below:

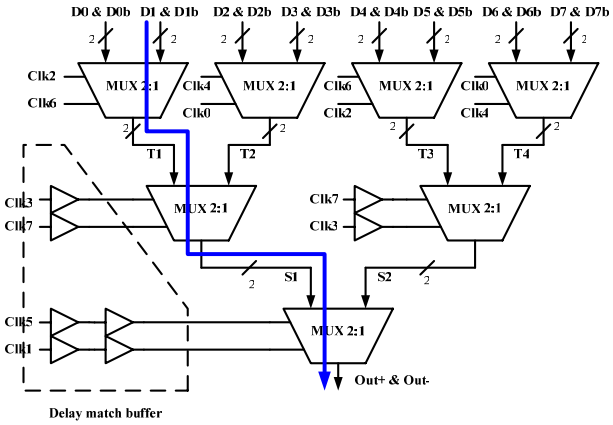

Fig. 5 Architecture of the 3-levels multiplexer [5]

In the issue of transmitter, there are a lot of types multiplexer to serialize the input parallel data. In the conventional MUX design, a multi-phase type MUX is usually used and shown as Fig 5. This circuit uses low frequency clock with different-phases, so the power consumption is low. But there is a fatal drawback that the fan-in at the point A and B is high while there are many multiplexer inputs. The high fan-in causes the large parasitic capacitance and the large parasitic capacitance will limit the maximum operating speed. The speed limitation is not only an inherent property of the process technology but also of the circuit topology. Therefore a proposed circuit, 3-levels MUX is introduced in this section to overcome the speed limitation problem.

Fig. 5 shows the architecture of the 3-levels 8 to 1 MUX which is built with seven 2 to 1 MUX and some delay match butters. The 2:1 MUX cell is shown in Fig. 6 and the output capacitance is small, so it can operate at higher speed. The 3-levels MUX is more suitable for high-speed operations with low power consumption than the conventional one. However, the delay match buffer is needed that the clock timing can match the data timing while the data passed through a MUX with a certain delay. The delay match buffer is shown in Fig 7 and the construction is the same to 2:1 MUX, so the circuit delay of these two circuits is almost the same.

This circuit, however, has some flaws. First, it converts serial data only into 2 bit parallel, which makes it unsuitable for some communication system such as 10-channel MUX needed in fiber channel designs. Second, it requires the distribution of precisely delay adjust for different phase clock signals to its respective 2:1 MUX.

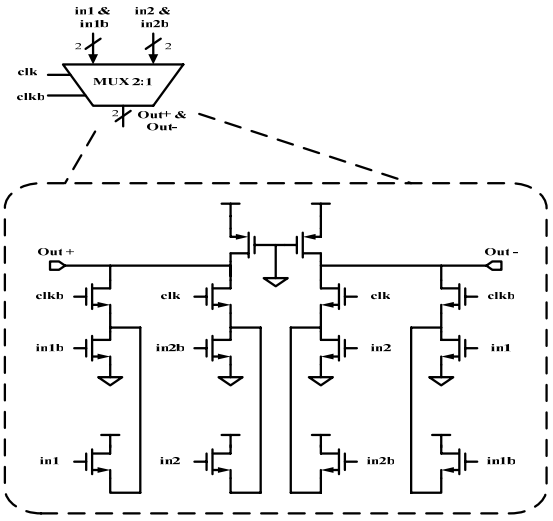

Fig. 6 Scheme of 2:1MUX Cell

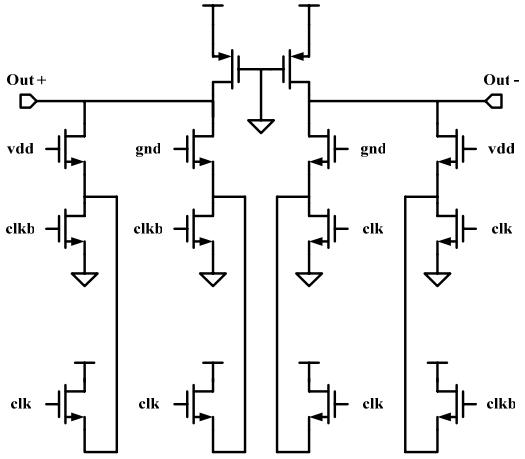

Fig. 7 Delay Match Buffer

3. Receiver

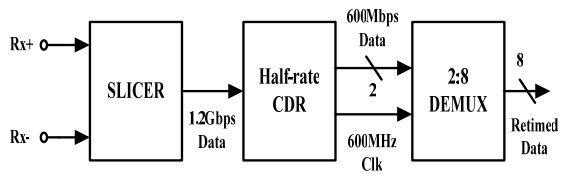

Figure 8 Block diagram of the receiver

Fig. 8 shows the architecture of the receiver design and the principle of the clock and data recovering circuit. The differential transmitted data signal is amplified to digital signals by the slicer circuit. The purpose of the clock and data recovery circuit is to generate the receiver sampling clock based on the input data and adjust the sampling point on the center of the data eye. Then the de-multiplexer circuit makes the input serial data restoring to the eight-phase parallel data.

Fig. 9 shows the CDR architecture used in this thesis, this is a half-rate dual-tracking loop design with improved jitter performance. Due to the temperature and process variations, the frequency drift in VCO exists. There are two circuits, FD (frequency detector) and PD (phase detector) to adjust the output frequency in VCO. The frequency detector detects the frequency difference to drive the charge pump to adjust the control voltage and then VCO frequency can be close to half of the data rate. Then, the half-rate phase detector produces error signal proportional to the phase difference between the 600 MHz VCO clock and 1.2Gbps data stream. Moreover, when the half-rate phase detector executes the adjusting operation, it generates the two 600Mbps data sequence for the de-multiplexer. This will be discussed in the following section.

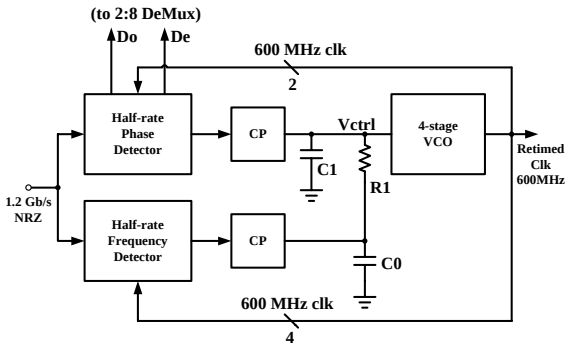

Fig. 9 Half-rate CDR architecture

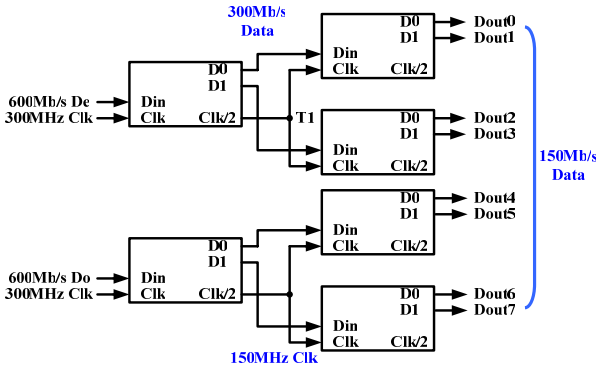

Fig. 10 Asynchronous tree-type 2:8 de-multiplexer

The architecture of 2:8 de-multiplexer is shown in the Fig 10[6]. The asynchronous tree-type de-multiplexer architecture can use both rising and falling clock edges to operate. Therefore, a tree-type de-multiplexer is able to operate at half the speed of the data rate. It is more suitable for high-speed work because of its simple construction and low power consumption.

Finally, with the sampling clock traced from the input data stream and the de-multiplexer. The input serial data can be recovered back to the original 8-paraelle data.

4. Experimental Result

The transmitter is implemented in tsmc 0.35um 2P4M CMOS process. Fig. 11 is the chip photo of transmitter.

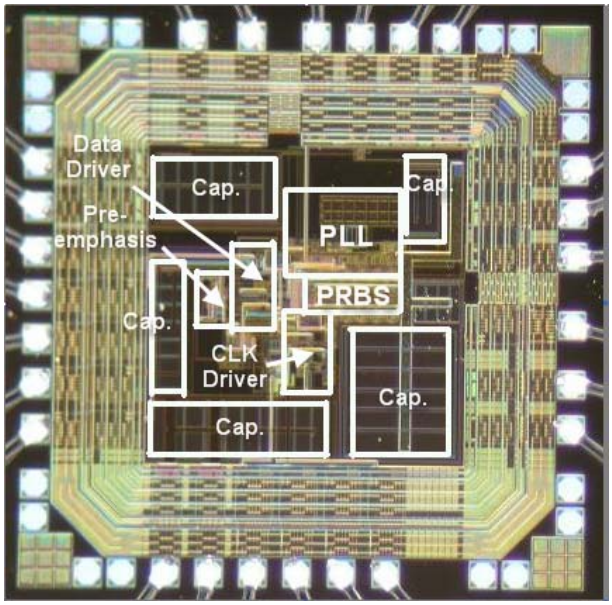

Fig. 11 Chip photo of the Transmitter.

In Fig. 12, the differential output of the transmitter clock driver at 533 MHz is shown. Meanwhile, Fig. 13 shows the eye diagram of the transmitter data driver differential output at 1066 Mbps.

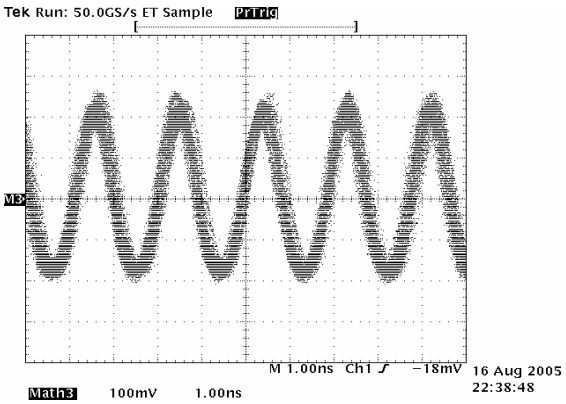

Fig. 12 the differential output of the transmitter clock driver at 533 MHz

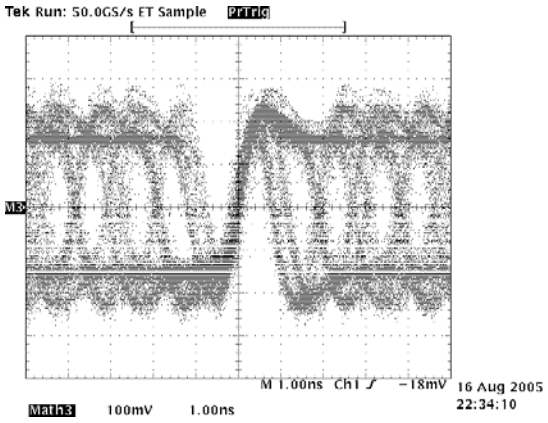

Fig. 13 the eye diagram of the transmitter data driver differential output at 1066 Mbps

In Fig. 14 and 15, the transmitter operates at high frequency. The clock rate is 727 MHz and the data rate is 1454 Mbps.

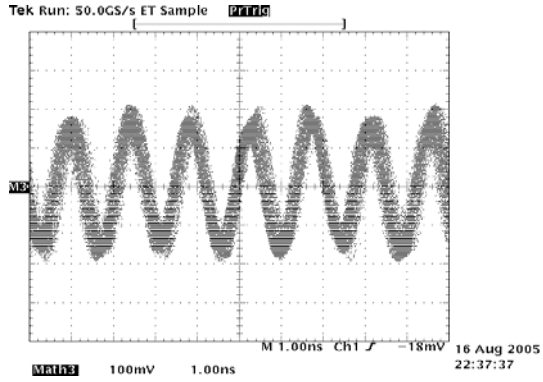

Fig. 14 the differential output of the transmitter clock driver at 727 MHz

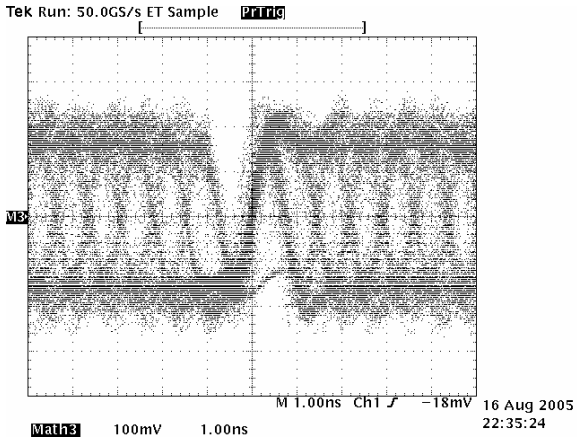

Fig. 15 the eye diagram of the transmitter data driver differential output at 1454 Mbps

The locked frequency of the PLL cannot be any higher in the normal design setup. Fig. 16 and Fig.17 show the experimental results of clock and data when the power supply voltage is turned to 4V.

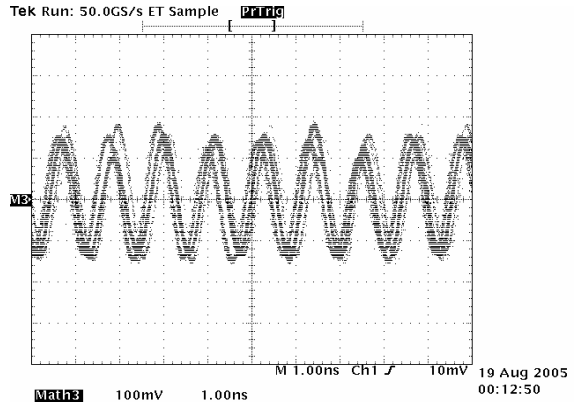

Fig. 16 the differential output of the transmitter clock driver at 930 MHz when vdd = 4V

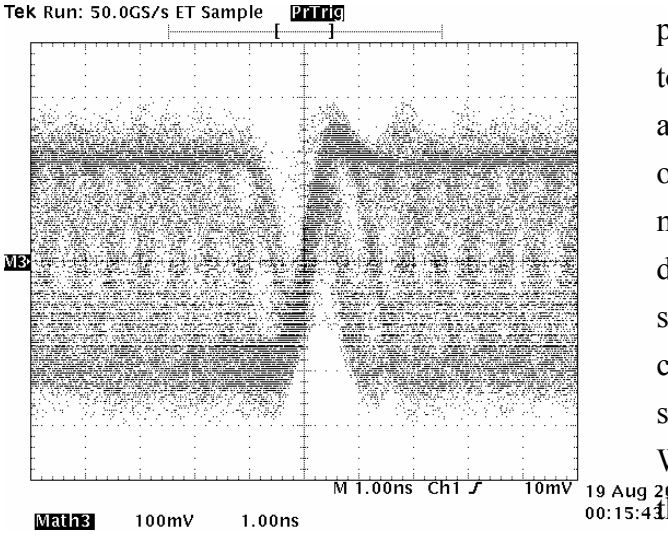

Fig. 17 the eye diagram of the transmitter data driver differential output at 1860 Mbps when vdd = 4V

5. Conclusion

To transmit high speed signals and achieve lower power consumption, a transmitter circuit with the RSDS^{TM} interface has been designed in this thesis. The chip is fabricated in a TSMC 0.35μm 2P4M CMOS process. The research results can be summarized as follows.

The transmitter is composed of a four-phase PLL, PRBS circuits, 2-1 multiplexers, an output clock driver and an output data driver with a pre-emphasis circuit. The input reference frequency of the four-phase PLL is 125MHz; it outputs four uniformly distributed clocks with 1 GHz frequency. The PLL comprises a Phase/Frequency Detector, a Charge Pump, a Loop Filter, a two-stage differential Voltage Control Oscillator and a divided-by-eight divider. The main issue of the PLL is to generate the required clock signals to the transmitter with timing jitter as small as possible. This may be down from system level to circuit level, including parameters design and layout considerations. Thus, the PLL outputs complementary clock signals to the multiplexers to convert parallel data to serial data. Finally, the output data driver drives the serial data onto the bus. Besides, the output clock driver drives the complementary clock signals onto another bus synchronously.

We have devoted to design a transmitter with the data rate at 2Gbps but the operation of the implemented chip can only achieve 1.4Gbps at most.

REFERENCES

1. W. J. Dally, and et al. “Transmitter Equalization for 4-Gbps Signaling,” *IEEE Micro.*, pp. 48-56, 1997.
2. Bautista, D.P.; Aranda, M.L.; “A low power and high speed CMOS Voltage

Controlled Ring Oscillator,” Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on 23-26 May. 2004, Volume 4, Page(s): IV - 752-5.

3. Yan, W.S.T.; Luong, H.C.; “A 900-MHz CMOS low-phase-noise voltage controlled ring oscillator,” Analog and Digital Signal Processing, IEEE Transactions on Circuits and Systems II, Volume 48, Issue 2, Page(s): 216 – 221, Feb. 2001.
4. Andrea Boni; Andrea Pierazzi; Davide Vecchi; “LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35- μm CMOS,” IEEE Journal of Solid-State Circuits, vol. 36, no. 4, pp. 706-711, April 2001.
5. Hung-Wen Lu and Chau-Chin Su, “A 5Gbps CMOS LVDS Transmitter with Multi-Phase Tree-Type Multiplexer” 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, Aug. 2004
6. M. Fukaishi, et al., “A 4.25-Gb/s CMOS fiber channel transceiver with asynchronous tree-type demultiplexer and frequency conversion architecture,” IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 2139-2147, Dec. 1998.