行政院國家科學委員會專題研究計畫　成果報告

具有形變通道之互補式金氧半元件製作與分析

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計畫主持人：黃調元

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□期中進度報告

具有形變通道之互補式金氧半元件製作與分析

Fabrication and characterization of CMOS devices with strained channel

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執行單位：國立交通大學電子工程研究所

中 華 民 國 年 月 日

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"Fabrication and characterization of CMOS devices with strained channel"

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中文摘要

在本報告中，我們主要探討單軸形變通道之奈米級互補式金氧半元件之通道背向散射特性分析。通道背向散射比在單軸伸張應力下或單軸壓縮應力下分別將增加或減少。我們發現，在次 100 奈米級元件中，背向散射載子平均自由路徑之形變造成的調變及 k_BT 層厚度的減少是造成具有不同背向散射比的原因。此外，不管形變極性如何，源極端注入速度將改善。我們也將藉由彈道效率及注入速度分析通道背向散射比對於驅動電流的影響。

關鍵字：金氧半元件、散射、單軸形變。

Abstracts

In this work, we have investigated the channel backscattering characteristics of uniaxially strained nanoscale CMOSFETs. Channel backscattering ratio increases and decreases under uniaxial tensile and compressive strain, respectively. It is found that in sub-100 nm devices, strain-induced modulation of carrier mean-free-path for backscattering and reduction in k_BT layer thickness are responsible for the different behaviors of backscattering ratio. Nevertheless, the source-side injection velocity improves irrespective of the strain polarities. The impact of channel backscattering ratio on drive current is also analyzed in terms of ballistic efficiency and injection velocity.

Keywords: MOSFETs、scattering、uniaxial strain.

Introduction

Recently various strain techniques are actively pursued to give the device performance a much needed boost in 90 nm node and beyond [1]–[3]. Mobility enhancement induced by strain in the channel has been widely characterized, however, only half of the mobility enhancement is all that needed to account for the observed saturation drain current increase [4]. To reconcile with this discrepancy and to understand ballistic transportation in nanoscale transistor, carrier backscattering theory has been proposed. As illustrated in the inset of Fig. 1, some of the injected carriers are backscattered near the source end of channel region within a k_BT layer which has a potential drop of k_BT / q and thickness of l_0. Since the transmitted carriers ultimately determine the drive current, carrier backscattering ratio r and injection velocity υ_{inj} at the top of source-channel barrier are both critical in determining the drive current I_{dsat}. For higher I_{dsat}, reducing r and increasing υ_{inj} are desirable [5]. It has been reported that biaxial tensile strain results in backscattering ratio reduction with $Si_{0.7}Ge_{0.3}$ virtual substrate from

simulation [6]. However, the influence of uniaxial strain on backscattering ratio has not been clarified yet. In this paper, we report the impact of uniaxial process-induced tensile and compressive strains on channel backscattering ratio for the first time. In addition, the impact of channel backscattering ratio on drive current is also analyzed in terms of mean-free-path (MFP), k_BT layer thickness, ballistic efficiency, and injection velocity.

Experimental

Process-strained Si (PSS) MOSFETs fabricated by state-of-the-art CMOS process are studied in this work [2]. Schematic structure with uniaxial strain engineering is illustrated in Fig. 1, where uniaxial tensile strain for nMOSFETs and uniaxial compressive strain for pMOSFETs are achieved. To minimize barrier height modulation from drain-induced barrier lowering (DIBL), PSS and control devices with nominally identical DIBL and subthreshold swing are characterized (inset of Fig. 2). Drive current improvement of both PSS devices relative to control devices is shown in Fig. 2, all devices with identical inversion *C*-*V* characteristics. From scattering theory in [6], drive current in saturation region ($|V_d|$= 1 V) can be expressed as

$$I_{dsat} = W\upsilon_{inj}\left[\frac{1-r_{sat}}{1+r_{sat}}\right]C_{\mathrm{OX}}\left(V_g - V_{T,sat}\right) \qquad (1)$$

where υ_{inj}, r_{sat}, and $V_{T,sat}$ represent injection velocity, backscattering ratio, and threshold voltage, respectively. The ratio r_{sat} is a function of carrier mean-free-path for backscattering λ_0 and k_BT layer thickness l_0 (r_{sat}= 1 / [1 + λ_0/ l_0]) [8]. The $V_{T,sat}$ is determined by maximum transconductance ($G_{m,max}$) method with DIBL consideration (ΔV_{DIBL}= $V_{T,lin}$@$|V_d|$=10 mV – $V_{T,sat}$@$|V_d|$=1 V, where V_T is defined as the gate voltage when $|I_d|$= 0.1W/L μA), i.e., $V_{T,sat}$= $V_{T,lin}$($G_{m,max}$@$|V_d|$=10 mV) – ΔV_{DIBL}. Then, a temperature-dependent analytical model is employed to extract the λ_0 / l_0 ratio using the following analytic expression

$$\alpha = \frac{1}{T}\left[\frac{1}{2} - \frac{4}{2+\lambda_0/l_0}\right] - \frac{\eta}{V_g - V_{T,sat}} \qquad (2)$$

where α and η represent temperature sensitivity of I_{dsat} and $V_{T,sat}$, i.e., α= ($I_{dsat1} - I_{dsat2}$) / ($T_1 - T_2$) and η= ($V_{T,sat1} - V_{T,sat2}$) / ($T_1 - T_2$) [8]. The measurement temperature is decreased from 298 K to 228 K at a step of 15 K. α and η are extracted from the best-fitted slopes of ΔI_{dsat} and $\Delta V_{T,sat}$ at different temperatures. The λ_0 / l_0 ratio can then be calculated by (2). Lastly, backscattering ratio and ballistic efficiency *B* (= [1 – r_{sat}] / [1 + r_{sat}]) can be deduced.

Results and Discussion

The gate length dependence of backscattering factors, $|\alpha|$, λ_0 / l_0, r_{sat}, and *B* are shown in Figs. 3 and 4. In Fig. 3, $|\alpha|$ is the dominant factor in determining λ_0 / l_0 of MOSFETs since the ratio η / (V_g – $V_{T,sat}$) ($|\eta|$= 0.5 to 0.9 mV/K) is ten times smaller than $|\alpha|$. Compared with control devices, PSS nMOSFET demonstrates slight increase in λ_0 / l_0, while PSS pMOSFET shows significant decrease. Comparing to r_{sat} of control devices, the tensile-strained PSS nMOSFET has smaller r_{sat} whereas compressive-strained PSS pMOSFET has larger $r_{sat.}$ This phenomenon indicates that injected electrons in tensile-strained nMOSFET exhibit less channel backscattering while

injected holes in compressive-strained pMOSFET suffer more backscattering. The r_{sat} difference between control and PSS devices becomes more dramatic as $L_{physical}$ is shorter than 0.1 μm. It is also shown that the ballistic efficiency of tensile-strained PSS nMOSFET is improved but that of compressive-strained PSS pMOSFET is degraded. Q_{inv} for characterized devices is extracted from MOSFETs with an area of 100 μm^2 under strong inversion, taking into account V_T roll-off and DIBL [9]. υ_{inj} can then be calculated by $I_{dsat}= W\upsilon_{inj}BQ_{inv}$. As shown in Fig. 5, the injection velocity is improved in both PSS devices, which is ascribed to process-strained induced reduction in carrier effective mass [1]. As shown in the inset of Fig. 5, ΔI_{dsat} can be related to the sum of $\Delta\upsilon_{inj}$ and ΔB. Slight underestimation of ΔI_{dsat} in NMOS is due to minor Q_{inv} difference between PSS and control devices. To further investigate the mechanism of strain-induced backscattering modulation, λ_0 is deduced from the expression $\lambda_0= (2\, k_B T / q)\, \mu_0 / \upsilon_{inj}$ [4], where the low field mobility μ_0 is extracted by the resistance slope-based method [10]. From the ratio of λ_0 / l_0, l_0 can be calculated. It is found that l_0 of both PSS devices is reduced to about 90% of that of control devices, and the thinning of l_0 may be due to the strain-induced bandgap shift causing sharper potential profile. In addition, λ_0 is increased in PSS nMOSFETs, which is consistent with the simulation results of [11]. Contrary to nMOSFETs, PSS pMOSFETs exhibit smaller λ_0 than that of control devices, which is probably due to the compressed lattice in the channel inducing much severe carrier scattering. Hence, it is essential to improve not only injection velocity but also ballistic efficiency in order to further enhance the performance of uniaxial-strained MOSFETs in nanoscale regime. Although I_{dsat} of PSS pMOSFETs is improved through the enhancement of injection velocity at the expense of ballistic efficiency loss, ultimate PSS performance boost should therefore be expected if one could conceive a clever method to enhance ballistic efficiency without sacrificing injection velocity.

Conclusions

In this letter, the influence of uniaxial strain on channel backscattering ratio in nanoscale MOSFETs is investigated. Channel backscattering ratio is reduced in tensile-strained nMOSFET but increased in compressive-strained pMOSFET, notwithstanding the increased carrier injection velocity in both cases. Drive current is determined not only by backscattering ratio but also injection velocity. Strain techniques or device structures with simultaneous improvement of channel backscattering ratio and injection velocity are therefore favorable for ultimate performance boost in mesoscopic regime.

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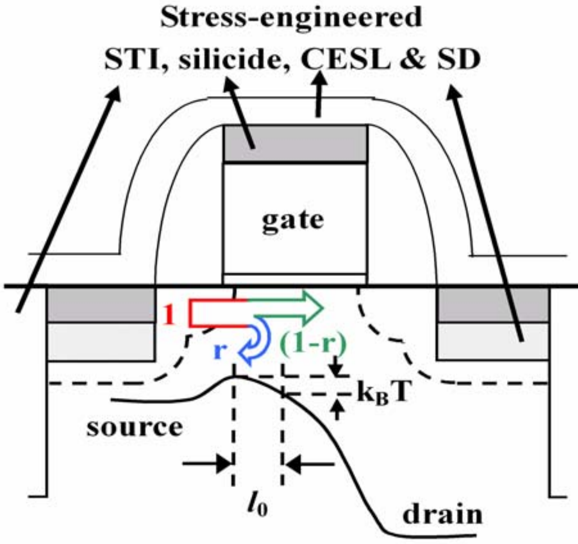

Fig.1. Schematic structure of process-strained Si (PSS) MOSFETs. Various stress -engineered processes are employed to achieve uniaxially tensile and compressive strains for nMOSFETs and pMOSFETs, respectively. The inset illustrates that carrier in k_BT layer region is with a backscattering ratio r where the thickness of k_BT layer is l_0.

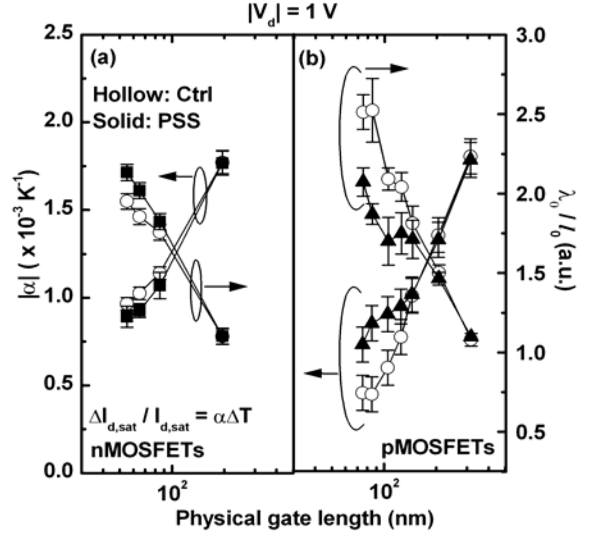

Fig.3 Comparison of temperature sensitivity of drive current $|\alpha|$, and ratio of mean-free-path (MFP) for backscattering over k_BT layer thickness λ_0 / l_0 between control devices, and PSS (a) nMOSFETs, (b) pMOSFETs.

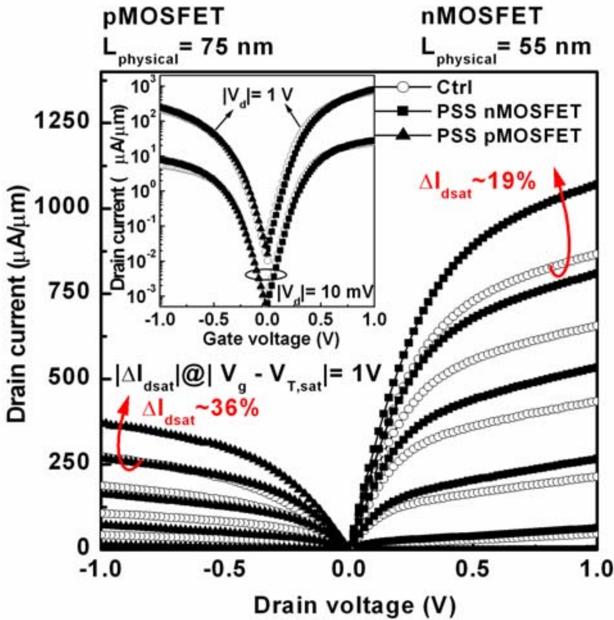

Fig.2. I_d-V_d characteristics of control and PSS MOSFETs. With identical subthreshold swing and DIBL to those of control devices (as shown in the inset), both PSS nMOSFET and pMOSFET exhibit about 19% and 36% improvement of drive current at $|V_g - V_{T,sat}|= |V_d|= 1$ V.

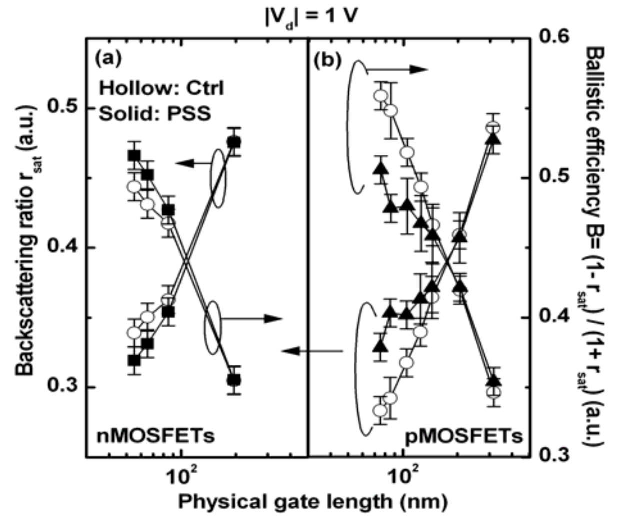

Fig. 4 Effects of uniaxial (a) tensile-strained nMOSFETs, and (b) compressive-strained pMOSFETs on channel backscattering ratio r_{sat} and ballistic efficiency B.

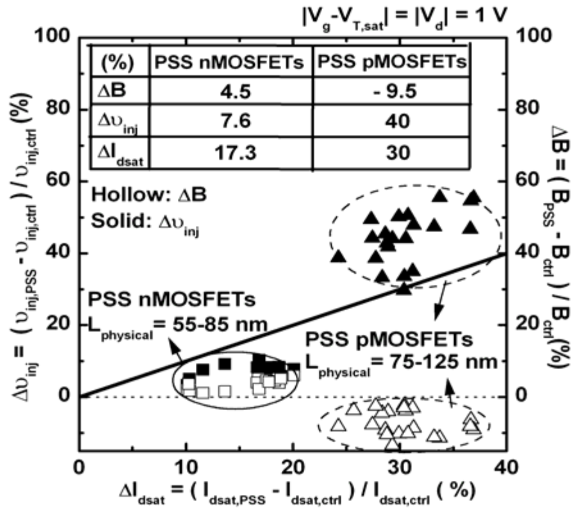

Fig. 5 $\Delta\upsilon_{\mathrm{inj}}$ and ΔB as a function of ΔI_{dsat} for PSS nMOSFETs (square symbol) and pMOSFETs (triangle symbol). The solid line indicates that $\Delta\upsilon_{\mathrm{inj}}$ (or ΔB) varies linearly with ΔI_{dsat}. For PSS nMOSFETs, both carrier injection velocity and ballistic efficiency are higher than control devices. While for PSS pMOSFETs, slightly lower B and much higher υ_{inj} are obtained. The inset shows the variation percentage of parameters of PSS devices (nMOSFETs, L_{physical}= 55 nm, pMOSFETs, L_{physical}= 75 nm) relative to those of control devices. ΔI_{dsat} can be related to the sum of $\Delta\upsilon_{\mathrm{inj}}$ and ΔB.