

Au/Ge/Pd Ohmic Contacts to n-GaAs with the Mo/Ti Diffusion Barrier

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The influences of the As-outdiffusion and Au-indiffusion on the performances of the Au/Ge/Pd/n-GaAs ohmic metallization systems are clarified by investigating three different types of barrier metal structures Au/Ge/Pd/GaAs, Au/Ti/Ge/Pd/GaAs, and Au/Mo/Ti/Ge/Pd/GaAs. The results indicate that As-outdiffusion leads to higher specific contact resistivity, whereas Au-indiffusion contributes to the turnaround of the contact resistivity at even higher annealing temperature. For Au/Mo/Ti/Ge/Pd/n-GaAs samples, they exhibit the smoothest surface and the lowest specific contact resistivity with the widest available annealing temperature range. Moreover, Auger electron spectroscopy depth profiles show that the existing Ti oxide for the Mo/Ti bilayer can very effectively retard Au-indiffusion, reflecting the onset of the turnaround point at much higher annealing temperature.

Key words: Au/Mo/Ti/Ge/Pd metallization, n-type GaAs, ohmic contact

INTRODUCTION

Ohmic contacts to n-type GaAs using the technologies of forming an interfacial with high Ge-doping concentrations have been widely investigated. The most commonly used metallization system is Au-Ge-Ni which was first proposed by Braslau and his coworkers.¹ This metallization system often resulted in structural nonuniformity due to nonplanar interface morphology and substantial lateral encroachment. These disadvantages made it unsuitable for devices with crucial dimensional requirements.

Recently, a more popular metallization system using nonalloyed Ge/Pd to GaAs was pioneered by Marshall et al.²⁻⁴ It was reported to possess many attractive features, including good surface morphology, planar, and shallow interfacial layer due to its limited solid phase reactions. These advantages have been demonstrated in device applications such as

CHINT/NERFET,⁵ metal semiconductor field effect transistors (MESFETs),⁶ and heterojunction bipolar transistors (HBTs).

When used in device applications, an overlayer on Pd/Ge is usually required for bonding and chemical protections. A gold-based overlayer system has the advantages of very low resistivities, but its fast diffusivity easily degrades the regrown interfacial layer and the surface morphology significantly. In order to overcome this problem, a metallic interlayer between Au and Pd/Ge as a diffusion barrier is required. The insertion of diffusion barrier might also benefit the ohmic characteristics by reducing the As-outdiffusion. Paccagnella et al.⁶ have investigated WN, Ti/Pd, Ti/Pt, and Ni as the diffusion barrier for the source/drain ohmic contacts in their MESFETs. They found that WN and Ti/Pt were the better candidates. More recently, Huang et al.⁷ compared both Cr and TiW and concluded that the TiW should be the preferred barrier metal. However, both WN and TiW are not easily deposited using electron beam evapora-

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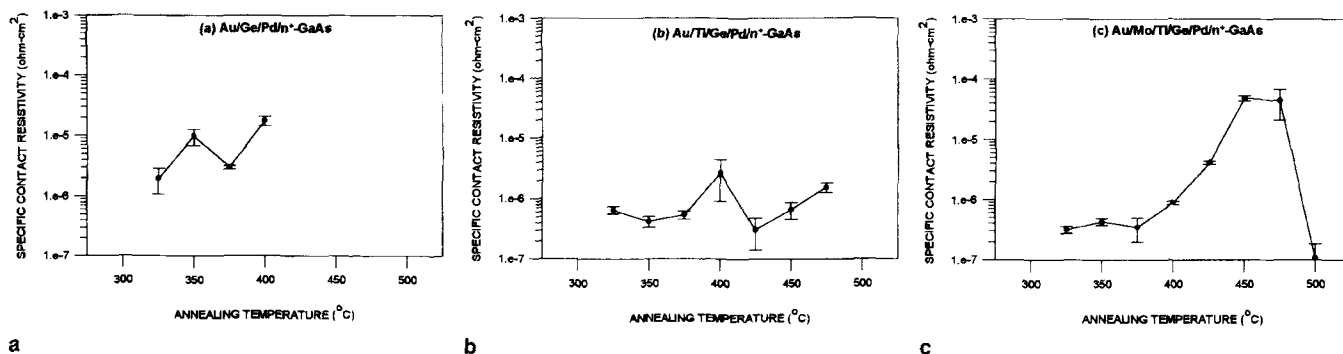


Fig. 1. The TLM-derived specific contact resistivities measured at room temperature as a function of annealing temperature for the samples of (a) Au/Ge/Pd/n-GaAs, (b) Au/Ti/Ge/Pd/n-GaAs, and (c) Au/Mo/Ti/Ge/Pd/n-GaAs.

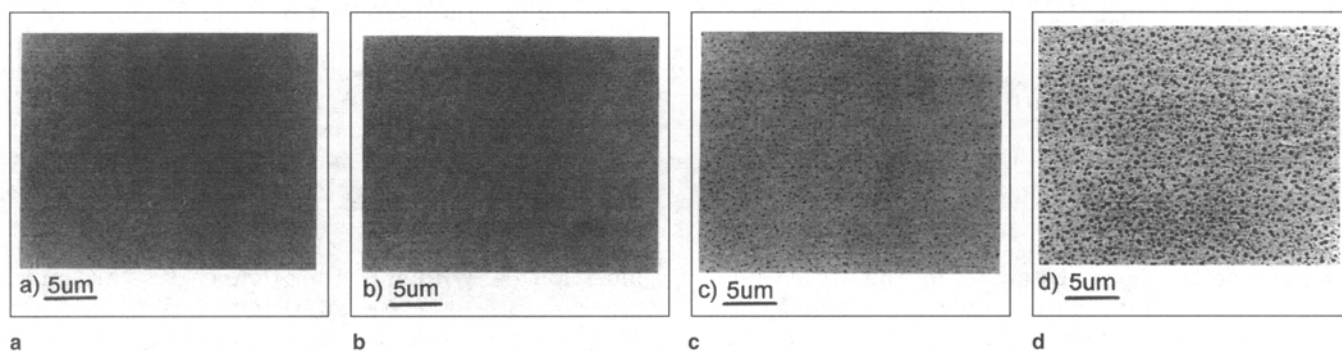


Fig. 2. Surface morphology of the samples deposited with the Au/Ge/Pd metallizations rapid thermal annealed for 60 s at different annealing temperatures. (a) 325, (b) 350, (c) 375, and (d) 400°C.

tor, and therefore, a more complex metal deposition system is needed.

In this paper, the Ti-Mo-Au metal system which had been studied and proven to be a very efficient diffusion barrier in silicon device process⁸ is therefore adopted to prevent As-outdiffusion and Au-indiffusion during thermal annealing for ohmic formation of Au/Ge/Pd/GaAs contact metallization systems. In this work, a specific contact resistivity as low as $2 \times 10^{-7} \Omega\text{-cm}^2$ has been therefore achieved at an annealing temperature of 375° for 60 s, which is remarkably lower than $1.2 \times 10^{-6} \Omega\text{-cm}^2$ obtained for the conventional Au/Ge/Pd ohmic metallization. In order to understand the roles of Mo/Ti diffusion barrier in the ohmic contact formation, samples without any diffusion barrier (Au/Ge/Pd/n-GaAs) and with single Ti-layer (Au/Ti/Ge/Pd/n-GaAs) were also fabricated. By comparing their results, the effects of the barrier metals on the As-outdiffusion and Au-indiffusion are clarified.

EXPERIMENTS

The GaAs epilayers were grown by the low-pressure metalorganic chemical vapor deposition (LP-MOCVD)⁹ system on (100)-oriented semi-insulating GaAs wafers. A 5000Å thick undoped GaAs buffer layer was grown prior to the 3500Å thick active layer with Si-doping concentration of around $2 \times 10^{18} \text{ cm}^{-3}$. The samples were patterned into transmission line model (TLM) testing structures. Then, the samples were rinsed in $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ (1:100) for 30 s immediately before loaded into a cryo-pumped electron beam

evaporator with a base pressure better than 2×10^{-6} Torr. The structure of the deposited Au/Ge/Pd metal layers without any diffusion barrier is as follows, Au(800Å)/Ge(1700Å)/Pd (500Å)/GaAs. For samples with Ti or Mo/Ti barrier metals, additional Ti(500Å) or Mo(300Å)/Ti(300Å) layers were deposited between the Au and the Ge layers, correspondingly. Since the efficiencies of the elemental-stuffed diffusion barrier Mo/Ti can be significantly improved by the additional oxygen atoms plugging easy path for migrations,⁸ therefore during evaporation, Au/Mo/Ti/Ge/Pd samples were exposed to oxygen after Ti deposition but before the following Mo deposition. After lift-off in acetone, the samples were then rapid-thermal-annealed (RTA) at various temperatures from 300 to 500°C at 25°C per interval for 60 s. During annealing, forming gas consisting of 13% H_2 and 87% N_2 was used as the ambient. The specific contact resistivities were derived using the TLM-pattern with the width of 60 μm and the spacings of 4, 6, 8, 10, 15, 20 μm, respectively. The length of the contact pad was 40 μm. The resistances of TLM patterns were measured by an HP-4156A precision semiconductor parameter analyzer with four probes, two of them for current source, and the others, for two individual voltage meters. Surface morphologies were inspected by the scanning electron microscopy (SEM). The depth profiles were carried out by Auger electron spectroscopy (AES) using VG-Micro LAB 310F.

RESULTS AND DISCUSSION

The TLM-derived specific contact resistivities (ρ_c s)

measured at room temperature as a function of annealing temperature for Au/Ge/Pd/GaAs, Au/Ti/Ge/Pd/GaAs, and Au/Mo/Ti/Ge/Pd/GaAs samples are shown in Figs. 1a, 1b, and 1c, respectively. For the Au/Ge/Pd samples, i.e. without any diffusion barrier, the minimum ρ_c is only $1.2 \times 10^{-6} \Omega\text{-cm}^2$ at the annealing temperature of 325°C . As observed, ρ_c degrades to about $7 \times 10^{-6} \Omega\text{-cm}^2$ as the annealing temperature is increased to 350°C . When the annealing temperature is further increased to 375°C , the respective ρ_c returns to a lower value of $3 \times 10^{-6} \Omega\text{-cm}^2$. But, for samples annealed above 400°C , ρ_c again increases with annealing temperature. With titanium deposited as the diffusion barrier metal between the Au-overlayer and the Ge/Pd/GaAs underlayers, a significant improvement of the electrical characteristics can be seen, as shown in Fig. 1b. Like the Au/Ge/Pd samples, the ohmic characteristics for the Au/Ti/Ge/Pd samples begin at 325°C and have a ρ_c of $7 \times 10^{-7} \Omega\text{-cm}^2$. However, the ρ_c further decreases to $3.2 \times 10^{-7} \Omega\text{-cm}^2$ at the annealing temperature of 350°C . This lower ρ_c is maintained up to the annealing temperature of 375°C , which implies a wider process window and also better thermal stability for the Au/Ti/Ge/Pd samples than that obtained for the Au/Ge/Pd ones. The ohmic contact resistivity gets worse with a value of $3 \times 10^{-6} \Omega\text{-cm}^2$ at the annealing temperature of 400°C and improves to an average value of $3 \times 10^{-7} \Omega\text{-cm}^2$ at the annealing temperature of 425°C . Above 425°C , ρ_c begins to increase with annealing temperature again. As for the Au/Mo/Ti/Ge/Pd/n-GaAs samples, the onset of ohmic characteristics with the ρ_c as low as $3 \times 10^{-7} \Omega\text{-cm}^2$ also occur at the same

annealing temperature of 325°C like the previous two. The ρ_c can further be reduced to $2 \times 10^{-7} \Omega\text{-cm}^2$ at the annealing temperature of 375°C . At 400°C , the ρ_c increases to a value of $9 \times 10^{-7} \Omega\text{-cm}^2$. These properties demonstrate that the ohmic characteristics and thermal stability for the Au/Mo/Ti/Ge/Pd samples are best among these three metallization schemes. This is conjectured to be associated with the most efficient Mo/Ti diffusion barrier. However, the specific contact resistivity increases significantly to a high value of $5 \times 10^{-5} \Omega\text{-cm}^2$ at the much higher annealing temperature of 450°C , and the ρ_c the decreases to a very low value below $10^{-7} \Omega\text{-cm}^2$, for which values the TLM-model is no longer valid.

To understand the effect of the diffusion barrier, the SEM micrographs are used to observe the specimens' surface after annealing. For Au/Ge/Pd samples annealed at 325 , 350 , 375 , and 400°C , the corresponding SEM pictures are shown in Figs. 2a–2d, respectively. The surfaces are more or less smooth from 325 to 400°C except that tiny holes were found to grow in size and density with annealing temperature. For Au/Ti/Ge/Pd/GaAs samples, the changes of the surface morphologies with annealing temperature are much more complex. For the annealing at 350°C , the surface is very smooth, as can be seen in Fig. 3a. But it degrades remarkably at 400°C , which is depicted in Fig. 3b. For even higher annealing temperature, lots of islands are present, as shown in Figs. 3c and 3d for the samples annealed at 425 and 475°C , respectively. By depositing an additional Mo-layer, namely Au/Mo/Ti/Ge/Pd/GaAs specimens, the surface morphologies are significantly improved and magnified SEM micro-

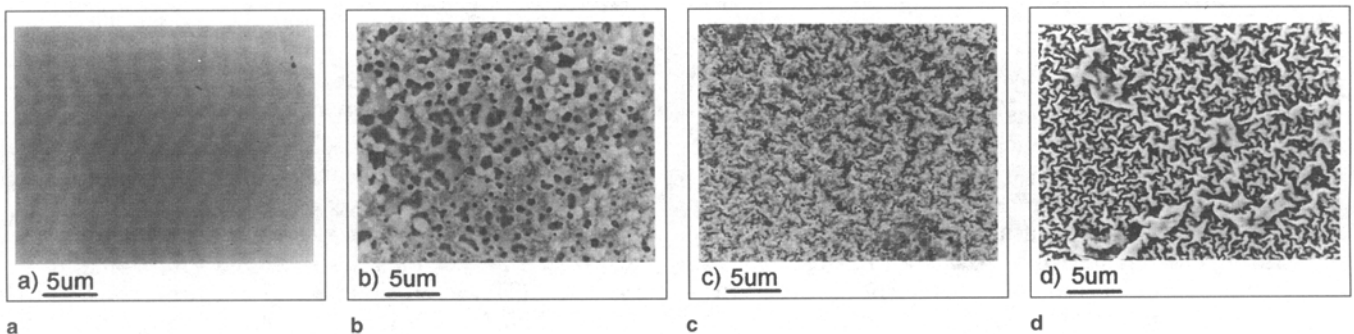


Fig. 3. Surface morphology of the samples deposited with the Au/Ti/Ge/Pd metallizations rapid thermal annealed for 60 s at different annealing temperatures. (a) 350°C , (b) 400°C , (c) 425°C , and (d) 475°C .

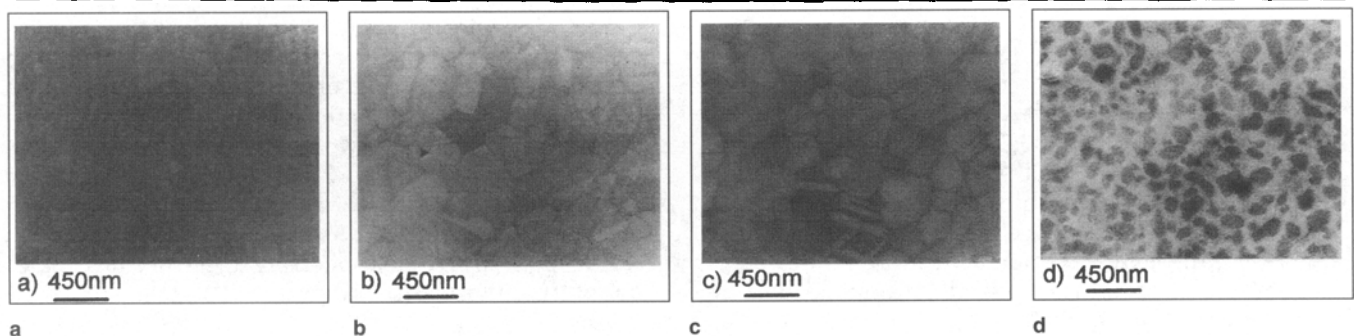


Fig. 4. Surface morphology of the Au/Mo/Ti/Ge/Pd metallization samples rapid thermal annealed for 60 s at different annealing temperatures. (a) 350°C , (b) 450°C , (c) 475°C , and (d) 500°C .

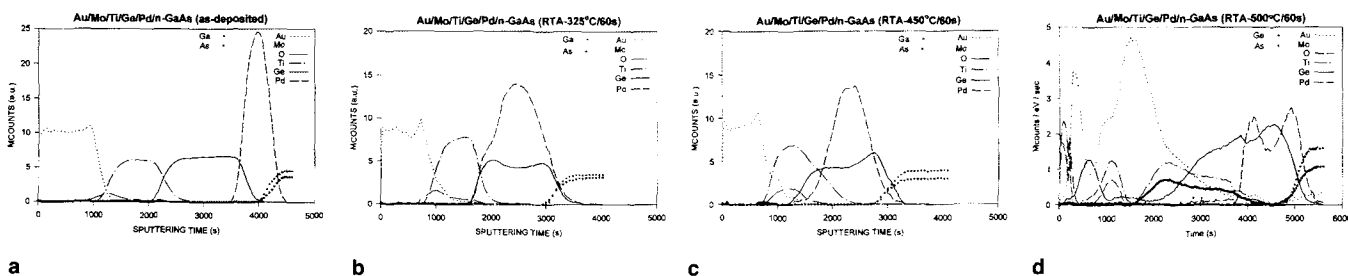


Fig. 5. AES depth profiles of each element for (a) the as-deposited Au/Mo/Ti/Ge/Pd/n-GaAs sample and those rapid thermal annealed for 60 s at the annealing temperatures of (b) 325, (c) 450, and (d) 500°C.

graphs are therefore shown. The micrographs for the samples annealed at 350, 450, and 475°C are shown in Figs. 4a–4c, respectively. The very smooth surface morphology is supposed to be due to the superior efficiency of the Mo/Ti-bilayer as the diffusion barrier for the As-outdiffusion and Au-indiffusion. Hence, the surface of the sample annealed at 500°C is still more or less smooth, as shown in Fig. 4d. Further increase in the annealing temperature deteriorates the surface morphology of the samples.

Because of the significant influences of the diffusion barrier on the variations of the electrical characteristics and the surface morphologies with annealing temperature described above, the As-outdiffusion and Au-indiffusion are therefore thought to be very important to the performances of ohmic contacts. Since many tiny holes are observed in the Au/Ge/Pd samples even at the annealing temperature of 325°C and since the H_2 contained in the forming gas annealing ambient is expected to easily carry As away, it is believed that the higher ρ_c s for the Au/Ge/Pd samples without any diffusion barrier are caused by the As-outdiffusion, resulting in the deterioration of GaAs surface. Also, Au diffuses easily through the metallic overlayer to react with Ga and provide many Ga vacancies for Ge-incorporations. The formation of Ga vacancies and the enhancement of Ge-doping in GaAs then compensate the effects from the As-outdiffusion, which are surmised to be responsible for the improvement of ρ_c s to a lower value again. But, massive interactions between Au and the GaAs substrates¹⁰ as well as the persistent As-outdiffusion for even higher annealing temperature would destroy the active layer and thus result in the further degradation of ρ_c s. By additionally depositing a Ti or Mo/Ti-bilayer, good diffusion barrier is provided. Because these two types of samples have similar electrical characteristics from 325 to 400°C, it seems that they do not differ significantly in the ability to prevent As-outdiffusion. But the onset of the second lowering of ρ_c for the Au/Ti/Ge/Pd/GaAs samples occurs at 425°C, which is significantly lower than 500°C for the Au/Mo/Ti/Ge/Pd/GaAs ones. This is due to the difference in the efficiencies of retarding the Au-indiffusion by the Ti and Mo/Ti-bilayer. The Au/Mo/Ti/Ge/Pd specimens possess the highest contact resistivity at the 450°C annealing among these three types of samples, which is also attributed to the efficient retardation of the Au-indiffusion by the Mo/Ti-bilayer.

To further clarify the barrier effect of the Mo/Ti-bilayer on the As-outdiffusion and Au-indiffusion, AES depth analysis is performed. The depth profile of each element for the as-deposited Au/Mo/Ti/Ge/Pd samples are shown in Fig. 5a. No obvious interaction among different layers is found. The TiO_x formed by the exposure to the oxygen after the deposition of Ti is observed at the interface between Mo and Ti where the tail of Au ends. In Fig. 5b, for the samples annealed at 325°C achieving low ρ_c , the distribution of As moves very slightly further toward the surface than the Ga. But it seems that the ohmic characteristics are not deteriorated. The distributions of Pd and Ge imply the formation of PdGe phase at the GaAs surface. This is consistent with previous investigations^{11–13} that the PdGe is essential to obtaining low ρ_c s. The retardation of Au-indiffusion by the Mo/Ti-bilayer is obvious from the distribution of Au being restricted to behind the oxygen signal of the TiO_x . This result is consistent with the previous model.⁸ Since the solubility of Au is very low in bulk Mo, Au atoms can migrate into the Mo layer through the structural defects in the Mo film. When the Ti and Mo are continuously deposited in a good vacuum condition, the Au can therefore get through the defects in the Mo-layer to the Mo/Ti interface. However, in the samples with Ti layer exposed to oxygen before the deposition of Mo, all the easy paths for diffusion are blocked by oxygen atoms resulting in the prevention of Au-indiffusion and As-outdiffusion. Hence, the Mo/Ti layer as a very efficient diffusion barrier does contribute to the formation of excellent ohmic contacts. The AES profiles for the sample annealed at 450°C are shown in Fig. 5c. The distributions of Ga and As are the same as those annealed at 325°C. Also the distribution of Au is still blocked by the TiO_x , although the oxygen atoms have moved deeply into the Ti layer. The only significant difference is in the distributions of Pd and Ge. An abnormally high Ge-containing layer is obviously formed on the GaAs surface, which is correlated to the degradation of ρ_c . It is believed that high doping concentrations of Ge in GaAs results in highly compensated material and in some cases even p-type material.^{13,14} Hence, the Mo/Ti bilayer significantly resists the Au-indiffusion, leading to the highly compensated layer. For the samples annealed at 500°C, Au atoms eventually migrate through the metal layers into the GaAs. The indiffusion of Au is expected to enhance the creation of

Ga vacancies and therefore assist the Ge-incorporation which is responsible for the lowering of ρ_c s. Since the layered metal structure is destroyed by the indiffusion Au, the elements are found to mix with each other in a complicated way as shown in Fig. 5d. On the other hand, the significant outdiffusion of As is also observed to be deterred by the Mo/Ti barrier.

CONCLUSIONS

In summary, samples with three different types of metallization structures are adopted to understand the influences of barrier metals on the ohmic characteristics of Au/Ge/Pd/GaAs. For Au/Ge/Pd/GaAs samples without any diffusion barrier, the specific contact resistivities are remarkably higher than those with barriers of Ti and Mo/Ti. In addition, a large number of tiny holes are found for the Au/Ge/Pd specimens but not for the samples with Ti and Mo/Ti barriers. The barrier metals are therefore surmised to effectively reduce the As-outdiffusion during thermal annealing. Consequently, the Au/Mo/Ti/Ge/Pd and the Au/Ti/Ge/Pd specimens possess lower ρ_c s and better thermal reliability. For the Au/Mo/Ti/Ge/Pd samples, minimum ρ_c as low as $2 \times 10^{-7} \Omega\text{-cm}^2$ can be achieved at an annealing temperature of 375°C, and the annealing temperature range for such low ρ_c s can be extended to about 400°C. Moreover, the efficient retardation of the Au-indiffusion by the Mo/Ti-bilayer clarified by the AES depth profile results in a turn-around phenomenon of the specific contact resistivity at the relatively high annealing temperature of ~500°C. Hence, the efficient diffusion barrier of Mo/Ti is proven to be very useful for Au/Ge/Pd/n-GaAs ohmic contacts.

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REFERENCES

1. N. Braslau and J.B. Gunn and J.L. Staples, *Solid-State Electron.* 10, 38 (1967).
2. E.D. Marshall, W.X. Chen, C.S. Wu, S.S. Lau and T.F. Kuech, *Appl. Phys. Lett.* 47, 298 (1985).
3. E.D. Marshall, C.S. Wu, C.S. Pai, D.M. Scott and S.S. Lau, *Thin Films: The Relationship of Structure to Properties*, ed. C.R. Aita and K.S. Sree Harsha 47, 161 (Pittsburgh, PA: Mater. Res. Soc., 1985).
4. E.D. Marshall, B. Zhang, L.C. Wang, P.F. Jiao, W.X. Chen, T. Sawada, S.S. Lau, K.L. Kavanagh and T.F. Kuech, *J. Appl. Phys.* 62, 942 (1987).
5. J.T. Lai and J.Y.M. Lee, *Appl. Phys. Lett.* 64, 306 (1994).
6. A. Paccagnella, L.C. Wang, C. Canali, G. Castellaneta, M. Dapor, G. Donzelli, E. Zanoni and S.S. Lau, *Thin Solid Films* 187, 9 (1990).
7. W.C. Huang, T.F. Lei and C.L. Lee, *J. Electron. Mater.* 23, 397 (1994).
8. J.W. Mayer and S. S. Lau, *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Ch. 11, 331 (Macmillan, 1990).
9. J.W. Wu, Ph.D. Thesis, National Chiao Tung University (1995).
10. R. Williams, *Modern GaAs Processing Methods*, (London: Artech House, 1990).
11. W.Y. Han, Y. Lu, H.S. Lee, M.W. Cole, L.M. Casas, A. DeAnni, K.A. Jones and L.W. Yang, *J. Appl. Phys.* 74, 1 (1993).
12. M.W. Cole, W.Y. Hane, L.M. Casas, D.W. Eckart and K.A. Jones, *J. Vac. Sci. Technol. A* 12, 1904 (1994).
13. C.J. Palmstrom, S.A. Schwarz, E. Yablonovitch, J.P. Harbison, C.L. Schwartz, L.T. Florez, T.J. Gmitter, E.D. Marshall and S.S. Lau, *J. Appl. Phys.* 67, 1 (1990).
14. J.T. Lai and J.Y. Lee, *J. Appl. Phys.* 76, 1 (1994).