行政院國家科學委員會專題研究計畫　期中進度報告

總計畫暨子計畫十：低功率系統架構及整合模擬研究(2/3)

計畫類別：整合型計畫
計畫編號：NSC93-2220-E-009-013-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學電子工程研究所

計畫主持人：溫瓌岸
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報告類型：完整報告

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中　華　民　國 94 年 5 月 30 日

行政院國家科學委員會補助專題研究計畫 □ 成 果 報 告
■ 期中進度報告

低功率系統之設計及自動化
子計畫十：無線 SOC 產品整合發展平台

計畫類別：□ 個別型計畫　　■ 整合型計畫
計畫編號：NSC 93-2220-E-009-013
執行期間：93 年 08 月 01 日 至 94 年 07 月 31 日

計畫主持人：溫瓌岸 教授
計畫參與人員：周美芬、莊源欣、彭嘉笙、陳哲生、林立協、鄒文安、林格輝、宋兆鈞、黃相霖、趙皓名、楊富昌、吳健銘、蔡彥凱、張懷仁、游振威、賴俊憲、洪志德、廖俊閔、張書瑋、張乃華、翁淑怡、楊惠雲、王裕欽、楊天仁

成果報告類型(依經費核定清單規定繳交)：□精簡報告　■完整報告

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■涉及專利或其他智慧財產權，□一年■二年後可公開查詢

執行單位：國立交通大學 電子工程學系

中華民國 94 年 5 月 26 日

Content

Design Descriptions

以無線無線 SOC 產品整合發展平台，實作適用於超寬頻無線通信規格（UWB）使用的 IFFT/FFT 模組，採用低功率、低面積、低操作延遲的目標設計。從架構設計、電路設計到整合於發展平台的實際電路驗證，以及 FPGA 平台上的量測驗證。並以 IP 化的方式為導向，可適用於其他採用與此類似規格的系統當中。

1. Architecture Specification

1.1 UWB Baseband Building Blocks:

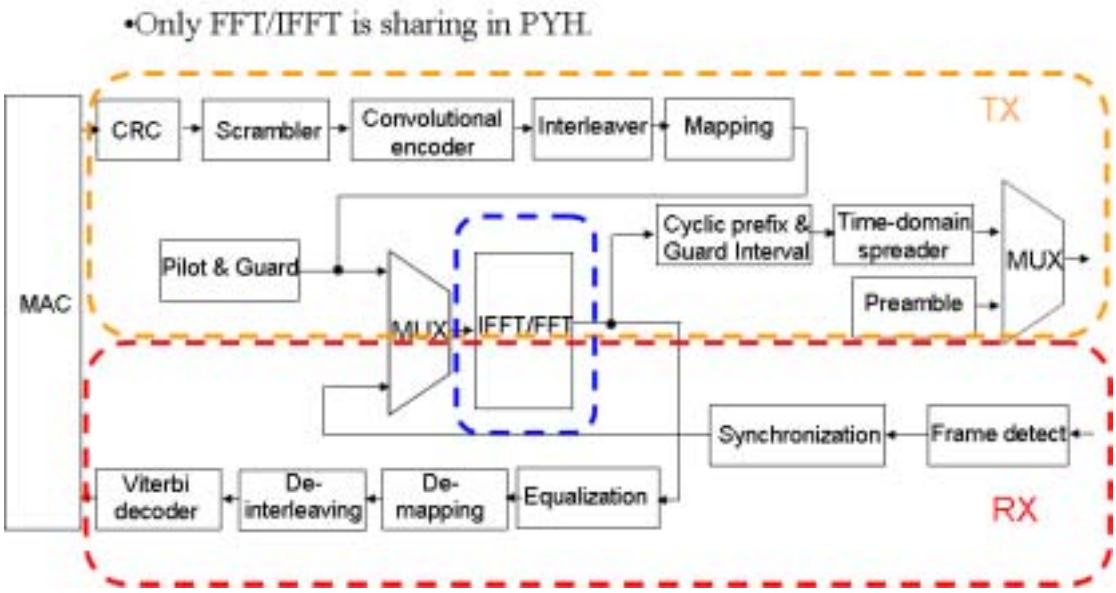


Figure 1.1 UWB Baseband Building Blocks

1.2 128 points FFT/IFFT for UWB spec.

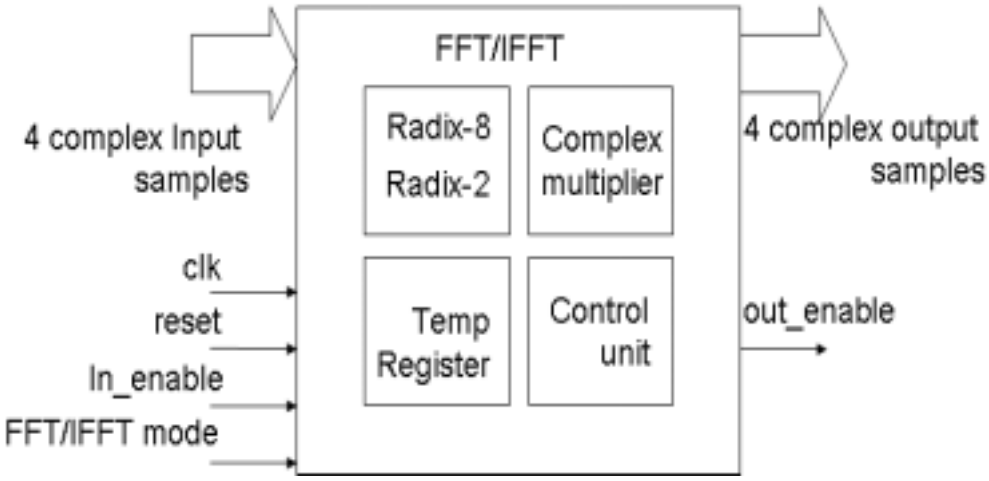


Figure 1.2 128 points FFT/IFFT for UWB spec.

input and output port specification

a. UWB 128 points FFT/IFFT period = 242.42ns (clock rate = 528 MHz about 1.89 ns/sample)
b. Input 5 bits and output 8 bits for system required
c. Parallel 4 complex sample input and 4 complex sample output (clock rate = 528MHz / 4 = 132MHz)
d. Latency 32 clock cycles.

1.3 128 points FFT/IFFT data flow diagram.

There is four radix-2 butterfly at first stage.

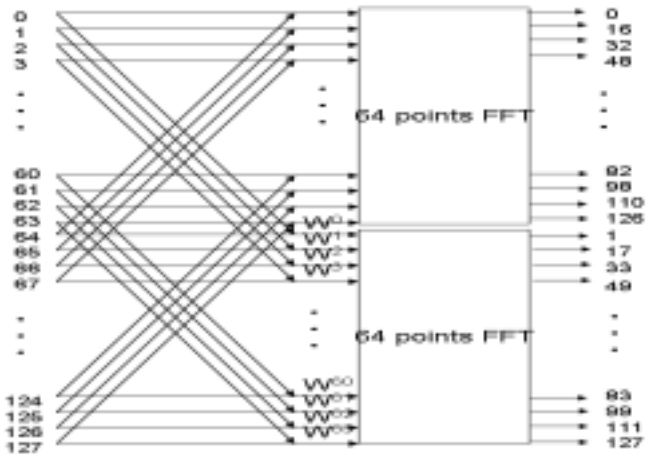


Figure 1.3-a 128 points FFT/IFFT data flow diagram

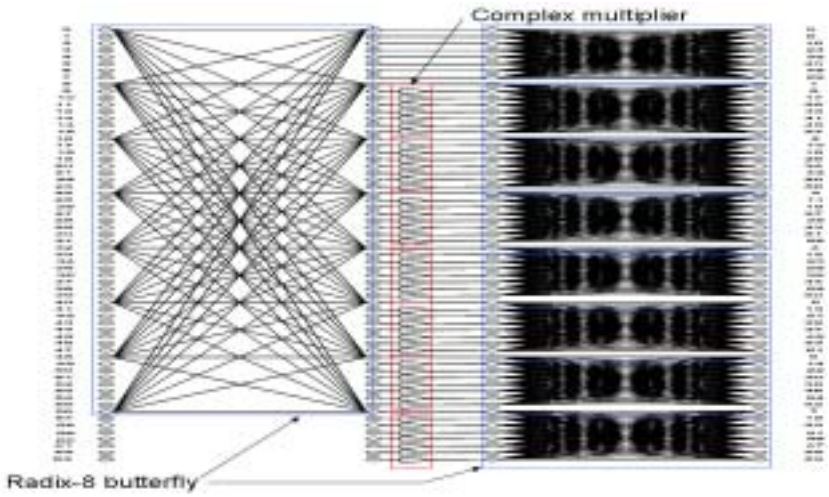


Figure 1.3-a 64 points FFT data flow diagram

1.4 Radix-8 butterfly data flow diagram.

The Radix-8 butterfly is composed by 12 Radix-2 butterfly and there is 7 complex multiplier at stage 3. The twiddle factor $e^{-j*pi/4}$ is implement by the shift adder and not necessary to use a multiplier. There is a critical path exclude complex multiplier show at figure 1.4.

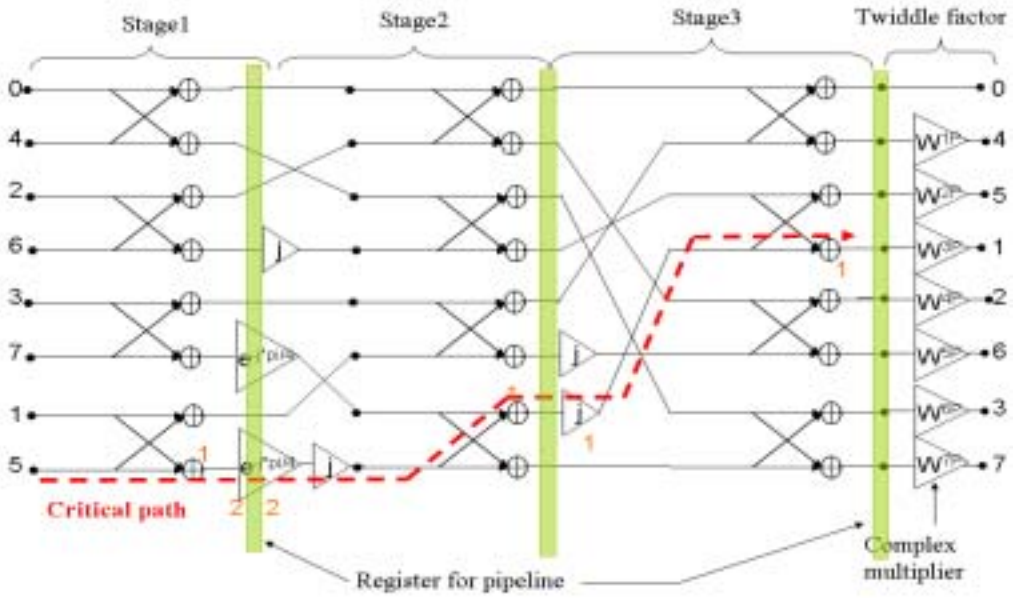


Figure 1.4 Radix-8 butterfly data flow diagram.

1.5 Twiddle factor multiplication.

1. General complex multiplier.
   - 4 real multiplication and 2 additions.
   - 2 stage pipeline.
2. CORDIC-Based phase rotator.
   -2N sequential additions.
   -N stage pipeline.
3. MAC-Based complex multiplier.
   -3 real multiplication and 3 additions and 2 subtractions.
   -3 stage pipeline.

	Gate count	Speed	Latency
General complex multiplier	**4.2k**	**3.15ns**	**3**
MAC-Based complex multiplier	**4.0k**	**3.17ns**	**4**
CORDIC-Based phase rotator	**3.2k**	**3.0ns**	**12**

* Design Analyzer UMC018 slow library

•General complex multiplier is better in this design because of
   -Low latency .
   -High speed .

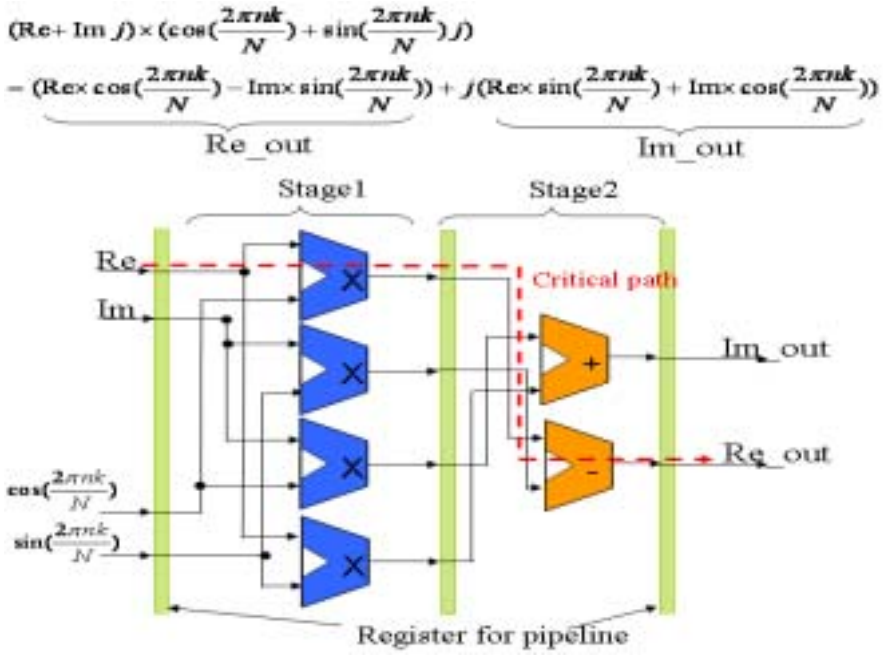
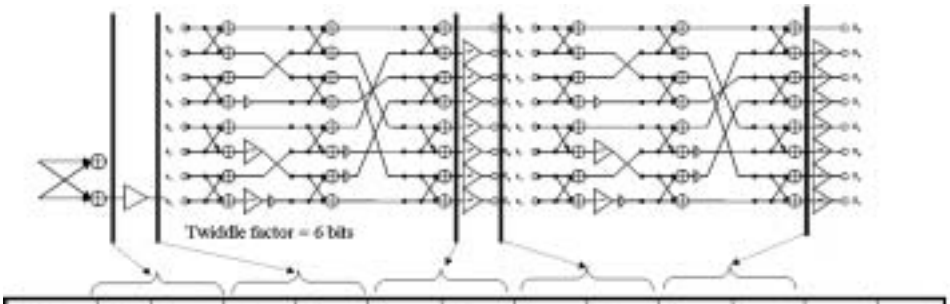


Figure 1.5 general complex multiplication

2. Behavior Specifications

2.1 Matlab simulation about word length decision

Figure 2.1 is a diagram that presents each stage quantize and scale status. If scale bit = 1 and quantize bit = (8.0), that means the LSB is removed 1 bit and we gets the MSB 8 bits. The format (8.0) means there are 8 bits at dot left side and 0 bit at dot right side. We make the input bits = 5 and the intermediate word length N , N=5~10 bits. Intermediate word length is the register and multiplier length which determinate the circuit area and EVM error. The EVM vs word length N is sketched at figure 2.2.



Stage	A	A	B	B	C	C	D	D	E	E		
operation	Scale bit	Quantize bit	Scale bit	Quantize bit	Scale bit	Quantize bit	Scale bit	Quantize bit	Scale bit	Quantize bit	SQNR Error(dB)	SQNR round (dB)
5 bits	1	(5.0)	1	(5.0)	2	(5.0)	0	(5.0)	1	(5.0)	7.41	12.32
6 bits	0	(6.0)	1	(6.0)	2	(6.0)	0	(6.0)	1	(6.0)	13.65	18.88
7 bits	0	(7.0)	0	(7.0)	2	(7.0)	0	(7.0)	1	(7.0)	19.97	25.58
8 bits	0	(8.0)	0	(7.1)	1	(8.0)	0	(8.0)	1	(8.0)	26.04	30.96
9 bits	0	(9.0)	0	(7.2)	0	(9.0)	0	(9.0)	1	(9.0)	31.80	36.03
10 bits	0	(10.0)	0	(7.3)	0	(9.1)	0	(9.1)	0	(10.0)	36.25	38.64

➢128*10000 points simulation

Figure 2.1 A diagram for each stage word length decision

2.2 Matlab simulation result for word length decision

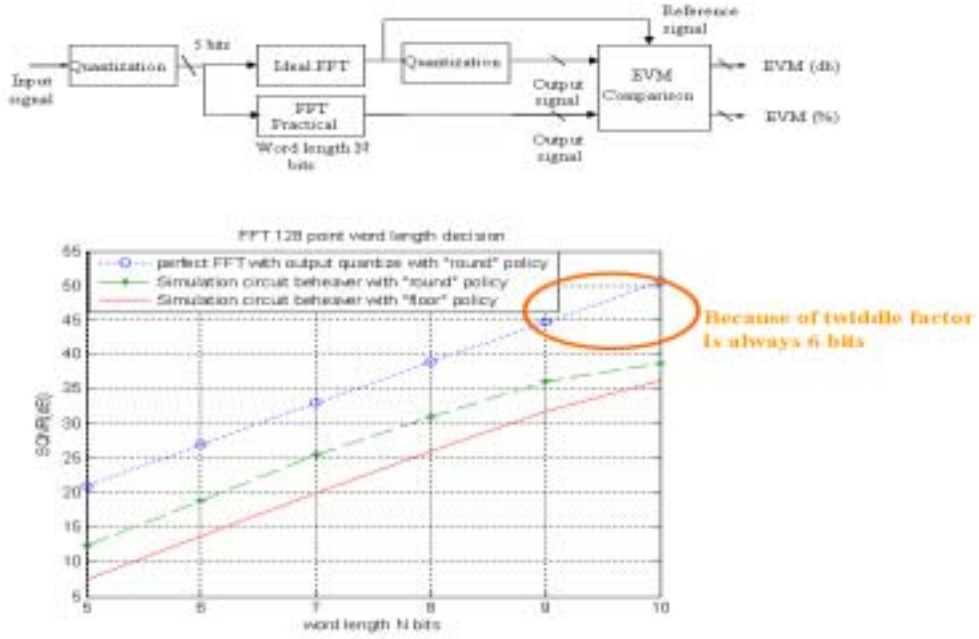


Figure 2.2 EVM(%) vs word length N bits

2.3 Matlab FFT and IFFT

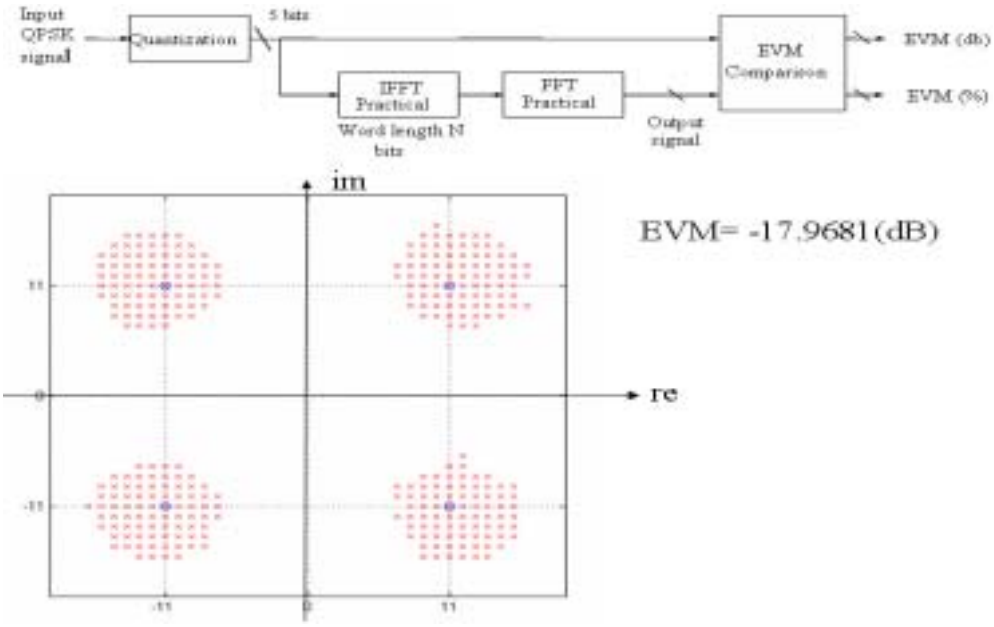


Figure 2.3 FFT and IFFT

3. Circuit Specifications

3.1 Circuit block diagram

Figure 3.1 circuit block diagram show the data path of 128 points FFT/IFFT. There are total 7 complex multipliers at this design. There are 4 complex multiplier for radix-2 butterfly and can share with radix-8 butterfly at different time. The detail can see the figure 3.2 delay diagram to realize each component's operation.

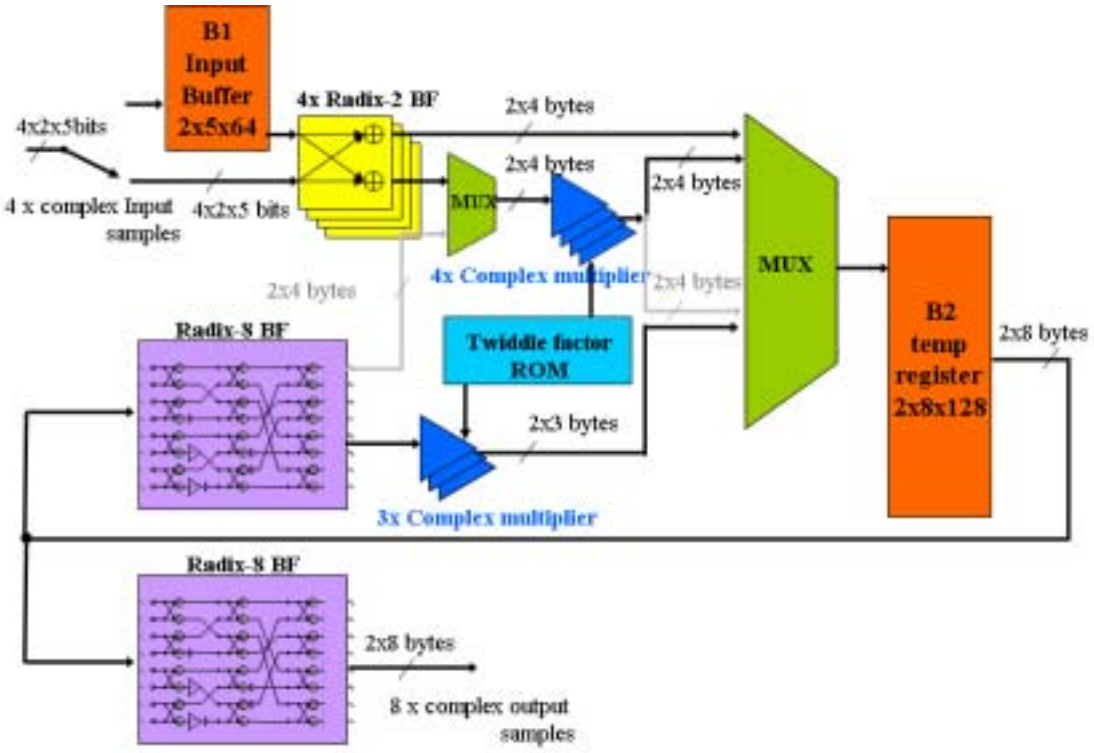


Figure 3.1 Circuit block diagram

3.2 Circuit delay diagram

Because of the first stage is radix-2 butterfly, the input data can be process after 16 clock cycles. The second stage is radix-8 butterfly and all the complex multiplier is working at the same time. The third stage that need no complex multiplier and

store the result at B3 . Figure 3.2 shows two 128 points pattern input and the operation at each clock cycles.

- Latency =32+16+1=49 clock cycle.

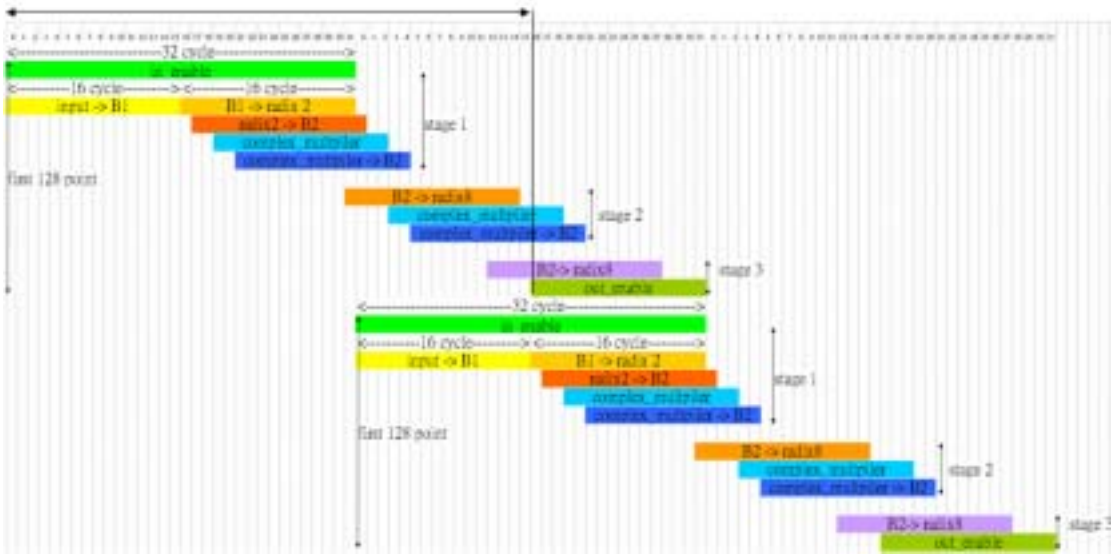


Figure 3.2 Circuit delay diagram

4. Circuit Verification

4.1 ADS RTL Verification with random pattern input

RTL core is compiler to an ADS function block and compare with the golden module which is default at ADS environment. The ADS block diagram can see figure 4.1-a.We can compare the output signal from the golden module and RTL module, see figure 4.1-b.

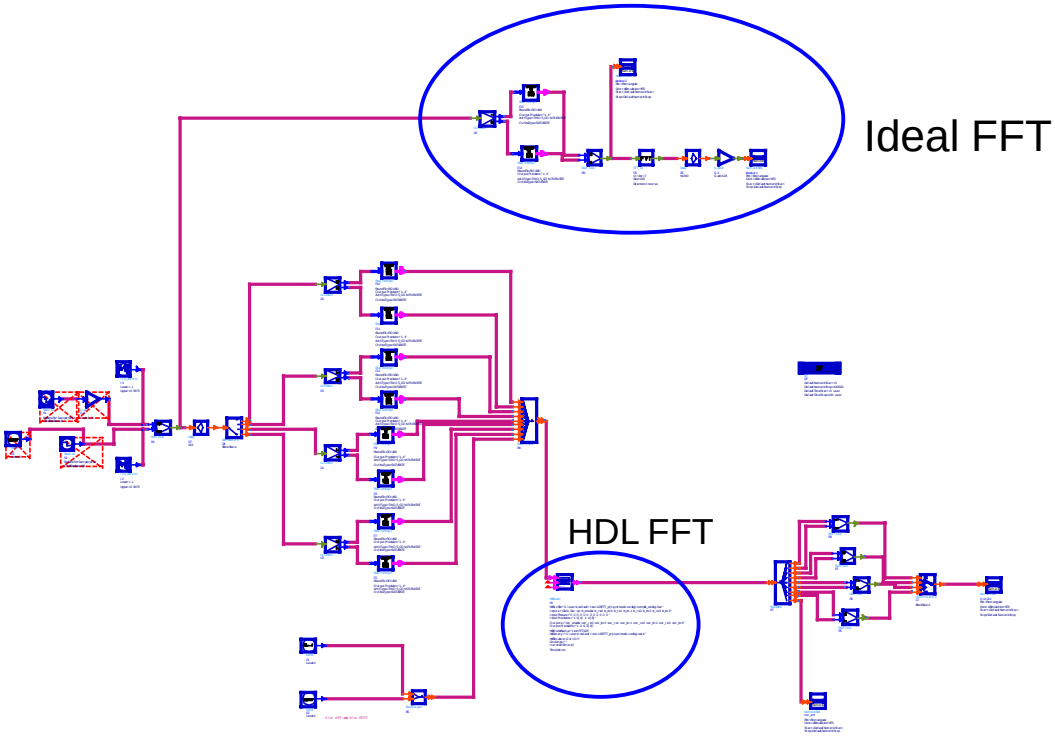


Figure 4.1-a ADS verification blocks

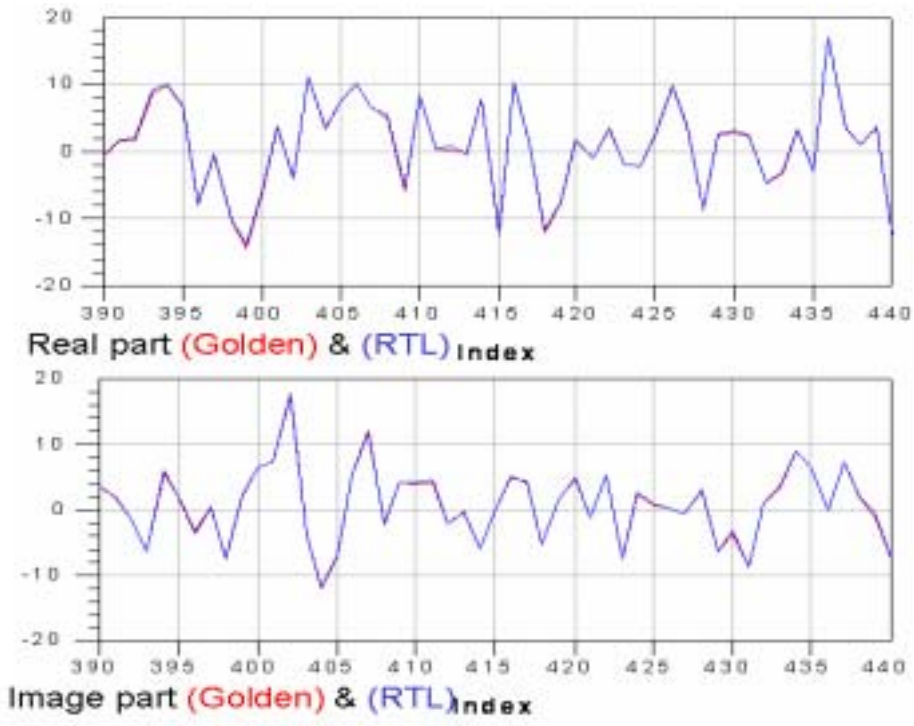


Figure 4.1-b Golden module(red) & RTL module(blue) output signal

4.2 Test bench

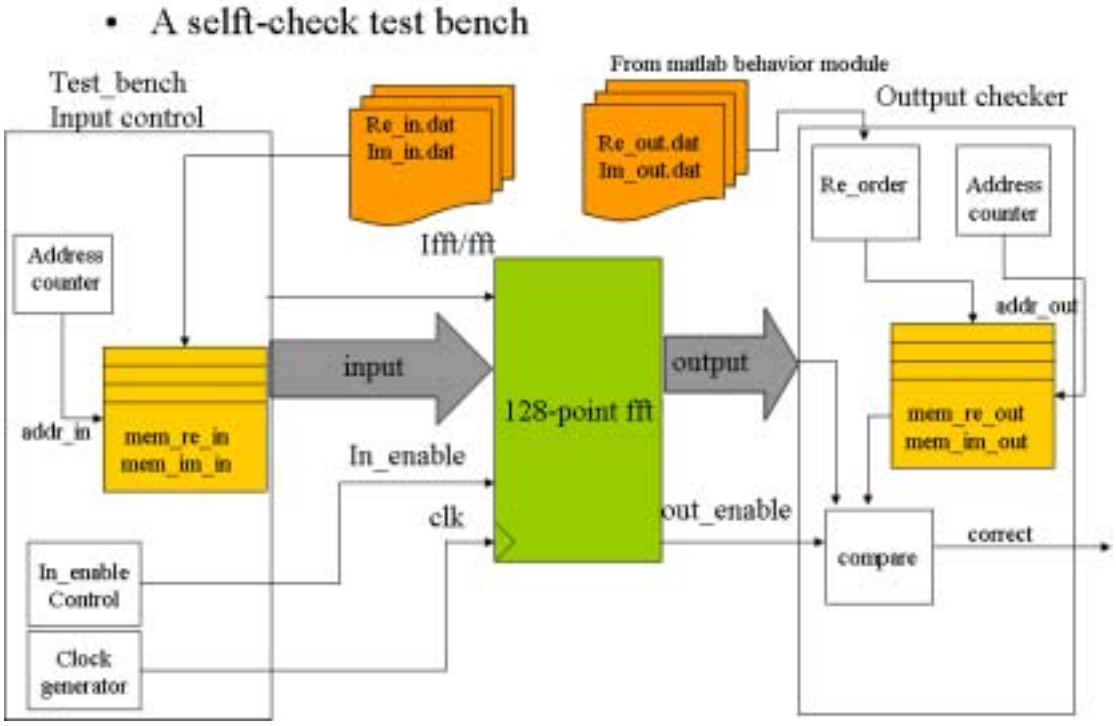


Figure 4.2 Self-test test bench

4.3 FPGA prototype verification

For FPGA prototype verification use two additional circuit that is serial-to-parallel and parallel-to-serial. It is more easy to monitor the output signal and compare the output with ideal signal.

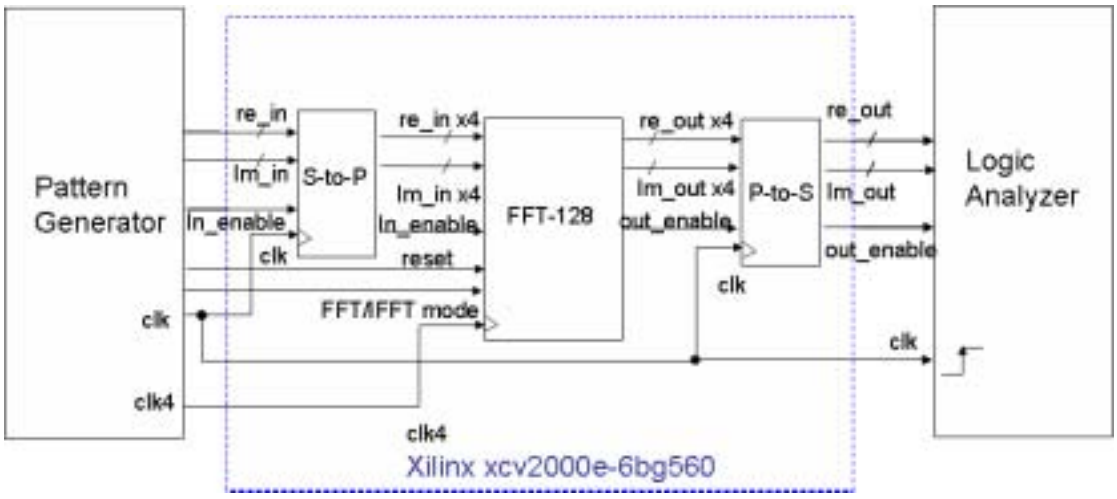


Figure 4.3 FPGA verification plan

4.3 FPGA synthesis report

Number of SLICES :14269 out of 19200 74%

Clock to Setup on destination clock clk4

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
clk	19.984			
clk4	61.180			

5. Synthesis report

Synthesis environment: Synopsys Design Analysis

Library(s) Used

slow (File: /home/lib/syn/slow.db)

Number of ports: 109

Number of nets: 29854

Number of cells: 27662

Number of references: 165

Combinational area: 782351.562500

Noncombinational area: 638927.812500

Net Interconnect area: undefined (No wire load specified)

Total cell area: 1421224.375000

Total area: undefined

Data arrival time : 4.67 ns

6. Chip Layout

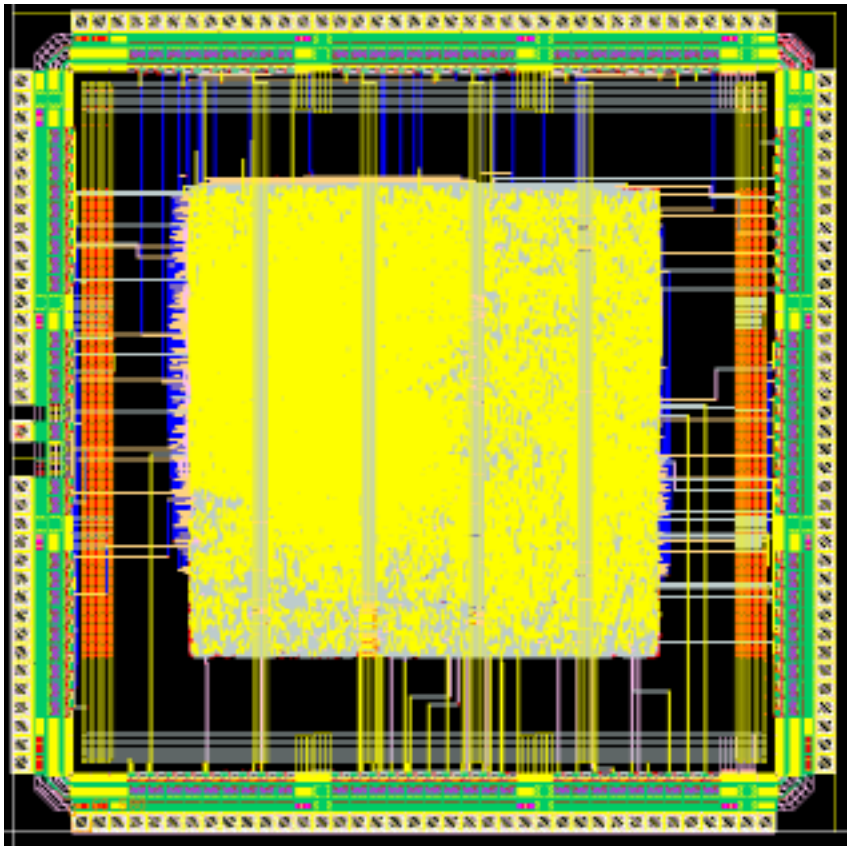


Figure 4.2 Chip Layout view

Core width: 1524.34 um

Core height: 1524.34 um

Die width: 2674.36 um

Die height: 2674.36 um

Core Utilization: 0.77666

7. Post Layout Simulation

After Place and Route, we can use Soc encounter to extract RC and dump delay information. Soc encounter can save the netlist that is after place and route. We can

use ncverilog to simulate the output waveform.

Synthesis timing report	Timing after Place & Route
Slow library: 125°C 1.62v	Slow library: 125°C 1.62v
4.67ns	8.22ns

Timing not met, require timing is 7.57ns but after Place & Route it lost about 0.65ns.Timing is slack !!

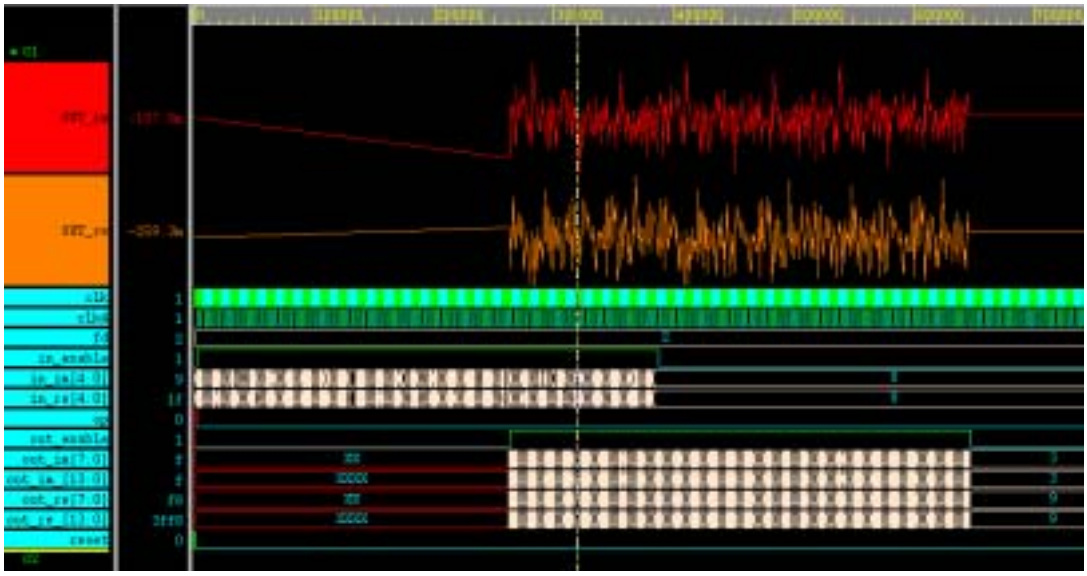


Figure 7 Post layout simulation waveform (clock period = 10 ns)

8. Testing Plan

Use CIC tester. Writing test pattern for tester format and mapping to Chip port.

9. Logistic Information

9.1 Design Flow

Figure 11.1 show the design flow of digital baseband design. Building Matlab behavior is important for RTL code verification and for quantization error

analysis. After function verification the RTL code must be synthesizable and no latch in this design. Making sure the timing constrain is enough and timing is met. Prepare the required file and library to place and route, then decision the utilization of core. Place and route must take a lot of time for downsize and timing optimization. If the DRC or LVS not pass, checking the library and operation flow, than retry again until the DRC and LVS is pass.

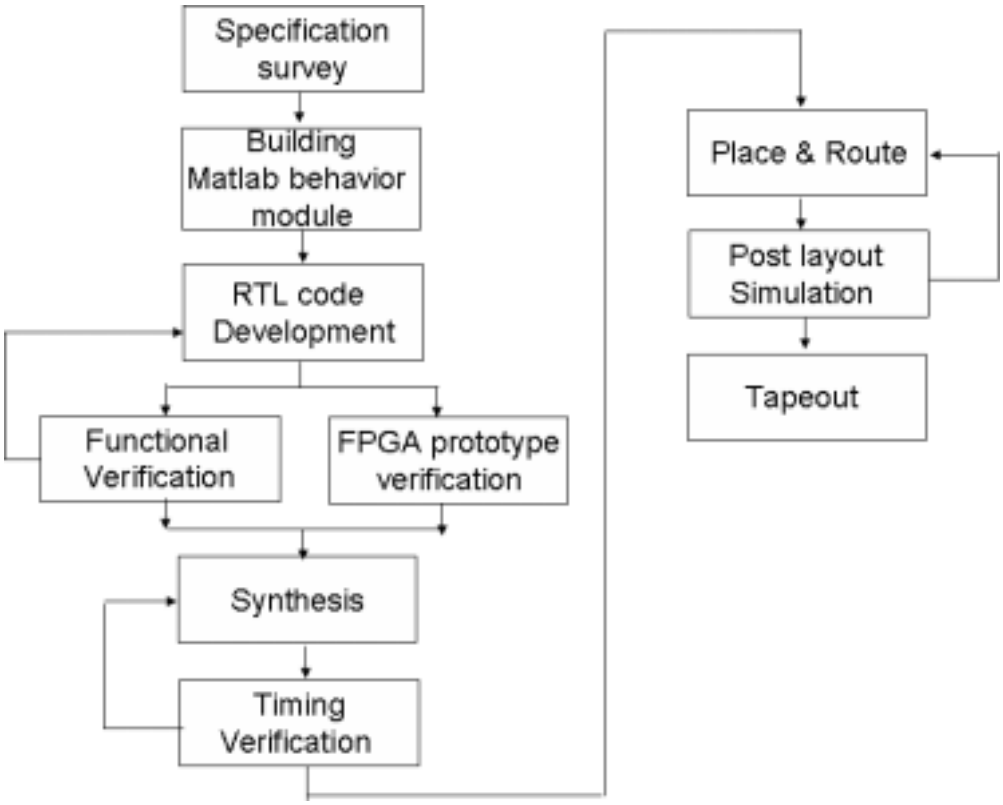


Figure 11.1 design flow diagram

9.2 EDA Tools version

a. Synthesis tool : Synopsys Design Analysis V-2003.12 for linux Nov 19 , 2003

b. Place and Route tool : Canence Soc encounter 4.1

-first encounter v04.10-p003_1

-NanoRoute nanoroute Version v04.10-p554 NR040529-0140/USR20-UB

c. Verilog Simulation tool : ncverilog.

d. Wave form viewer : Debussy nWave.

9.3 Tapeout Information

Process	UMC 0.18-um
Shuttle Date	JAN 2, 2005
Chip ID	L18501
Purpose	
LEF	umc18_6lm.lef umc18_6lm_antenna.lef umc18io3v5v_6lm.lef
LIB	fast.lib slow.lib typical.lib umc18io3v5v_fast.lib umc18io3v5v_slow.lib umc18io3v5v_typ.lib
Standard cell	Artisan fb_umc18_sc-x_2003q4v2
I/O cell	Artisan fb_io-gp-18-23-50-il-v00_2003q4v1
EDR	G-02-LOGIC18-1.8V/3.3V-1P6M-GENERICII-EDR
DRC	G-DF-LOGIC18-1.8V-3.3V-1P6M-Calibre-drc-2.4-p6
TLR	G-03-LOGIC18-1.8V_3.3V-1P6M-TLR
Layout Area	5000x5000 um
Package	