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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
□期中進度報告

The Researches of Growth Mechanism and Control of One-Dimensional Silicon Nanowires

一維矽奈米線成長機制與控制之研究(I)

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計畫編號：**NSC　93 － 2215 － E － 009 －　045 －**
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Introduction

In recent years, resulting from quantum size effects in the electronic transport, one-dimensional silicon nano-wires (SiNWs) have much interest because of their different electronic and optical characteristics compared with bulk materials [1-4]. Silicon nano-wires have been also proposed for other applications such as ultra-sensitive bolometers [5] and high sensitive biological and chemical sensors [6], etc. There are many methodologies have been proposed in the literature for the fabrication of silicon nanowires. Based on the vapor-liquid-solid (VLS) growth mechanism [7], various techniques have been developed to fabricate SiNWs, mainly including laser ablation [8], chemical-vapor-deposition (CVD) [9-11], thermal evaporation [12,13], electrochemistry [14], stress limited oxidation [15,16], self-assembling [17], etching processes [18], solid-liquid-solid (SLS) [19,20]. In the vapor-liquid-solid (VLS) growth mechanism, the role of the metal catalyst is to form a liquid alloy droplet of relatively low solidification temperature. The metals used to catalyze silicon nano-wire growth include Au, Fe, Zn, Ni, Co, and Ti. Gold has been generally used in this process because the Au-Si alloy has a low eutectic temperature. However, this method needs to supply silicon sources such as silane (SiH_4) or silicon tetrachloride ($SiCl_4$) to fabricate silicon nano-wire. In this paper, we report that SiNWs can be controllably grown on a silicon substrate via a solid-liquid-solid (SLS) growth mechanism.

Experiment

The procedure of was described briefly as the following and the flow chart was shown in figure 1. First, silicon wafers were cleaned with a standard RCA cleaning procedure. Next, a thin layer of catalytic metal (Ni) was deposited on the wafer surface by electron beam evaporation. Then, the samples were loaded into a thermal furnace of 6 inch diameter size for the synthesis of silicon nano-wires. The silicon nano-wires were grown at a variety range of temperatures from 850C to 1050C, and a nitrogen gas used to preventing the oxidation of nano-wires during synthesis was the ambient gas flow which could also be varied with different flow rates. Field emission Scanning electron microscope (FESEM) was performed to characterize the morphologies of the silicon nanowires synthesized at different conditions. An energy dispersive X-ray analyzer (EDX) was also adopted for an investigation of the growth model of the silicon nano-wires.

Results and discussion

Influence of nitrogen gas flow rate

The silicon wafers cleaned with RCA procedures was coated with 40nm Ni by electron beam evaporation. The furnace temperature was sustained at 950℃ for 15 min as the ambient nitrogen

gas flow rates varied with different conditions, 0.5 slm, 2.5 slm, 5 slm, and 10 slm, respectively. Figure 2 represented the results which were clearly seen that as the nitrogen flow rates increased, the quantity of silicon nano-wires also increased. The ambient gas was believed to take the heat away from the surface of wafers and provide the effect of super cooling which could create the growth sites of nano-wires. Therefore, when the heat was driven away from the catalysts, the driving force for segregation of silicon nano-wires would enhance and they could protrude and grow from the surface of catalysts.

Influence of synthetic temperature

In this case, catalyst thickness of 400A was used for synthesis at the ambient flow rate of 10 slm for 15 min. According to the binary phase diagram of Ni-Si, the lowest melting point of liquid was around 900℃. Therefore, it was supposed that the nano-wire synthetic temperature should be higher than the lowest melting temperature. Four different temperatures were conducted for the observation of silicon nano-wire growth. As shown in figure 3, there were nano-wire successfully synthesized at temperatures higher than 900℃, which was consisted with the work completed by Yu and et al [19,20]. Since higher temperatures supplied more heat for the movement of atoms, the growth sites and rates would both be enhanced.

Influence of catalytic metal thickness

Appropriate catalyst and its thickness played an important role in the growth of silicon nano-wires. Versatile thicknesses of Ni catalyst were adopted for the issues of successful synthesis. The growth condition was at nitrogen flow rate of 10 slm and at furnace temperature of 900℃, and the time for growth was 15 min. Different thicknesses showed different morphologies which were represented in figure 4, indicating that the optimum thickness of nickel catalyst was 400A. The image of FESEM revealed that the nano-wires were straight with appropriate density which was suitable for the application of nano-devices. Since the thickness of catalysts increased, the catalysts could not form nano-particles which were necessary for nano-wire growth.

Growth model

The growth of silicon nano-wires could be cataloged into two different mechanisms: base growth model and tip growth model, respectively. The single nano-wire grown on the sample surface was shown in figure 5, where a lonely nano-wire lay down on the surface. There was a larger white spot which was a result of a strong refection of electrons at the tip of the nano-wire. Therefore, it seemed that the white spot was the catalyst metal which contributed the growth of silicon nano-wires. In order to distinguish what the component of the white spot, EDX was used to

analyze the tip and base of this nano-wire. The results of analysis were represented in figure 6, where the inset showed the statistics of what the composition elements existed in the tip and base, respectively. It was obviously that the percentage of Ni element was higher at the tip (0.9%) than that at the base (0.16%). Accordingly, the mechanism of nano-wires was ascribed to the tip growth model.

Conclusions

Silicon nano-wires were synthesized in a thermal furnace with different catalyst thicknesses, ambient flow rates and temperatures. Catalyst thickness of 400A was found to be the optimum thickness because of the straight morphologies and appropriate densities. Synthetic temperatures higher than 900℃ were also necessary due to the formation of liquid nano-particles at which the nano-wires would segregate and grow. Higher ambient flow rates supplied the nucleation sites as the heat taken away by it. Furthermore, the nano-wires synthesized by SLS mechanism were revealed to be the tip growth modle.

Acknowledgements

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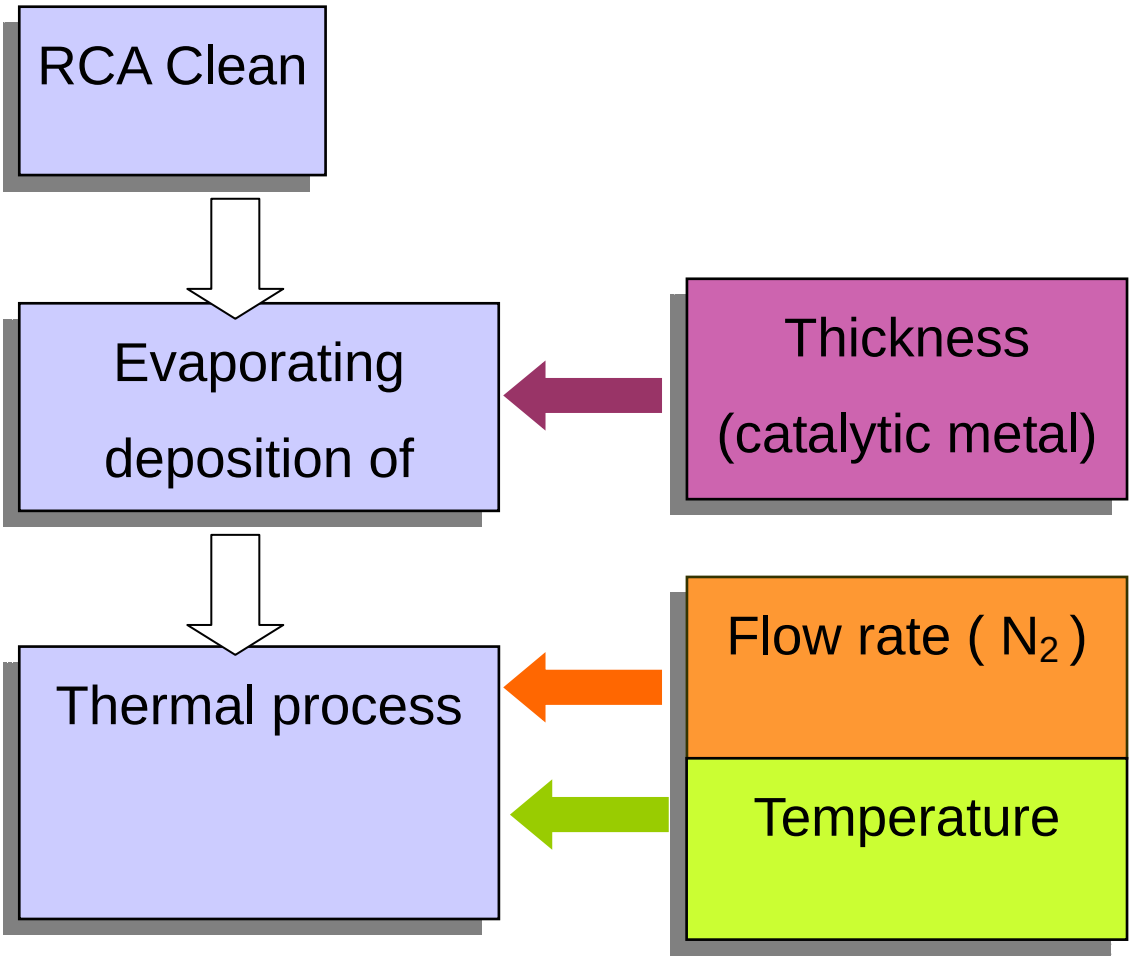

Figure 1. The flow chart of the experiment on which the synthesis of silicon nanowires were based.

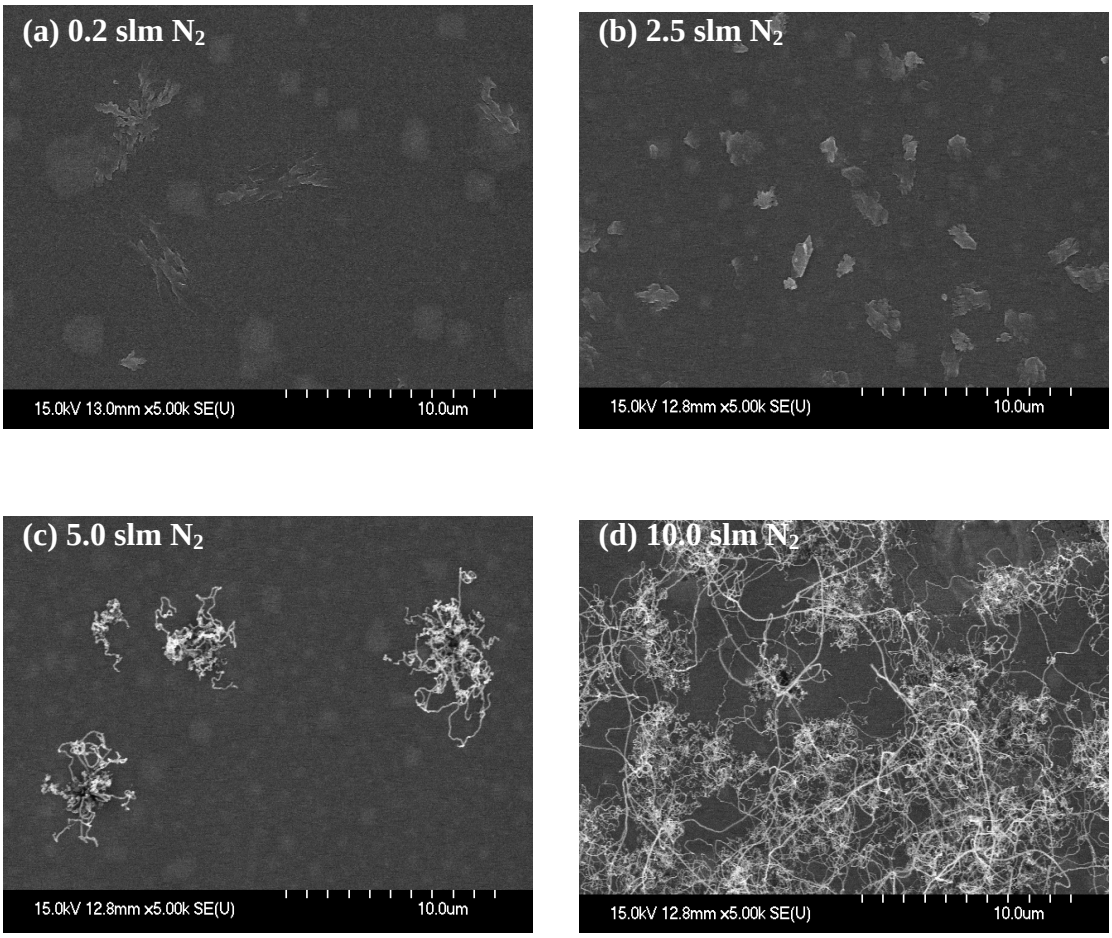

Figure 2. The FESEM images of silicon nanowires with different ambient nitrogen gas flow rates. (a) 0.2 slm, (b) 2.5 slm, (c) 5 slm, and (d)10 slm.

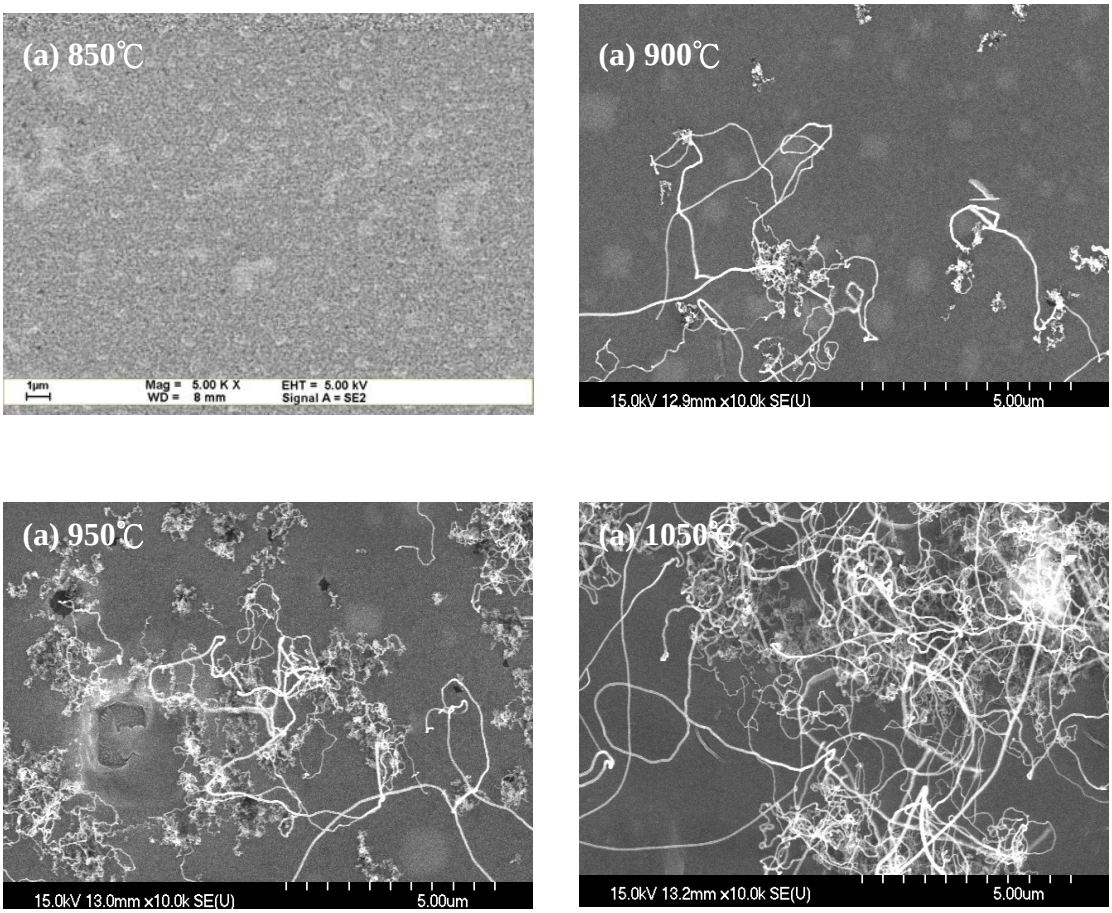

Figure 3. The FESEM images of silicon nanowires with different synthetic temperatures. (a) 850℃, (b) 900℃, (c) 950℃, and (d) 1050℃.

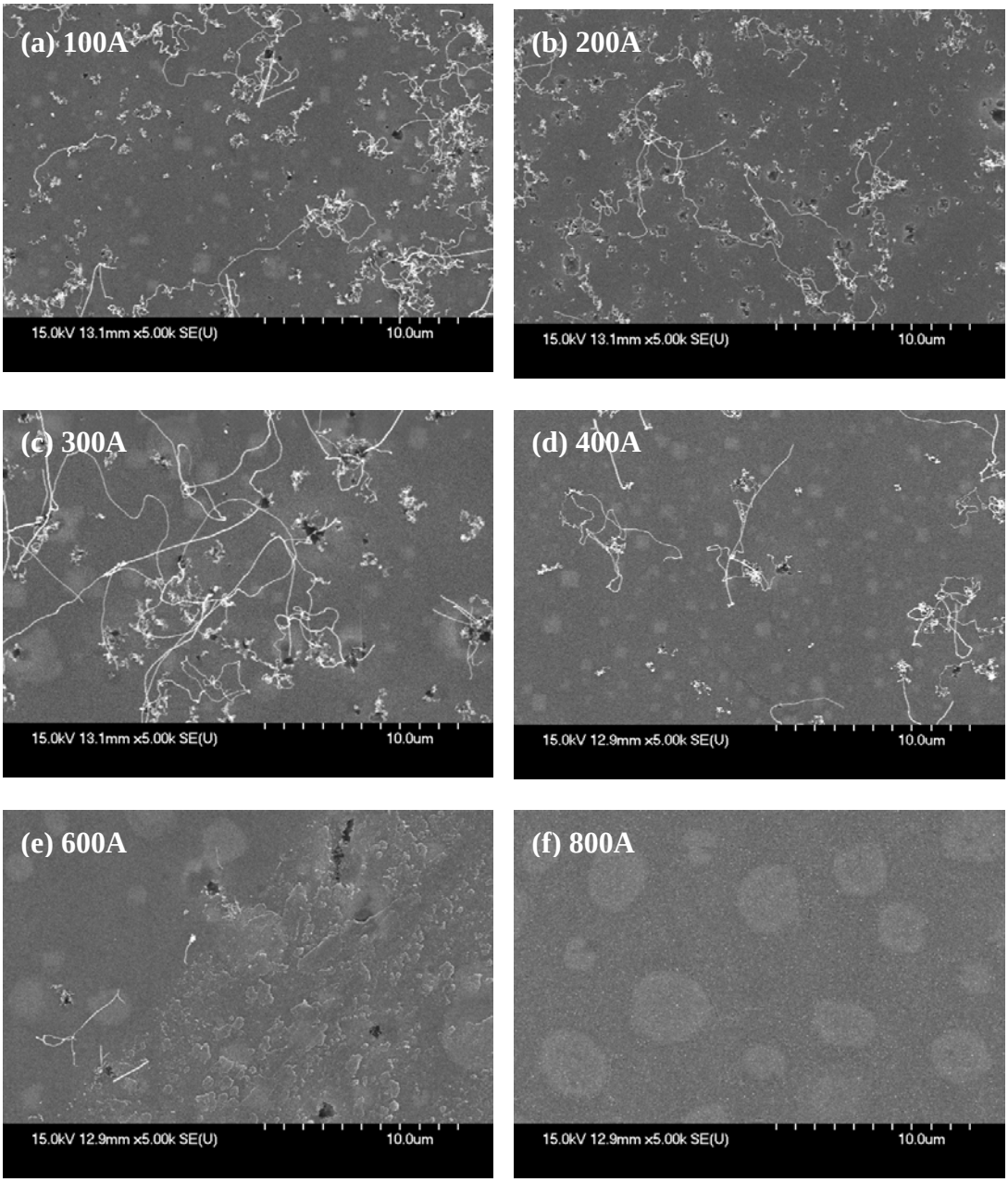

Figure 4. The FESEM images of silicon nanowires with different catalytic metal thicknesses. (a)100A, (b)200A, (c) 300A, (d) 400A, (e) 600A,and (f) 800A.

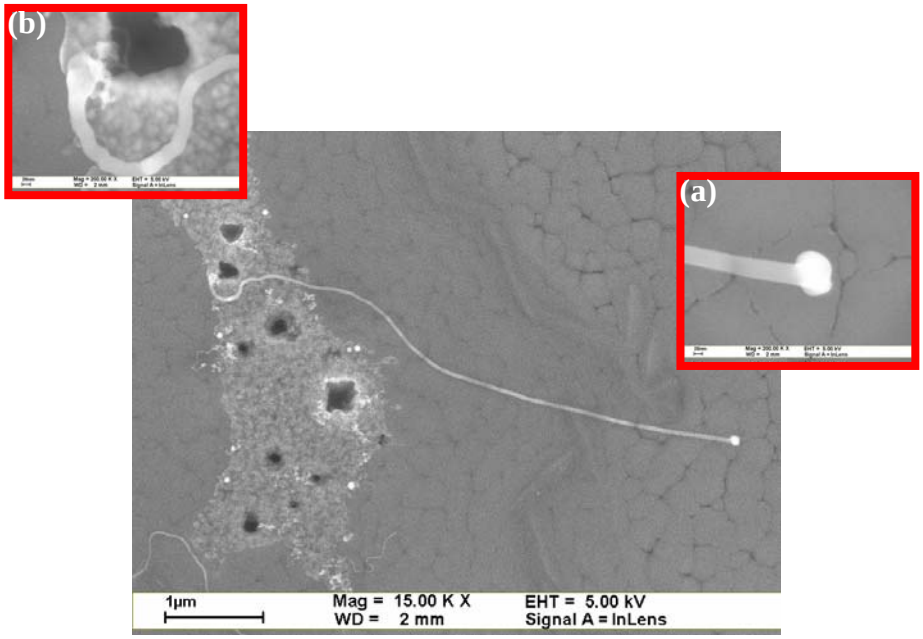

Figure 5. A single silicon nanowire lay on the surface. The insets (a) and (b) indicated the magnified images of FESEM at the tip and base, respectively.

Element	At %
N	2.52
O	4.26
Si	93.06
Ni	**0.16**

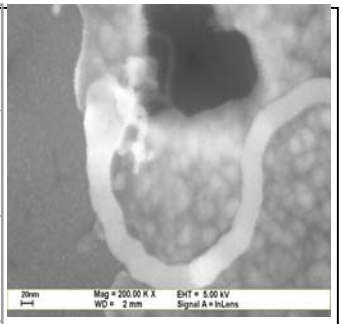

Figure 6 (a). EDX profile and element percentage statistics at the base of a single silicon nanowire.

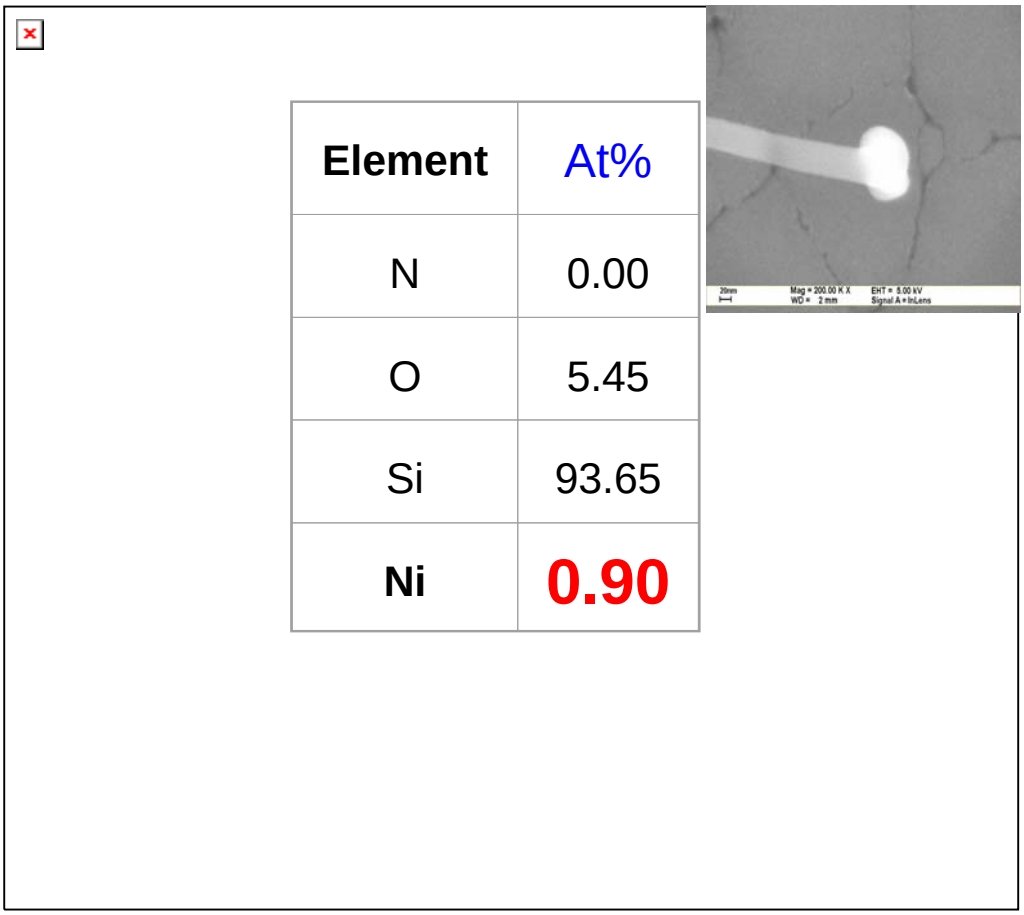

Figure 6 (b). EDX profile and element percentage statistics at the tip of a single silicon nanowire.