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子計畫六：系統單晶片電壓供應規劃與干擾消除之平面放置相關設計(1/3)

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e-Home 核心技術之研究

子計劃六

系統單晶片電壓供應規劃與干擾消除之平面放置相關設計

Simultaneous Power Supply Planning and Noise Avoidance in SoC Floorplan Design

計畫編號：NSC 93－2220－E－009－030－
執行期間：93 年 8 月 1 日至 94 年 7 月 31 日
計畫主持人：陳宏明 助理教授 國立交通大學電子工程學系
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一、中文摘要

今日的晶片製成技術已經進入深次微米環境，我們可以將整個電子系統集合在單一個晶片上。然而，如果沒有在平面設計上做好完善的電源供應規劃，我們設計的晶片將會產生熱點、電源的不足與訊號完整性的問題。在這一年計畫執行期間，我們研究在早期的平面規劃階段裡，同時考慮電源供應規劃與雜訊避免的問題。我們說明這兩個問題可以用限制最大流量的方法來闡述，並且提出一個有效率的辦法來解決。實驗結果發現只要增加些微的佈線長度，我們就可以得到一個符合電流與功率損耗規格，但幾乎沒有靜態電源雜訊的電源供應平面規劃。而且與傳統只考慮電源供應的平面規劃比較起來，在ΔI 雜訊上會有 45.7%的改善。除此之外，我們計劃使用晶片內的去耦合電容更進一步低來降低雜訊，以達到更佳的效能。不過我們需注意去耦合電容與封裝結構上的電感所產生的自然共振現象，這會使得電源震盪不穩定。
關鍵字：電源供應雜訊、平面規劃、去耦合電容。

英文摘要(Abstract)

With today’s advanced integrated circuit manufacturing technology in deep submicron (DSM) environment, we can integrate entire electronic systems on a single system on a chip. However, without careful power supply planning in layout, the design of chips will suffer from local hot spots, insufficient power supply, and signal integrity problems. In this project, we study the problem of

simultaneous power supply planning and noise avoidance as early as in the floorplanning stage. We show that the problem of simultaneous power supply planning and noise avoidance can be formulated as a constrained maximum flow problem and present an efficient yet effective heuristic to handle the problem. Experimental results are encouraging. With a slight increase of total wirelength, we achieve almost no static IR (voltage)-drop requirement violation in meeting the current and power demand requirement imposed by the circuit blocks compared with a traditional floorplanner and 45.7% of improvement on ΔI noise constraint violation compared with the approach that only considers power supply planning. Besides, we plan to use on-chip decoupling capacitor (decap) to minimize the noise and improve the circuit performance. However, the resonance of the package inductance and on-chip decoupling capacitance can result in an oscillation in the supply voltage.

Keywords : power supply noise、floorplanning、decoupling capacitor(decap)。

二、計畫的緣由與目的(Background and Objective)

1. Background

Because of deep submicron (DSM) technology, chips now contain more functions and are being driven to higher performance levels than ever before. Furthermore, reduced supply voltage in low power design nowadays tightens the noise margin. Without careful layout planning, the design will suffer from local hot spots, insufficient power supply, and signal integrity problems, among which we focus primarily on IR-drop and noise. In traditional VLSI design, as [1-3] pointed out for power supply noise analysis, the resistive IR-drop occurs mostly on the chip and the inductive noise only occurs on the package. IR-drop is voltage drop of the power and ground due to current flowing in the P/G resistive network. However, as we move into DSM regime, the inductive component of wire impedance $j\omega L$ becomes comparable to *R*. Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power distribution network. These voltage fluctuations are also called simultaneous switching noise (SSN) [4]. The noise will not only increase the signal delay but also cause false switching of logic gates. Therefore, we should try to minimize the noise across the entire chip during power supply planning in order to ensure the performance and reliability of the chip.

2. Objective

High-performance ICs require a robust power delivery network with nominal supply voltage fluctuations. We formulate the problem as a supply-demand problem for power delivery with side constraint for power supply noise requirement. In order to handle the power supply planning problem along with static IR-drop and noise constraints to be met, we need to develop reasonable and efficient strategies to deal with the constraints. First, we define a feasible power supply region to consider the IR-drop requirement. Then we introduce the construction of a special network for power supply planning based on a feasible power supply region for noise avoidance. In preserving the advantage of polynomial time max-flow algorithm, we also develop an effective algorithm to deal with the noise constraint. If the noise constraint is still not met after the power supply planning, we can further use decoupling capacitor to reduce the noise in local area [5].

三、研究方法及成果 (Research Methods and Experimental Results)

1. Problem Formulation and Proposed Method

A. Problem Formulation

Problem 1 *Given a floorplan of n blocks $b_1, \cdots, b_n$ and their minimum current requirements $d_1, \cdots, d_n$, respectively, and given a set of m power supply bumps $p_1, \cdots, p_m$ and the maximum current they can deliver $s_1, \cdots, s_m$, respectively, find a feasible solution such that each circuit block b_j obtains d_j from power supply bumps, and each power supply bump p_i delivers current s_i or less. In addition, the resistance of delivering path from power supply bumps to blocks should be bounded. Meanwhile, the power delivery assignment needs to meet the ΔI noise constraint:*

$$[\sum_h \delta(x_{ih}) L_i \frac{(\frac{dI}{dt})_h}{\sum_{k \in S_h} w_{kh} \delta(x_{kh})}] + [L_{ij} \frac{(\frac{dI}{dt})_j}{\sum_{k \in S_j} w_{kj} \delta(x_{kj})}] \leq \Delta V_j, \quad for\ each\ p_i, b_j\ s.t.\ \delta(x_{ij}) = 1$$

We refer to $x = \{ x_{ij} \}$ satisfying (1) as a flow and the corresponding value of the scalar variable v as the value of the flow. x_{ij} is the amount of current delivered from p_i to b_j, $\delta (x_{ij}) = 1$ if $x_{ij} > 1$, $\delta (x_{ij}) = 0$, otherwise. $(dI / dt)_j$ is the maximum rate of current change during transition at b_j. L_i is the parasitic inductance for p_i and L_{ij} is the effective wire inductance from p_i to the center of b_j. S_j is the set of all power supply bumps that connect to b_j, ΔV_j is the upper bound on ΔV for b_j, and $w_{ij} = d_{ij} / \sum_{k \in S_j}$, d_{ij} is the weight calculated from the distance between p_i and b_j.

B. Feasible Power Supply Region (FPSR)

We bound the resistance between a block and its power sources to reflect the IR-drop constraint. Given the current requirement and the upper bound on ΔV for a block, we can derive a region that is an expansion of the block in all four directions by a distance *r*. Such a region is referred to as the feasible power supply region (FPSR) for the block. Only the power supply bumps within the FPSR of a block can deliver power to the block. In Fig. 1, the FPSR of block *b2* is within the dashed lines, meaning four bumps *p1 ~ p4* can deliver power to block *b2* .

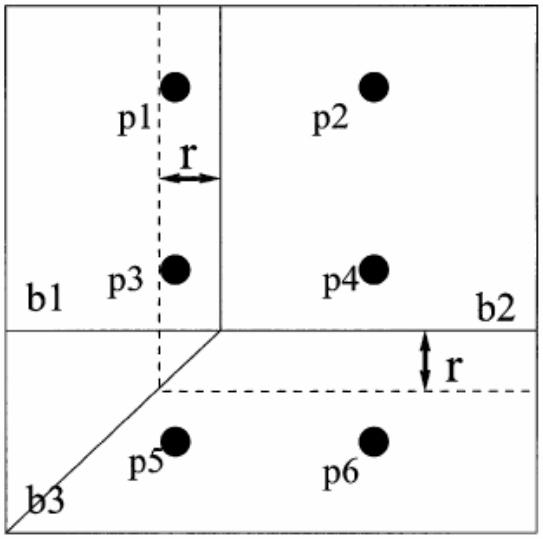

Fig. 1. Floorplan and the available power supply bumps. A circuit block can use the power supply bumps within its feasible FPSR.

C. Constrained Network Formulation

We then construct a special network graph and run a modified max-flow algorithm [6] based on the FPSR to solve the problem. The graph consists of two kinds of vertices besides the source *s* and the sink *t***:** the circuit block vertices *B = {b1,b2,…, bn}* and the power supply bump vertices *P = {p1, p2,…,pm}*. To simplify the presentation, we use the same name for a vertex and for the corresponding circuit block or power supply bump interchangeably.

The network graph *G = (V, E)* is constructed as follows. There is an edge from the source *s* to every power supply bump vertex and there is an edge from every circuit block vertex to the sink *t*. The edge capacity from the source *s* to a power supply bump vertex p_i is s_i , which is the maximum current that can be delivered by p_i. The edge capacity from a circuit block vertex b_j to the sink *t* is d_j, which is the minimum current that is required by b_j. There is an edge from p_i to b_j if p_i is inside the

FPSR of b_j. If such an edge exists, the edge capacity is set to ∞. We wish to find the maximum flow from the source *s* to the sink *t* that satisfies the edge capacities and mass balance constraints at all nodes. We can state the problem formally as follows.

Minimize ***v***

Subject to

$$\sum_{j:e_{ij}\in E} x_{ij} - \sum_{j:e_{ji}\in E} x_{ji} = \begin{cases} v, & \text{for } i = s \\ 0, & \text{for all } i \in V - \{s,t\} \\ -v, & \text{for } i = t \end{cases} \quad (1)$$

$$\left[\sum_h \delta(x_{ih}) L_i \frac{\left(\frac{dI}{dt}\right)_h}{\sum_{k\in S_h} w_{kh}\delta(x_{kh})}\right] + \left[L_{ij}\frac{\left(\frac{dI}{dt}\right)_j}{\sum_{k\in S_j} w_{kj}\delta(x_{kj})}\right] \leq \Delta V_j, \quad \text{for each } p_i, b_j \text{ such that } \delta(x_{ij}) = 1. \quad (2)$$

Fig. 2 illustrates the construction of the network graph for the floorplan example in Fig. 1. Block b_2 can get power supply bumps *p1~p4* to deliver power, as shown in Fig. 1.

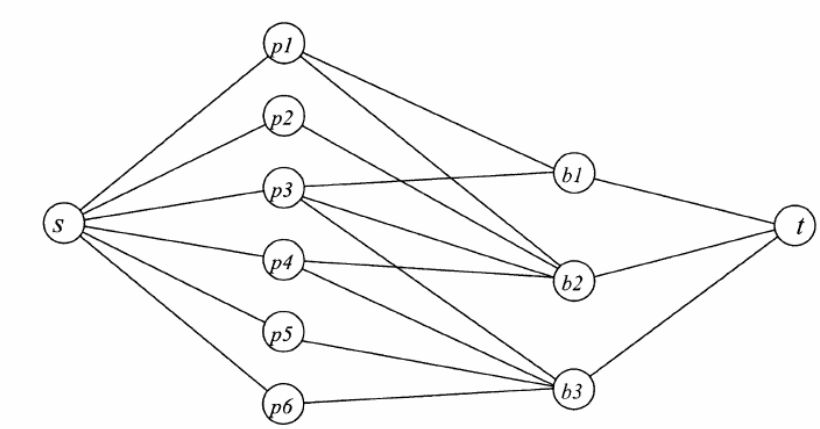

Fig. 2. Network graph captures the current and power demand of the circuit blocks, and the current and power that power supply bumps can provide in Fig. 1

The feasible power supply regions of block b_1 and b_3 are not shown in Fig. 1, where block b_1 can get power supply bumps *p1* and *p2* to deliver power, and block b_3 can get power supply bumps *p3~p6* to deliver power. Note that in Fig. 2 some power supply bump vertices can be connected to two circuit block vertices or `more because a power supply bump can supply power to several circuit blocks at the same time, as long as the demanded current and power never exceeds the maximum amount that can be delivered by the power supply bump.

Any flow from the source to the sink in the network assigns current delivering from a power supply bump to a circuit block. If there is a feasible power supply planning solution satisfying all power requirements of the circuit blocks, the total flow on every edge from the circuit block vertex to the sink should equal to the edge capacity. It can be shown that our network flow algorithm optimally solves the power supply planning problem if we do not consider the other constraint we have introduced. We have the following theorem.

Theorem: A maximum flow in the network graph corresponds to a power supply planning solution which maximizes the amount of current and power delivered from the power supply bumps to the circuit blocks. A feasible solution with respect to FPSRs for all blocks exists if and only if all edges from the circuit block vertices to the sink are saturated.

As can be seen in the problem definition, the side constraints are nonlinear, so it may be treated as an NP-hard or an approximately NP-hard problem. We cannot use min-cost max-flow/min-cut or maximum bipartite matching algorithms to optimally solve this problem. In the following section, we introduce an efficient yet effective algorithm to minimize the violations of the noise constraint and still obtain maximum flow.

D. Priority_Augmenting_Path Algorithm

Here we describe a priority-based heuristic to deal with the power supply noise constraint in the max-flow algorithm. In the Ford–Fulkerson method, we try to find any augmenting path to increase the flow. However, randomly picking a feasible augmenting path may cause serious violations for the noise constraint in power delivery planning. Fig. 3 shows the constraint violation example when not carefully augmenting the flow. Due to this observation, we implement an efficient algorithm to decide the order of finding augmenting paths based on the priority assigned on the edges between power supply bump vertices and block vertices in our network.

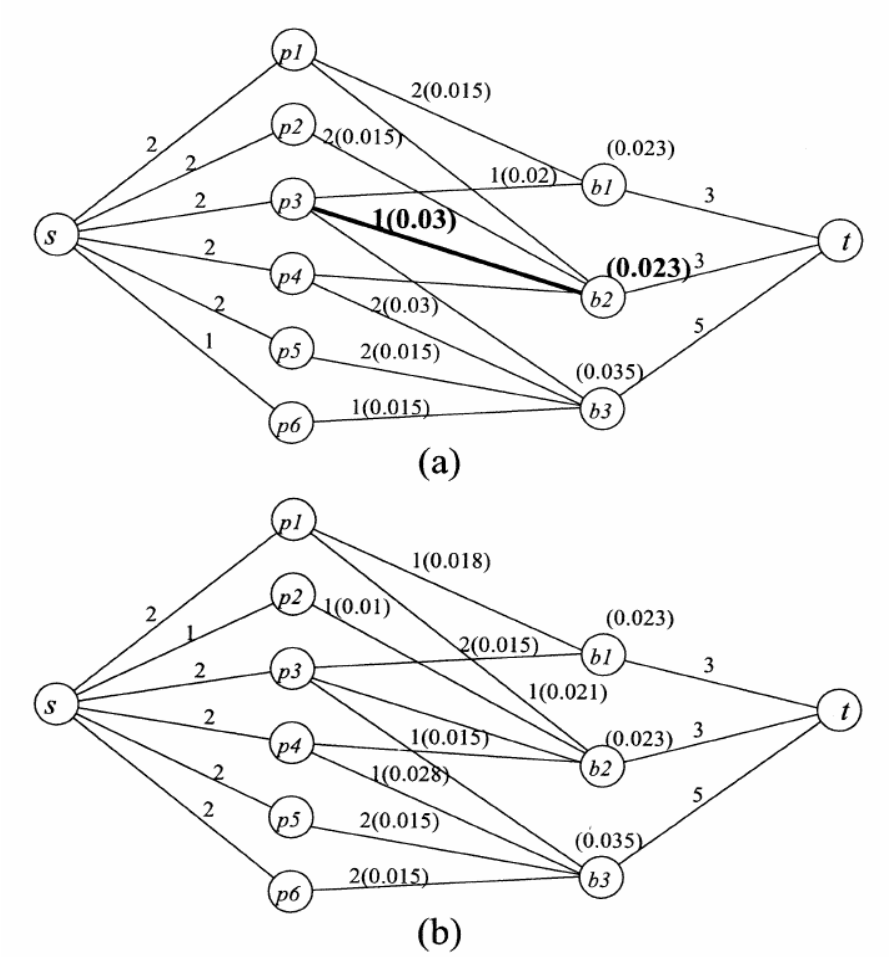

Fig. 3. Numeric examples include two max-flow solutions of the network graph from Fig. 2. Those numbers are calculated from the technology file, given IP parameters, and the estimation models used earlier. The darker numbers and the edge show that there is a ΔI noise constraint violation. The number on the edge is the amount of flow on that edge. The number inside the parentheses on the edges between power supply bumps and blocks is the amount of inductive induced voltage drop on that edge. The number inside the parentheses above the block node is the upper bound on _V for the block. (a) The solution with randomly choosing augumenting path. For example, *e*(*p1*; *b1*) has 0.015 V for inductive induced voltage drop, which does not exceed ΔV = 0.023 V. However, for *e*(*p3*; *b2*), it has 0.03 V, which exceeds ΔV = 0.023 V, indicating a violation. (b) The solution using the algorithm in Section C. There is no ΔI noise constraint violation.

The main point is that we want to choose a path or edge with either low inductive induced voltage drop or large ΔV for the block to augument the flow. The reason for low inductive induced voltage drop is obvious:We want to deliver power via low voltage drop to blocks; the reason for large voltage tolerance of blocks on inductive induced voltage is that delivering power to small ΔV blocks is harder due to the cleaner power supply requirement. We use the following implementation to realize these two rationales.

We assign the cost first to reflect the rough inductive induced voltage drop without the effect of

sharing the power demand of the block. The cost for edge e_{ij} from p_i to b_j is $c_{ij} = (dI/dt)_j * (L_i + L_{ij})$.We then assign priority values for the edges between p_i and b_j as follows. Note that for the forward and backward direction of the edges, we should assign different priority values so that the preferred augmenting path can be found. For the forward direction, the priority value $P_{ij} = (c_{ij} / N_j) + (1/\Delta V_j)$; for the backward direction, the priority value $Q_{ji} = (N_j / c_{ij}) + \Delta V_j$, where N_j is the current number of power supply bumps which deliver power to block b_j. N_j needs to be updated whenever we obtain an augmenting path and augment the flow since the intermediate flow solution has been modified. During the process of finding an augmenting path, we can use the priority values to select a preferred path. In this way, finding the augmenting path which minimizes the violations of the noise constraint can be accomplished.We have the following algorithm.

```
Algorithm Priority_Augmenting_Path
begin
  x := 0;
  while G(x) contains a directed path from s to
  t do
    Identify an augmenting path U from s to t
      based on priority of the edge from some
      power supply bump to some block;
    ν := min{r_ij : e_ij ∈ U, i, j ∈ V};
    Augment ν units of flow along U;
    Update G(x) and N_k, k ∈ B;
  end
end
```

In the algorithm, *x* is the flow vector, *G(x)* is the residual network, r_{ij} is the residual capacity for edge e_{ij}, and *v* is the residual capacity of the augmenting path *U* [6]. We use the Edmonds–Karp algorithm to implement pure max-flow problem, where the runtime is $O(nm^2)$, and where $n = |V|$ and $m = |E|$ [7]. To be more specific, the number of iterations is at most $O(nm)$ and each iteration of the Ford–Fulkerson method can be implemented in $O(m)$ time using breadth-first search (BFS).We can use the Fibonacci heap to implement priority queue and obtain the logarithmic runtime in operations. In addition, the dequeue and enqueue operations in BFS both take $O(1)$ time originally, but in our proposed algorithm, they take $O(\lg n)$ time. The update of the number of power supply bumps which deliver power to blocks can be done in $O(nm)$ since they are only updated when we obtain augmenting paths. The runtime of the priority augmenting path algorithm hence is $O(nm(n \lg n + m))$. We have the following corollary.

Corollary: The priority augmenting path algorithm with prioritized breadth-first search solves

the max-flow problem and heuristically minimizes side constraint violations in $O(n \lg n + m)$ time. Hence, the modified Edmonds–Karp algorithm runs in $O(nm(n \lg n + m))$ time.

E. Floorplanning with Power Supply Planning and Noise Avoidance

Our floorplanning algorithm with simultaneous power supply planning and noise avoidance is based on the Wong-Liu floorplanning algorithm [9]. In this paper, in addition to optimizing total wirelength and chip area, we propose to perform simultaneous power delivery planning and power supply noise avoidance design with respect to the current floorplan being considered and in result to obtain a much better floorplan with less power supply noise constraint violations.

The cost function used to evaluate a floorplan in [9] is $A + \lambda W$, where A is the total area of the packing, W is the half-perimeter estimation of the interconnect cost, and λ is a constant which controls the relative importance of these two terms. In this paper, we use the cost function $\alpha A + \beta W + \gamma P$ for floorplanning with simultaneous power supply planning and noise avoidance, where A can be either total area of the packing or fixed die penalty if using fixed die implementation, which is zero if the area of floorplan is within the fixed die and is the difference between the area of current floorplan and fixed die area otherwise, W is total wirelength estimation, and P is the power supply cost penalty, which is positive if current floorplan cannot find max-flow solution and/or obtain the violations of power supply noise constraint and is zero if there is a max-fow solution and no constraint violations for current floorplan. The coefficients are constants that control the relative importance of the three terms.

2. Experimental Results

We have tested our approach on some Microelectronics Center of North Carolina (MCNC) building block benchmarks. All experiments were carried out on a 650-MHz+ Pentium III processor. The minimum amount required by a circuit block and the maximum rate of current change during transition at a circuit block are roughly proportional to its area. The power supply bumps are in a regular array structure and the maximum amounts of power they can deliver are all the same. (In fact, our approach can be applied to other equivalent structures.) The values of parasitic and wire inductance and other technology parameters are from ITRS'97 roadmap [8], 0.18 m. In order to show the effectiveness of our approach, we implement three algorithms: 1) the traditional approach without any power supply planning consideration [9], 2) the approach with rough IR-drop

requirement consideration in power supply planning [10], and 3) the feature approach in simultaneous power supply planning and noise avoidance.

TABLE I
COMPARISON OF OUR APPROACH WITH [15] AND [23] ON MCNC BENCHMARKS. THE WIRELENGTH DATA ARE DESCRIBED IN SECTION V

		Traditional Floorplanner [15]		Floorplanner with Power Supply Planning [23]			Simultaneous PSP-NA		
Data	Block#	IR-drop Vio(%)	Noise Vio(%)	IR-drop Vio(%)	Noise Vio(%)	Time (hr)	IR-drop Vio(%)	Noise Vio(%)	Time (hr)
apte	9	0	54	0	54.6	0.2	0	3.9	0.24
xerox	10	0	61	0	61.4	0.6	0	9.1	0.44
hp	11	27.3	65	0	60.4	0.11	0	7.3	0.1
ami33	33	31.3	48	3.1	45.1	1.3	3.1	9.9	1.7
ami49	49	4.1	62	0	44.6	3.6	0	7.6	3.74
Average		12.54	58	0.62	53.2		0.62	7.5	

Table I shows the comparison between the floorplans obtained from our approach, those obtained from a traditional floorplanner without any power supply planning consideration, and those obtained from the approach with supply-demand-only power supply planning consideration during the annealing process. All the floorplans obtained are within a fixed die area with 7% dead space. We use the IR-drop requirement violation and noise constraint violation (in percentage) to reflect the effectiveness of our approach. Since we use FPSR to bound the power delivering path's resistance to prevent static IR-drop violation, we thus use a percentage, which is the number of blocks that obtain insufficient current and power due to IR-drop normalized by total number of blocks, to show the IR-drop requirement violation. The noise constraint violation percentage is the number of power supply bump-block edge constraint violations normalized by the number of total power supply bump-block edges in the network. From Fig. 3, we can see that if there is no violating edge in the network graph, the noise constraint violation percentage is 0%. The floorplans obtained from our approach have far fewer IR-drop violations, over which is 50% improvement on the noise constraint violations, and less than 5% of the total wirelength increase on average compared with the floorplanner with power supply planning.

四、結論與討論(Conclusion and Discussion)

We have presented an approach to simultaneously solving power supply planning and noise avoidance in floorplan design and it has been published in [11]. The efficient yet effective priority-based heuristic we have introduced ensures the polynomial time max-flow algorithm for this difficult problem and experimental results are encouraging. With a slight increase of total wirelength,

we can obtain a big improvement on IR-drop and noise constraint violations in the floorplanning stage.

We have formulated the problem which we treat two constraints, IR-drop and Ldi/dt, independently and separately. In fact, since the drop in the supply network is the sum of the static IR-drop and the inductive induced drop, ideally these two should not be treated separately. We consider them separately for simplified and conservative modelings. Typically an IP block specifies the minimum voltage required to meet specifications, we consider the worst case scenario that we bound IR-drop and let it be a fixed value. Thus the upper bounds on ΔV for blocks become the difference between the specification and IR-drop bound. The reason we consider the constraints in separate worst case bounds is because the circuit should operate correctly even under the worst case scenarios [5]. However we can actually combine these two constraints using same algorithm. We can simply change ΔV_j to be dynamically updated when we take the difference between static IR-drop and maximum permitted drop for each power supply bump-block edge. This alternative approach, nevertheless, cannot use pre-computed values for ΔV_j and it needs small amount of additional spaces.

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六、未來研究方向(Future Work)

We plan to find out approaches in floorplan optimization to further avoiding power supply noise by decap insertion. Also possible approach to lowering power dissipation and minimizing power supply noise by simultaneously inserting sleep transistors and decaps will be explored.