行政院國家科學委員會專題研究計畫　成果報告

奈米級先進絕緣層上覆矽(SOI)元件研製與分析

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計畫主持人：林鴻志

計畫參與人員：呂嘉裕、謝雨霖、趙志誠、張伊鋒、林賢達

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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
□期中進度報告

奈米級先進絕緣層上覆矽(SOI)元件研製與分析

Fabrication and characterization of advanced nano-scale SOI devices

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計畫主持人：**林鴻志**
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中 華 民 國 2005 年 10 月 31 日

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I. 摘要

本計畫主要是探討具有鉑金屬矽化與雜質隔離技術的蕭特基 SOI 元件之特性表現。因為其具有 tri-gate 的結構，元件整體表現會比傳統蕭特基元件來的好，而且因為雜質隔離可有效的降低蕭特基能障，因此不再需要電場引致汲極的技術來降低漏電流。元件導通電流對於具有雜質隔離技術的蕭特基元件，會比傳統使用電場引致汲極方法增加五倍之多，當能有效運用雜質隔離技術於砷和磷離子時，可成功的製作出高效能的蕭特機 SOI 元件，而且運用雜質隔離技術對於製作奈米級互補式金氧半場效電晶體是相當具發展潛力。

Abstract

SB SOI-PMOSFET formed by Pt salicide and impurity segregation has been demonstrated. Because of tri-gate structure, the overall performance is excellent than conventional SB device. By adjusting SB height through impurity segregation, excellent device performance is achieved and FID structure is not necessary to reduce leakage current. The driving current of the SB device with impurity segregation is five times larger than that of the SB device with FID. Since the impurity segregation technique is also applicable to arsenic or phosphorous dopants, high performance SB CMOS can be realized. Schottky junction with impurity segregation thus appears to be a promising technique for future nano-scale MOSFETs.

Keywords: *SOI, Schottky barrier, field-induced drain (FID), On/Off current ratio.*

II. Introduction

When entering deep nano-scale region, how to control short channel effect is extremely important. The ultra-thin-body [1] and the double-gate [2] MOSFET are more scalable than the conventional bulk-Si structure, and show good device characteristics due to reduce junction leakage current by buried oxide and ultra-thin Si channel. The quasi-planar FinFET offers the superior scalability of the double gate devices together with a process flow and layout similar to the conventional MOSFET [3]-[5].

SB MOSFET also has much attention as a candidate to suppress short channel effect. However, a serious problem has been pointed out, that lower driving current due to a large schottky barrier height at the source region. Several metal silicide materials have been investigated to solve this problem, such as $ErSi_2$ for NMOSFET and PtSi for PMOSFET, respectively [6]. The other reason for the lower current is that there appears a gap between the source side Schottky contact and the channel which

causes a large series resistance. Recently, the impurity segregation technique was used to adjust Ni fully silicided gate work-function [7]. In this study, we propose and demonstrate a novel approach for Schottky barrier height engineering with PtSi process using the impurity segregation technique on SOI wafer.

III. Device Fabrication

SOI wafer with 190nm-thick Si film and 330nm-thick buried oxide were used as the starting substrate. Thermal oxidation and wet etching were to reduce Si film thickness to 50nm. Then, patterned by MESA isolation, a 10nm-thick sacrificial oxide was grown and wet etched to remove the damage created by dry-etch. Followed by 2.5nm oxynitride gate dielectric and 150nm in-suit doped n+ poly-Si. A 20nm TEOS oxide spacer was deposited and etched. BF_2 was implanted with the dose of 1×15 cm^{-2} and energy of 10 keV. RTA(850 ℃, 20s) was performed to active dopants and suppress implant damage. 50nm Pt was deposited and 450 °C furnace anneal to form PtSi. Un-reacted Pt was then removed in a diluted aqua regia etch. Next, 25nm-thick PETEOS passivation layer were deposited, and followed by contact holes and aluminum pads. The device process flow and cross section are in Fig. 1 and Fig. 2, respectively.

IV. Results and Discussion

Before the silicidation, BF_2 is implanted and activated to form a shallow junction. Next, silicided is to consume the doping region. Boron is piled-up at the silicide/Si interface due to the impurity redistribution. The piled-up profile can be steeper with higher peak concentration than the original dopant profile. Figures 3 and 4 show the subthreshold characteristics and output characteristics of the SOI device using impurity segregation with L = 0.14 μm and Si fin width = 0.06 μm. The driving current is 225 μA/μm at Vg = -2.0 V, Vd = -1.5V. On/Off current ratio reach to 10^9 and DIBL is 60 mV/V. Note that the high threshold voltage in these devices is primarily due to the use of n^+ poly-Si gate material used in our lot for simplicity, and could be lowered when gate electrodes with suitable gate materials, such as p^+-poly and metal gate, are used.

Figure 5 shows the relationship between the subthreshold swing (SS) and the fin width. SS has a dependence of fin width and the smaller fin width has the smaller SS. This conforms that FinFET has superior ability to reduce short channel effect when fin width is smaller or equal to 0.7 times channel length. The subthreshold swing of the new SB PMOSFET is 73.5 mV/dec. Short channel effect would be suppressed by using tri-gate structure. The overall device performance is excellent than the early SB device.

The transconductiance of the new SB device is higher than the conventional SB device with field induced drain (FID), as shown in Fig. 6. Conventional SB MOSFET has a large off state GIDL-like leakage current due to its ambipolar characteristics. In our previous work, use of FID structure could effectively reduce this leakage and improve device performance [8]. Nevertheless, FID used extra sub-gate which

needs additional power line with high applied voltage, making it not practical for the integrated circuit manufacturing. Figures 7 and 8 are the subthreshold and output characteristics of the SB device with impurity segregation and FID.

According to above discussion, characteristics of the device with impurity segregation are better than that with FID. The driving current of the SB with impurity segregation is five times larger than that of conventional SB device, and easier to apply using modern technology.

V. References

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- Thinning SIMOX SOI wafer to 50 nm by oxidation
- Patterning and etching the Si fin to 60 nm and sacrificial oxide to reduce damage
- 2.5 nm oxynitride gate dielectride and 150 nm poly-gate deposited and pattern
- 20 nm LPTEOS spacer deposited and pattern
- BF_2 implantation and 850 ℃, 20s RTA annealing
- Deposited 50 nm Pt by E-gun and PtSi formed by 450 ℃ furnace anneal and removed unreacted Pt
- Passivation oxide, contact hole, and metal pad were sequential finished

Fig. 1 The process flow of the SB MOSFET with impurity sefreaftion.

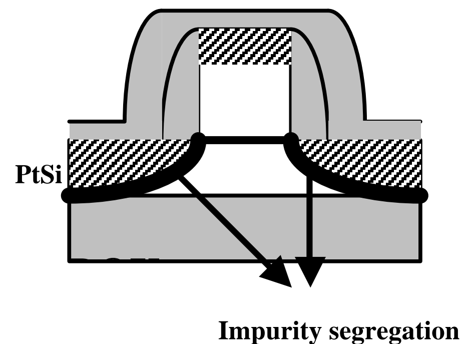

Fig.2 The cross-section of SB SOI PMOSFET with PtSi source/drain. The dopant is segregating at the PtSi/Si interface.

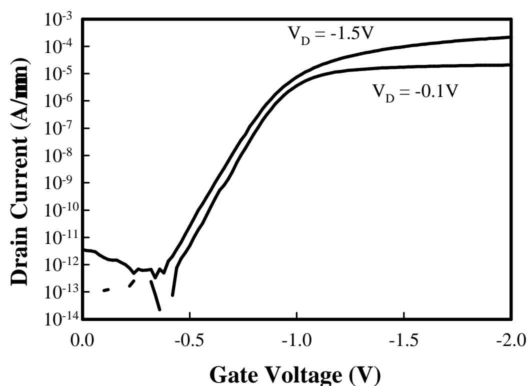

Fig. 3 Drain current versus gate voltage, which gate length was equal to 0.14 μm with Si fin width equal to 0.06 μm.

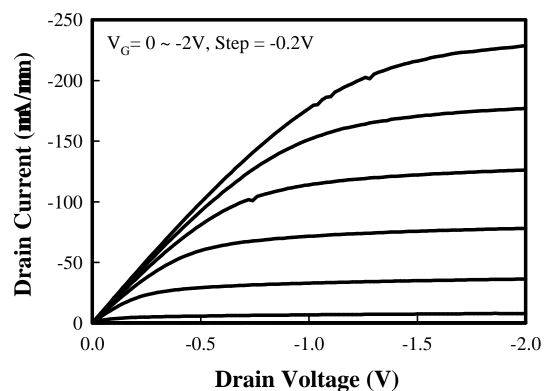

Fig. 4 Drain current versus drain voltage, which gate length was equal to 0.14 μm with Si fin width equal to 0.06 μm.

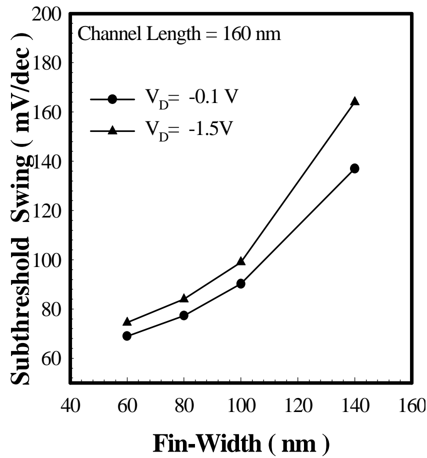

Fig. 5 The Subthreshold Swing of the new SB MOSFET with different fin width.

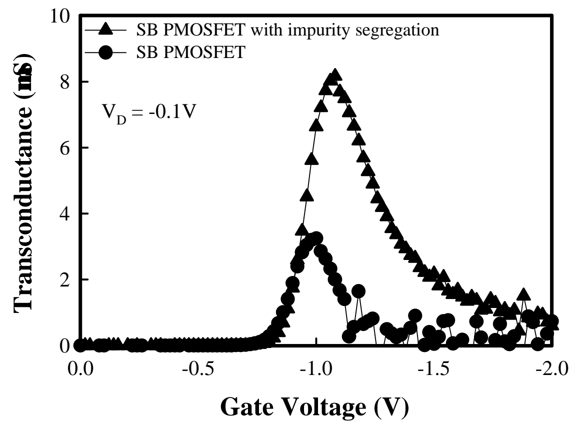

Fig. 6 The transconductance curve of the conventional SB PMOSFET and SB with impurity segregation.

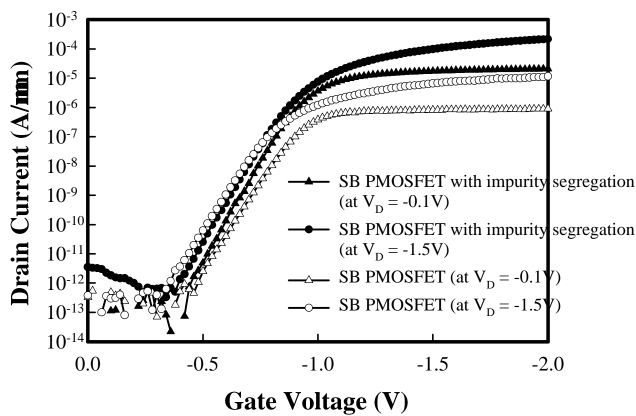

Fig. 7 The subthreshold characteristics of the conventional SB MOSFET and SB with impurity segregation.

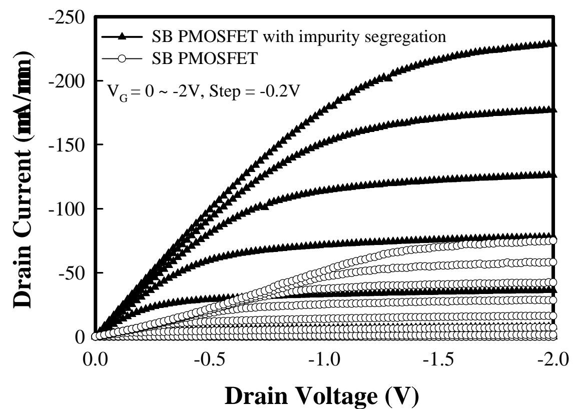

Fig. 8 The output characteristics of the conventional SB MOSFET and SB with impurity segregation.