行政院國家科學委員會專題研究計畫　成果報告

多晶薄膜電晶體通道層缺陷分布分析與多晶鍺薄膜電晶體之研製

計畫類別：個別型計畫
計畫編號：NSC93-2215-E-009-079-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
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計畫主持人：林鴻志

計畫參與人員：葉冠麟、李明賢、蘇俊榮、房新原、蘇育正

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中　華　民　國 94 年 11 月 7 日

行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
□期中進度報告

多晶薄膜電晶體通道層缺陷分布分析與多晶鍺薄膜電晶體之研製

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成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

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中　華　民　國 2005 年 10 月 31 日

中文摘要：

在本報告中，我們提出並成功演示一種先進方式，能在萃取薄膜電晶體元件通道區的全能障區缺陷密度。在這種方式中，我們將場效電導法應用在一具有場引發源/汲極之蕭特基複晶矽膜薄電晶體。僅需要單一個電晶體和兩條在室溫之下的次臨界電流-電壓量測即可萃取出全能障區缺陷密度。不同製程處理的影響可以用這個方法清楚地鑑別出來。

我們也觀察了電性量測和結構參數對於萃取結果的影響，用以得到最佳的測試條件。我們的研究顯示通道中的寄生電阻會造成尾態密度的過度高估。精準的缺陷密度可以藉由足夠高的汲極電壓，足夠高的副閘極電壓，和夠短的場引發源/汲極長度。

關鍵字：

複晶矽，缺陷密度，場引發汲極，蕭特基複晶矽薄膜電晶體，全能障區缺陷密度

英文摘要：

In this work, we have proposed and successfully demonstrated a novel approach to obtain the full band-gap DOS in the channel of TFT devices. In this approach, the field-effect conductance method is performed on an Schottky barrier (SB) poly-Si TFT with electrical source/drain extensions induced by a field-plate. Only one single device and two simple subthreshold I-V measurements at room temperature are needed for full band-gap DOS extraction. Impacts of different process treatments are clearly resolved using this methodology.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the parasitic resistance presenting in the channel would result in an overestimation of tail state density. Accurate DOS extraction can be obtained by employing sufficiently high drain and sub-gate biases and short electrical source/drain extensions.

Keywords:

poly-Si, density of states, field induced drain, Schottky Barrier TFT, full band-gap DOS

Introduction

Poly-Si TFTs have been investigated extensively due to their applications in large-area electronics like flat-panel displays. The operation of poly-Si TFTs is more complicated compared with their single-crystal counterpart due to the existence of grain boundaries in the channel, since the defects at and inside the grain boundaries may increase the off-state leakage, retard the device turn-on, and impede the carrier transport [1]. Accurate modeling of poly-Si TFT behavior is thus indispensable for simulation and design of poly-Si TFT circuits. This requires precise determination of the effective density-of-states (DOS) distribution within the poly-Si band gap. Previously, field-effect conductance (FEC) method [2-4] which characterizes the subthreshold conductance of devices has been employed to extract DOS. Fig. 1 shows the flow chart of FEC analysis. Detailed theoretical background of FEC could be found in [2] and [3]. Briefly, three major steps are involved: (a) determination of flat-band voltage, VFB, (b) determination of relationship between VG and surface potential, ? s, and (c) calculation of DOS as a function of E-EF within the gap. In step (a), VFB can be determined as the VG when the term T•[d(logG)/dVG] is independent of temperature. (T is temperature, G is ID/VD) [5]. In step (b), either the "incremental method" or the "temperature method" can be adopted[4] . To obtain full band-gap DOS, at least one n-channel device and one p-channel device are needed for characterization. Besides, I-V measurements need to be performed at various temperatures, making the procedure very tedious and time-consuming. In this work, we present a novel methodology to address this issue. In this scheme, all we need for full band-gap DOS extraction are only one device and two I-V measurements performed at room temperature. The whole process is thus greatly simplified and shortened.

Structure of the Test Device

The characterization is performed on a Schottky barrier (SB) TFT which features metallic (CoSi) source/drain and a sub-gate lying over the passivation oxide [6, 7], as shown in Fig. 2. During operation, electrical source/drain extensions are induced in the channel offset regions underneath the gate sidewall spacers by applying a high voltage on the sub-gate (or the field-plate). Depending on the polarity of sub-gate bias, the device could be set for either n-or p-channel operation. The formation of electrical junctions could also dramatically reduce the off-state leakage [7], which is essential for the analysis. To reduce the impact of series resistance on the analysis, self-aligned sidewall spacers were used to define the channel offset regions. By exploiting the ambipolar characteristics of Schottky-barrier (SB) TFTs, full band-gap DOS can be obtained on a single device. Detailed device fabrication and operation could be found in our previous reports [6, 7].

Experimental Results

A. Determination of VFB by temperature method

Multiple ID-VG measurements were performed at various temperatures to

determine VFB. In this work we found that the FB extracted from n-channel operation coincides well with that of p-channel operation with the same device. An example is shown in Fig.3 in which T[*d*(logG)/*d*VG] is expressed as a function of 1000/T. In the figures, the results for both p- and n-channel operations indicate that VFB is around –2.1 V at which T[*d*(logG)/*d*VG] is almost independent of temperature. This consistency between the two operation modes is expected and confirms the validity of this method.

B. DOS extraction

Next, we used both the "incremental method" and the "temperature method" to extract DOS. Ambipolar subthreshold I-V characteristics measured at various temperatures are show in Fig. 4. For the "temperature method", Arrehenius plots of *d*G/*d*VG and the corresponding EA as a function of VG are shown in Fig. 5 and Fig. 6, respectively. Good agreement in the extracted DOS between the two methods is obtained, as shown in Fig. 7. We have also performed the incremental method" at room temperature and 55 °C to check if ambient temperature will cause any disparity on the results. As can be seen in Fig. 8, no significant difference is observed between the two characterizations.

C. Effects of process treatments

It's well known that the DOS of poly-Si TFT is closely related to the channel preparation methods and the process conditions. In this work the new DOS characterization scheme was also employed to study the impact of different process treatments on the device characteristics. Fig. 9 illustrates the effect of plasma hydrogenation performed in an NH_3 plasma at 300 °C for one hour. As can be seen in the figure that such plasma treatment is useful in reducing the DOS, especially for those located near the mid-gap level.

Fig.10 compares the DOS characteristics of devices with channel prepared by three different schemes, namely, as-deposited poly-Si, solid-phase crystallization (SPC), and excimer laser annealing (ELA). Among those splits the ELA sample shows lowest DOS value. Figs. 11 (a) and (b) show the TEM pictures for SPC and ELA samples, respectively. The larger grain size observed in the ELA sample explains the results shown in Fig.10. The above results indicate that the proposed methodology is useful in resolving the effects of different process treatments on the material and device characteristics.

D. A new way for determining VFB

Finally, an important finding is discovered during the course of this study. Specifically, we observed that the extracted FB using the tedious conventional temperature scheme coincides well with the VG value at the intersection point of the bi-channel I-V curves measured at room temperature. An example can be found by comparing Fig. 3 and Fig. 4. To further validate the universality of this observation, different groups of samples were characterized and the results are summarized in Fig. 12. It can be seen that good agreements are obtained in all cases. This important finding

thus provides a new and much simpler methodology for the determination of VFB.

E. Effect of Applied Drain Bias

Here we address the effect of drain bias on the measurement results. The measurements were carried out for n-channel operation by sweeping gate voltages from –3 to +6V, and for p-channel operation by sweeping gate voltages from –1 to –10 V, with drain voltages $|V_{DS}|$= 0.1V or 5V, and sub-gate voltage |Vsub|=50V. Fig. 13 shows the characteristics of the I_D-V_G for the FID SB-TFT with $CoSi_2$ S/D material. The channel film is SPC poly-Si film. As can be seen in the figure, the on-current in n-channel operation is more sensitive to V_{DS} than p-channel operation, owing to the higher barrier height of electrons than holes at the $CoSi_2$/Si contact. The extracted DOS results are shown in Fig. 14. It is observed that the DOS remains unaffected in the mid-gap regime, but increases significantly near the band edge when $|V_{DS}|$ is set at 0.1V, especially for the conduction band edge. It was shown previously that the increase in $|V_{DS}|$ could decrease the source-side carrier tunneling distance [6-8], and thus the parasitic resistance. As the Fermi level moves toward the band edge, the operation is near threshold and becomes more sensitive to the contact resistance. As a result, the DOS is overestimated when $|V_{DS}|$ is not sufficiently high.

F. Effects of the channel length

Fig. 15~18 shows the extracted DOS for four devices with self-aligned spacer and channel length ranging from 0.8 to 5 μm. The on-current measured at $|V_{DS}|$ = 0.1 V as a function of channel length for these devices is shown in Fig.19. The on current becomes larger as the channel length becomes shorter due to reduced channel resistance. However, the n-mode current is almost independent of channel length when channel length is lager than 1 μm, indicating the significance of contact resistance due to larger electron barrier height. In these measurements, the mid-gap DOS is almost the same (about 1.2×10^{18} $eV^{-1}cm^{-3}$), while the tail DOS is strongly dependent of the applied bias conditions. Fig. 20 (a) & (b) compare the DOS results among devices with different channel length and $|V_{DS}|$ of 5 V. It can be seen that reasonable agreement is achieved among these devices, indicating that $|V_{DS}|$ of 5 V is sufficient large so the effects of parasitic resistance is insignificant.

G. Effects of drain-side extension length

Fig. 21 (a) shows the ambipolar transfer characteristics of device with self-aligned and non-self-aligned (X_D = 3 μm) FID length under $|V_{DS}|$ of 0.1V. The extracted DOS results are shown in Fig. 21 (b). It can be seen that the on-state current is significantly lower for device with X_D of 3μm. This is apparently due to the larger parasitic resistance in the FID region and thus leads to an overestimation of tail DOS, as shown in Fig. 21 (b). Such disparity can, again, be removed by increasing the $|V_{DS}|$ to 5 V, as shown in Fig. 22.

Discussion and Conclusion

Using the new methodology, the overall DOS extraction procedure for TFT can be greatly simplified compared to the conventional scheme (TABLE I). In short, only a single device and two simple subthreshold I-V measurements at room temperature are all that needed for full band-gap DOS extraction. In addition, the new methodology lends itself handily to automatic measurement system. It is very simple and useful for TFT technology development as well as practical manufacturing, since the device structure (Fig. 2) and layout are compatible with modern TFT technology. In particular, the sub-gate can be formed simultaneously with the metal pad, so no extra mask is needed. And the formation of the metallic source/drain could be cleverly incorporated into the baseline by skipping the source/drain implant in the DOS test structure.

We have also characterized the dependence of both electrical and structural parameters on the measurement results in order to set suitable test conditions. Our results indicate that the parasitic resistance presenting in the channel would result in overestimation of tail state density. A sufficiently high drain and sub-gate biases and short electrical junction length are thus needed.

In this work, only the defect states contained in the channel are considered, though more precise DOS extraction is possible if the oxide interface states are also taken into account [9]. This will be the main subject of our future work.

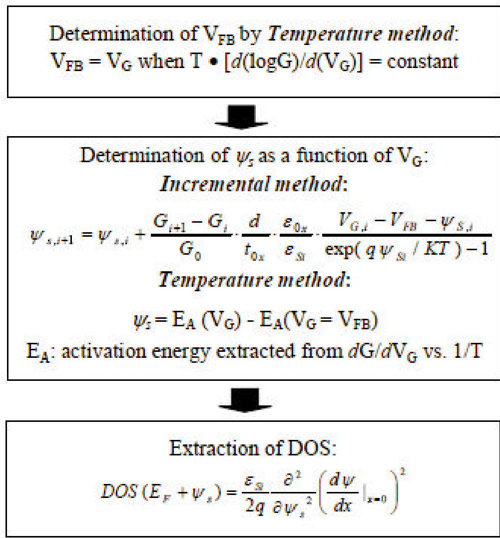

Fig. 1 Flow chart for extracting DOS in TFT using conventional FEC method.

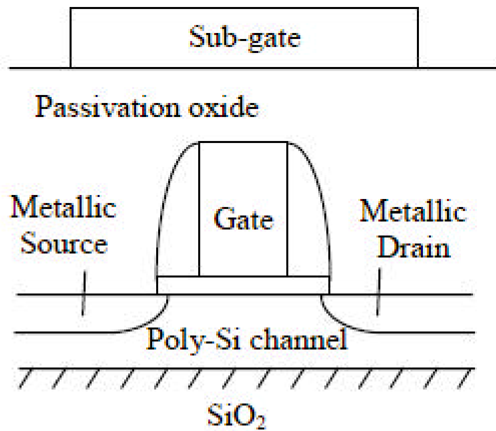

Fig. 2 Structure of poly-Si SB-TFT featuring silicide source/drain and a sub-gate lying over the passivation oxide.

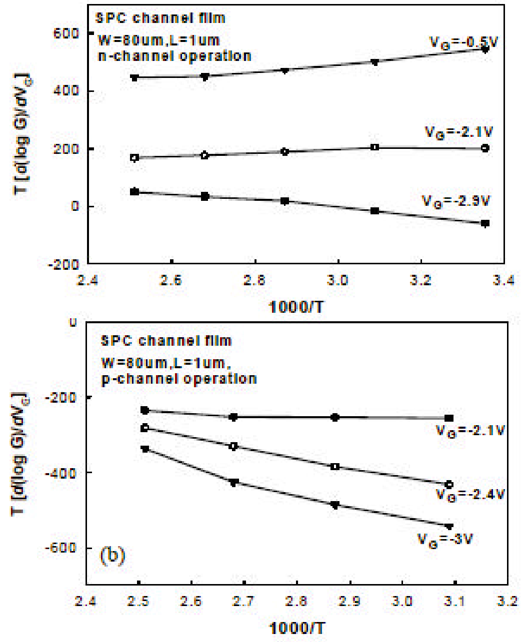

Fig. 3 T[d(logG)/dVG] vs. 1000/T for (a) a- and (b) p-channel operations of a SB poly-Si TFT. In both cases, V_{FB} is determined to be around –2.1V.

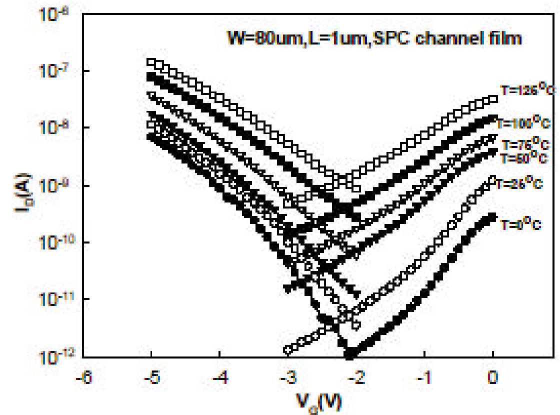

Fig.4 Ambipolar subthreshold I-V characteristics of a SB poly-Si TFT measured at various temperatures.

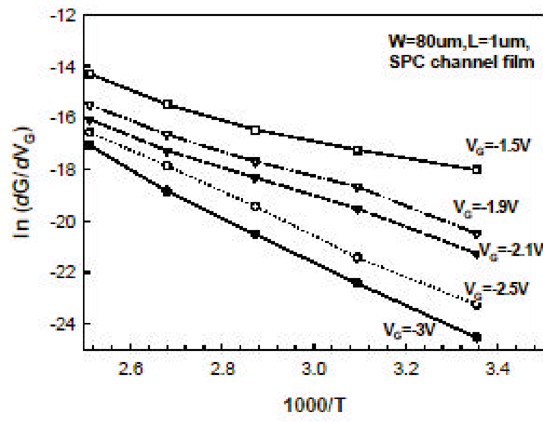

Fig. 5 Arrhenius plots of ln (dG/dV_G) extracted from Fig. 4

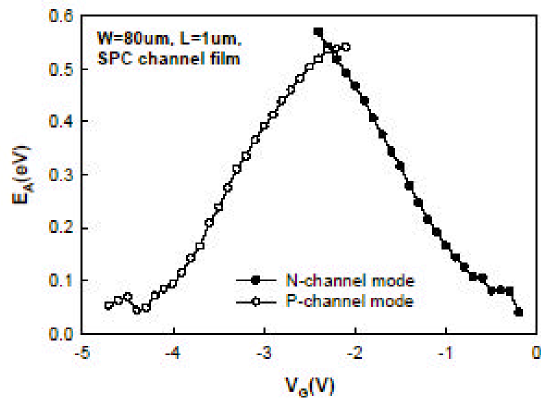

Fig. 6 Activation energy extracted from Figs. 4 and. 5.

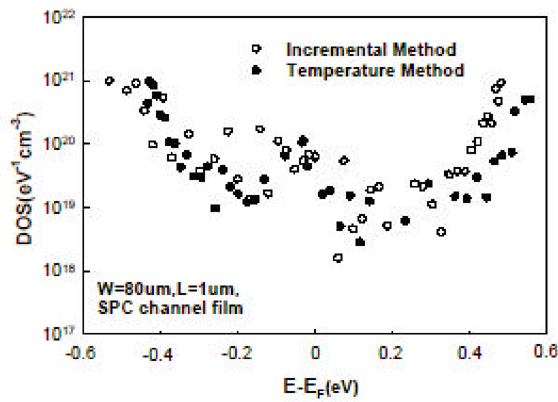

Fig. 7 DOS results obtained by using incremental method and temperature method.

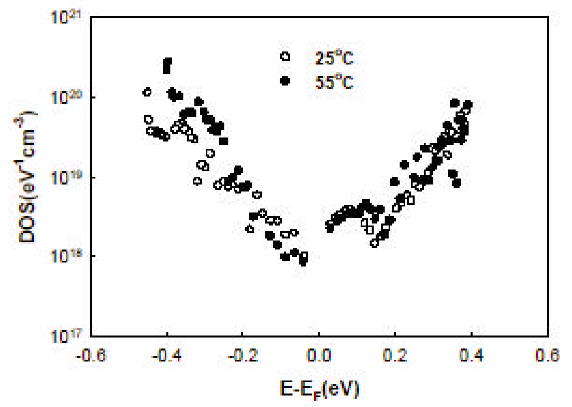

Fig. 8 DOS results obtained by using incremental method performed on ambipolar subthreshold I-V characteristics measured at 25 and 55 °C

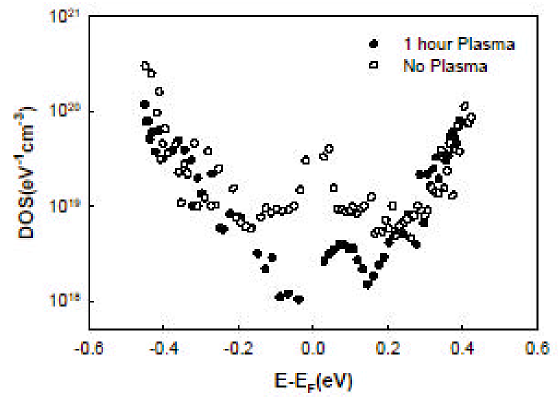

Fig. 9 Effects of plasma treatment on the DOS of devices. temperature method. The results indicate that 1-hour NH_3 treatment is effective in reducing the mid-gap defect density.

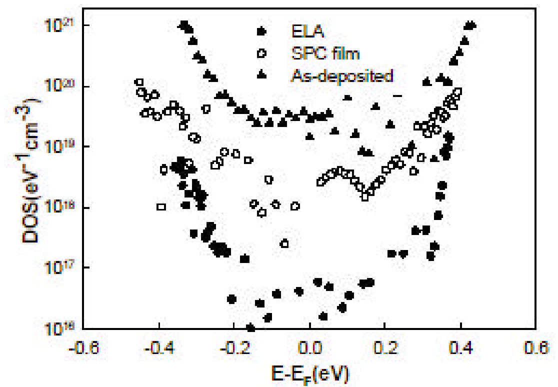

Fig. 10 Effects of different recrystallization treatments on the DOS of devices.

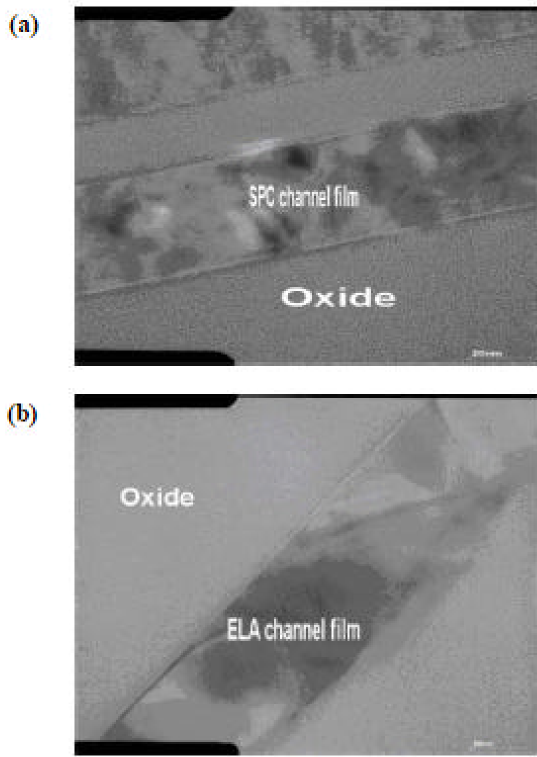

Fig. 11 TEM pictures of characterized samples that received (a) solid-phase crystallization (SPC), and (b) excimer laser annealing (ELA) treatments. The larger grain size in ELA sample well explains its low extracted DOS shown in Fig. 10.

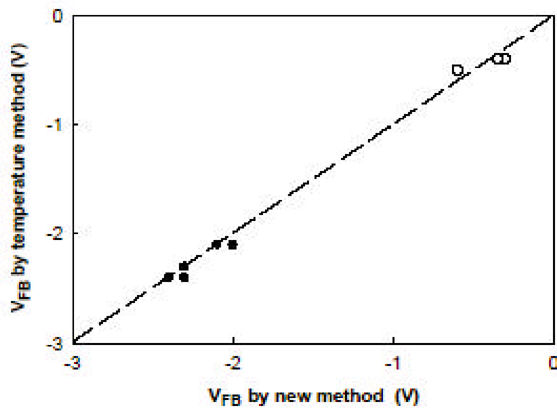

Fig. 12 Comparison of V_{FB} values determined using the conventional ***temperature method*** and the new methodology performed on two groups of devices with various parameters.

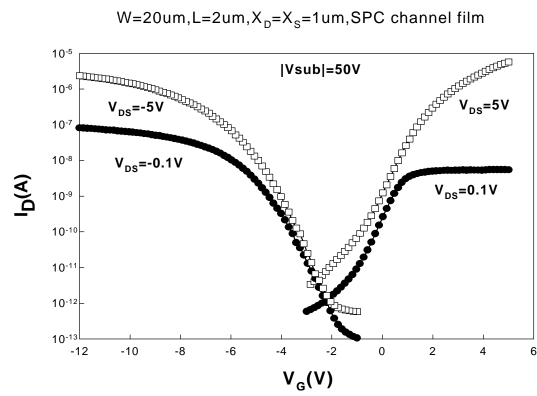

Fig. 13 Ambipolar transfer characteristics in both low and high drain bias

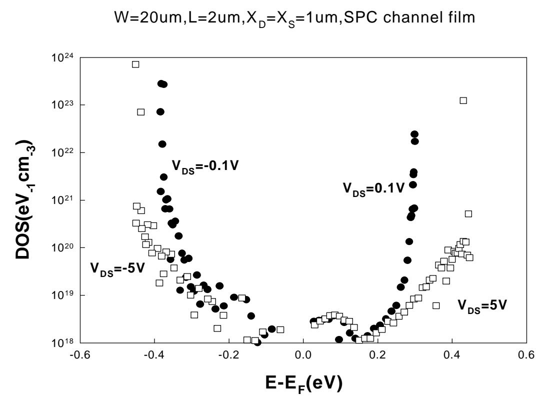

Fig. 14 Full-band gap DOS extracted at $|V_{DS}|$ of 0.1 and 5 V

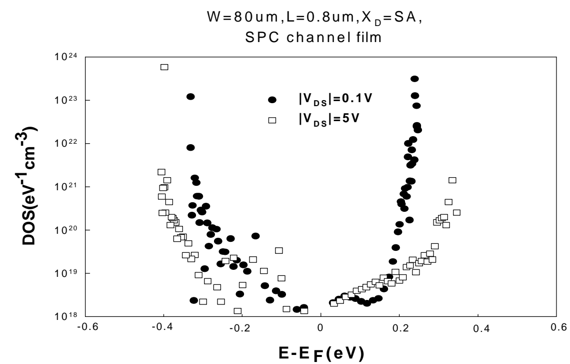

Fig. 15 The extracted DOS results in a device with channel length of 0.8um.

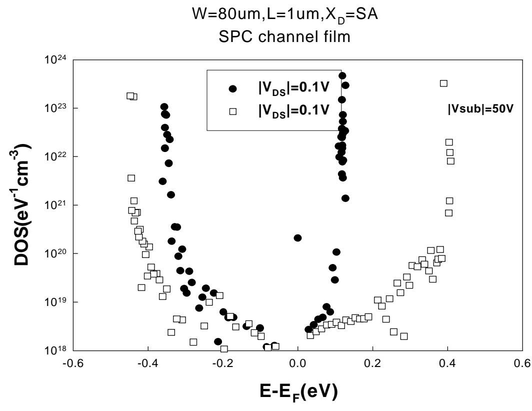

Fig. 16 The extracted DOS results in a device with channel length of 1um.

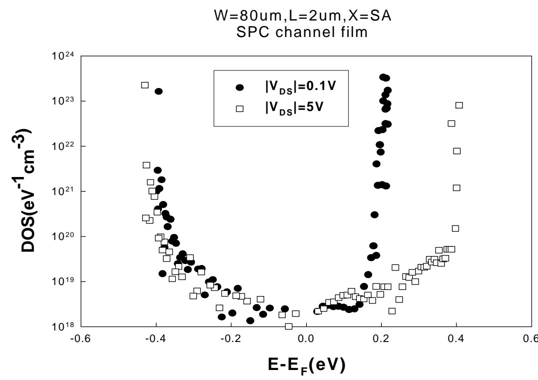

Fig. 17 The extracted DOS results in a device with channel length of 2um.

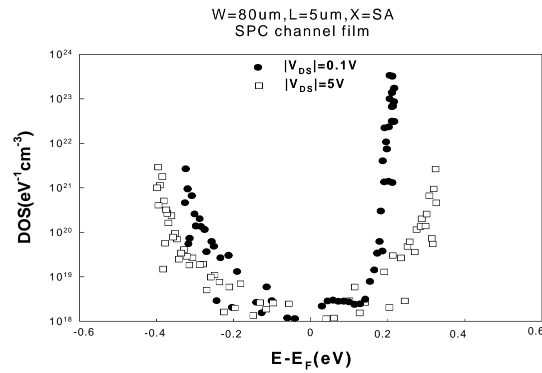

Fig. 18 The extracted DOS results in a device with channel length of 5um.

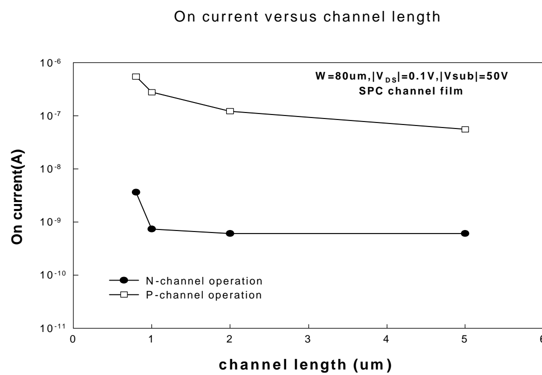

Fig. 19 On current vs. channel length

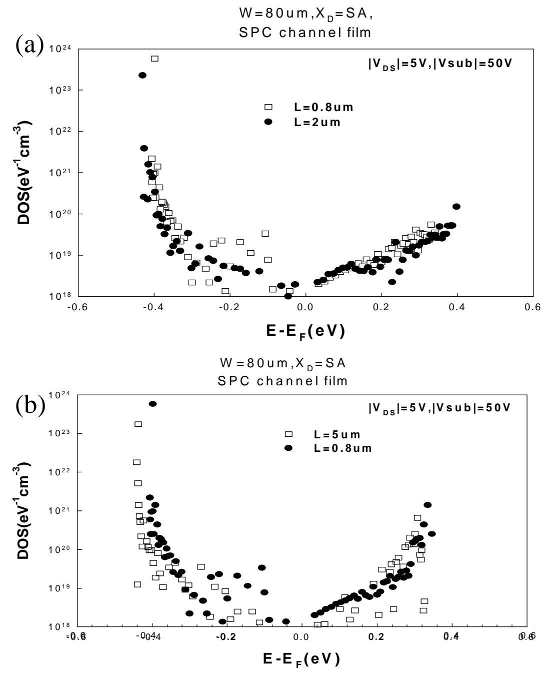

Fig. 20(a), (b) Comparison of DOS extracted in devices with various channel length.

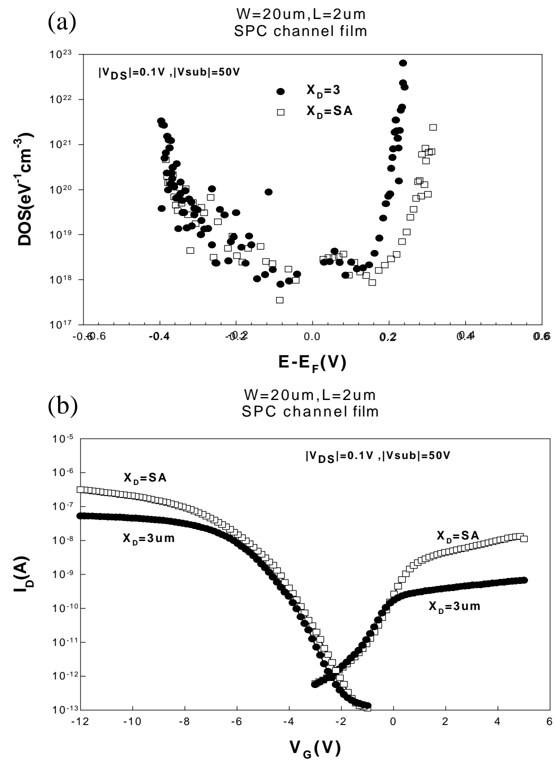

Fig. 21 (a)Ambipolar transfer characteristics of deices with various drain-side offset length at $|V_{DS}|$ of 0.1 V. (b)Full-band gap DOS extracted deices with various drain-side offset length at $|V_{DS}|$ of 0.1V.

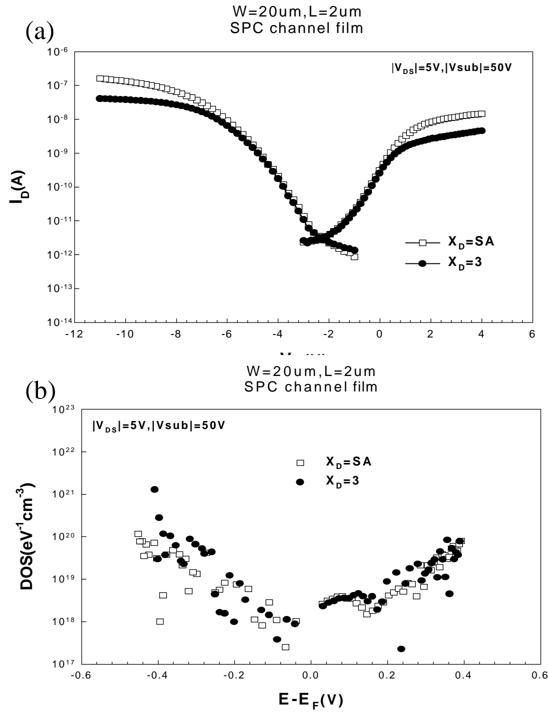

Fig. 22 (a) Ambipolar transfer characteristics of deices with variousdrain-side offset length at $|V_{DS}|$ of 5 V. (b) Full-band gap DOS extracted deices with various drain-side offset length at $|V_{DS}|$ of 5 V

TABLE I Comparison between conventional and the new methodologies.

	Conventional FEC methodology	The new methodology
Test device	One p-device for extracting DOS between Ev and Ei in the gap. One n-device for extracting DOS between Ec and Ei in the gap.	One SB device for full band-gap DOS extraction.
V_{FB} determination	*Temperature method* Multiple I-V measurements conducted at various temperatures are necessary.	V_{FB} = V_G @ the intersection point of ambipolar subthreshold I-V curves. Only needs to perform two I-V measurements at room temperature.
Determination of ψ_S as a function of V_G	*Temperature method* or *Incremental method.*	*Incremental method.*

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