行政院國家科學委員會專題研究計畫　成果報告

新型絕緣層上覆晶奈米元件(3/3)

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摘　要

本報告包含本三年期計畫之全部成果。內容分為三個部分：修正蕭基位障鰭狀電晶體(MSB FinFET)、以掃瞄探針測量載子濃度分佈、全金屬矽化物源極/汲極薄膜電晶體(FSD TFT)。

修正蕭基位障鰭狀電晶體部分，我們發明一種修正蕭基位障元件結構及製程。首先開發出兩階段退火的完全金屬矽化物源極/汲極技術，成功的利用 ITS 技術整合電子束微影等製程，製作出閘極長度 25nm 的三閘極修正蕭基位障鰭狀電晶體(MSB FinFET)，製程溫度僅 600　C。元件特性極佳，以總閘極寬度計算，在 1 伏特工作電壓下，驅動電流約 108　A/　m，若以平面佈局寬度計算，可高達 325　A/　m，和傳統 pn 接面源極/汲極元件類似。開關電流比超過 10^9，遠優於傳統 SB MOSFET。室溫下的次臨界電流上升率可低至 60.4 mV/decade，接近理想值。25nm 元件的 DIBL 約 235mV/V，也在水準之上，種種特性顯示 MSB 接面的確發生預期的效應。我們測量汲極電流的溫度效應，其活化能和經過高溫製程的傳統元件相同，證實 MSB 製程的確不會產生源極/汲極缺陷。亦探討鰭狀通道寬度對元件特性的影響，發現因為側面閘極以及金屬矽化物晶相的影響，愈窄的鰭狀通道造成愈好的元件特性。工作電壓一伏特的熱載子效應生命期遠大於十年，愈窄的鰭狀通道因為側面閘極的效應，熱載子效應較為輕微。也因為極窄的鰭狀通道，背閘極電場不易進入通道區，SOI 元件的背閘極效應得到改善。所有研究結果顯示 MSB 元件極適合繼續微縮，是 45 奈米世代以下極有潛力的元件。

掃描探針顯微術是近年來發展迅速的一種表面分析技術，具有非破壞性、二維量測、高空間解析度等諸多優點。KFM (Kelvin Probe Force Microscopy)是其中一種，能夠量測試片表面電位。藉由量測矽半導體的表面電位，KFM 可望應用於載子濃度的二維量測。本計畫首先改良既有的 KFM 系統的回饋控制電路，以得到較佳的掃瞄結果。接著探討試片的表面處理，發現經過氧化處理與氫氟酸浸泡會使試片表面產生 Si-F 及 Si-O 鍵結而導致表面電位影像對比劣化，而使用丙酮超音波震盪、氫氟酸浸泡、去離子水沖洗，可有效消除上述鍵結，提升影像對比。

修正蕭基位障鰭狀電晶體的製程技術也可以應用在薄膜電晶體。採用離子植入金屬矽化物技術，不僅可以避免植入損傷，也可以免除金屬矽化物突刺的問題。因為熱預算也可以大幅減少，得到極佳的短通道效應。漏電流接近或低於傳統的薄膜電晶體，導通電流則因為源極/汲極阻抗降低而大幅提昇。這些特性顯示，在系統面板的應用上，高性

能的全金屬矽化物源極/汲極薄膜電晶體是極有潛力的元件技術。

本計畫三年內有三名博士研究生、三名碩士研究生、數名大學生參與計畫執行。三名碩士研究生中的兩名已經獲得碩士學位，其中一名博士班研究生即將完成畢業論文。計畫成果已發表六篇 SCI 期刊論文、七篇研討會論文，另有兩篇期刊論文在審查中。近期的成果將會陸續撰寫成至少四篇期刊論文發表。專利方面，提出五件專利申請，其中兩件(中、美各一件)已經獲證，另三件在審查中。

關鍵字：鰭狀電晶體、蕭基位障、修正蕭基位障、金屬矽化物、絕緣層上矽、薄膜電晶體、掃描探針顯微術、凱爾文探針顯微鏡

Abstract

This final report includes all of the results of the 3-year project. This report is divided into three parts : modified-Schottky barrier FinFETs (MSB FinFET), dopant profiling by scanning probe microscopy, and fully-silicided source/drain thin-film transistors (FSD TFT).

In the part of MSB FinFETs, this project demonstrates a novel high performance MSB FinFETs with several unique features such as fully silicided S/D, ultra-short SDE, defect free S/D junction, and low temperature processing. A two-step Ni-salicide process is developed to completely convert the Si layer at the S/D region to silicide with controlled lateral silicidation. By inserting an ultra-short SDE using the ITS technique, the Schottky barrier is modified so that the barrier width is suppressed at the on-state and is increased at the off-state. In addition, the triple gate wrapping around the fin also effectively diminished the Schottky barrier by the gate-fringing effect. With a 4 nm thick gate oxide, the I_{on}/I_{off} current ratio over 10^9 is achieved, and the room temperature subthreshold swings of 25 nm and 49 nm MSB FinFETs are as low as 83 and 60.4 mV/decade, respectively. These values are close to the theoretical limitations. The I_{on} of the 25nm MSB FinFET at $|V_d| = |V_g-V_{th}| = 1$ V is higher than 108 μA/μm or 325 μA/μm, depending on the definition of channel width. The I_{on} of 108 μA/μm is lower than the conventional devices. However, if we consider the actual deriving capability of devices with the same layout width, the I_{on} of the MSB FinFET, 325μA/μm, will be compatible with that of conventional planar MOSFETs. The MSB FinFETFs with narrower fins have better hot-carrier immunity (HCI) and could more efficiently restrict the influence of buried oxide quality induced by the V_b. It is not only attributed to the decreasing of the ratio of buried oxide interface to front gate oxide interface but also attributed to the screening effect by the extension of side gate. The extrapolated hot-carrier lifetime encourages the MSB nFinFETs as promising sub-10nm devices. All of these results indicate that the MSB FinFET would be a very promising device beyond 45 nm technology node.

Kelvin probe force microscopy is a useful tool for 2D surface potential imaging. For semiconductor material, it is able to be applied to measure dopant type and dopant concentration. Its 2D imaging capability and high spatial resolutions are the advantages for the dopant profiling application in submicron semiconductor devices. However, because the surface potential is sensitive to the surface condition, 2D profiling on a cleaved surface is still difficult at this moment. Great efforts must be devoted to solve this issue. Therefore, we can not measure the doping profile of the ultra-short SDE of the MSB junction fabricated in this project.

The MSB junction technique can be applied for TFTs. Using ITS technique, not only the implant-damages but also the silicide spiking is avoided. Furthermore, the activation thermal budget of the proposed devices can be decreased obviously than that of conventional ones with long-term furnace annealing. At off-sate; therefore, the Ioff of FSD devices is equal to (n-channel) or smaller than (p-channel) that of the CN TFTs. At on-state, due to the fully-silicide S/D and SDE structure, the parasitic resistance of S/D region and the contact resistance between silicide and channel are reduced. Therefore, superior I_{on}/I_{off} ratio can be obtained. The influences of annealing temperature and time are also examined in this work. A 600°C/30sec rapid thermal annealing is sufficient to diffuse and activate the dopants, and then fabricate high performance FSD TFTs. Excellent short channel behavior of the FSD TFTs are also confirmed. To conclude, the high performance FSD TFTs with low parasitic resistance fabricated by low thermal budget process are promising devices for AMLCD, AMOLED and system-on-panel applications.

In the past three years, 3 Ph.D students, 3 graduate students, and several under-graduate students involved this project. Among them, 2 of the 3 graduate students have received their MS degree and one Ph.D student is preparing his Thesis. Parts of the results have been published as 6 SCI journal papers and 7 conference papers. Another 2 SCI journal papers are under reviewing procedure. Recent results will be written as 4 SCI journal papers at least. We also applied 5 patents. Two of them have been authorized and the other 3 are pending.

Key Words : FinFETs, Schottky barrier,modified-Schottky barrier (MSB), metal silicide, silicon-on-insulator (SOI), thin-film transistors, scanning probe microscopy (SPM), Kelvin probe Force Microscopy (KFM)

Contents

Chapter 1
Introduction

1-1 Project Background

The first Schottky barrier MOSFET (SB-MOSFET) utilizing metal silicide to replace the heavily doped silicon within the source/drain regions was proposed in 1968 [1]. Compared with conventional MOSFET, SB MOSFET had several advantages including easy processing, ultra-shallow junction, low source/drain (S/D) series resistance, low thermal budget, and excellent short channel effect immunity. In 1983, the Schottky barrier PMOS was proposed to eliminate the latch-up effect [2, 3]. However, the drawbacks of high drain leakage current attributed to the thermionic emission current and low driving capability due to the abnormally high Schottky barrier height made it impractical [4, 5]. Subsequently, asymmetric Schottky MOSFET with Schottky barrier source junction and p-n drain junction was shown to solve the leakage current issue [6]. However, the problem of low driving current left unsolved. Furthermore, the asymmetric device is difficult to be scaled down.

Recently, nano scale SB-MOSFETs were proposed so that the driving capability could be improved by the gate-fringing field due to the short spacer length [7]. Nevertheless, previous problems still existed for those nano scale SB-MOSFETs. For example, the gate fringing field could not suppress the Schottky barrier effectively, so that the on-state current (Ion) of SB-MOSFET was still lower than that of the conventional MOSFET. A method of reducing this barrier by using complementary silicide (PtSi for PMOS and ErSi for NMOS) on bulk or SOI substrate has been suggested [7, 8]. However, the process to form complimentary-silicide was more complex than that to form single silicide, and the abnormally high off-state leakage current (Ioff) due to the thermionic injection and GIDL-like effect was still a problem [9]. Adding a metal field-plate over the MOSFET was shown to be effective in reducing the off-state leakage current by suppressing thermionic-injection from the drain contact; nevertheless, it required an additional voltage supply and it sacrificed device density [10]. The SOI structure with fully silicided S/D and doped S/D extension (SDE) fabricated by a conventional process was also reported to have proper electrical characteristics [11]. It was basically a conventional MOSFET with identical thermal budget.

In this project, to overcome the drawbacks of SB-MOSFETs while keeping the advantages of low S/D external resistance and low temperature process, a new Modified

Schottky barrier (MSB) FinFET with ultra-short SDE using an implant-to-silicide (ITS) process is proposed. It is a fully-deplete silicon-on-insulator (FD SOI) device with modified Schottky barrier source/drain junction. The silicide at source/drain consumes the whole silicon layer to reduce series resistance and junction leakage current. An ultra-shallow doping layer at the lateral side of silicide forms modified Schottky junction and suppresses the source injection resistance and the drain junction leakage current. The shallow doping layer can be formed by lateral out-diffusion of dopant implanted into metal or metal silicide layer so that the process temperature can be reduced to around 600℃. In the MSB FinFET structure, the gate wraps around the rectangular silicon fin from three sides, so that a significantly high driving current and excellent short channel effect could be achieved at the same feature size [12]. Furthermore, the proposed MSB device is expected to exhibit significantly lower I_{off} than the conventional SB device because of the thick Schottky-barrier at the drain/body junction during off-state.

1-2 Report Organization

Beside the fundamental e-beam lithography and plasma etching techniques for nano scale pattern transformation, the key process developed in this project is a two-step annealing technique under 600°C to control the silicidation process for the MSB FinFET. We also carried out a detailed study on the I-V characteristics of the MSB FinFET with various fin thicknesses. Based on these results, the conduction mechanisms for on-state and off-state were proposed. The temperature effect was studied and the leakage current mechanism was analyzed. The uniformity dependence of SDE region related to the electrical characteristics, including drain-induced barrier lowing (DIBL) and subthreshold swing (S.S) were also investigated. Since the MSB FinFTEs exhibited excellent fundamental characteristics, the hot carrier reliability as well as the back gate bias effect was investigated.

The MSB junction property is tightly related to the doping distribution of the SDE. It is important to known the actual doping distribution in the SDE area. Typical depth profiling techniques such as spreading- resistance profiling (SRP) and secondary- ion- mass-spectroscopy (SIMS) do not work at such a tiny area. Therefore, a new scanning probe microscopy (SPM) technique named Kelvin-Force Microscope (KFM) was evaluated for this application. Furthermore, since the TFT process is very similar to the SOI process, the proposed MSB process was also applied to fabricate TFTs. A 0.1um TFT was demonstrated by integration metal gate, high-dielectric constant gate dielectric, and MSB S/D junction

successfully.

This final report is organized as follows :.

In chapter-1, we briefly explain the background of this project and the report organization. In chapter-2, the detailed MSB FinFET process is explained. The S/D silicidation is a key process and is also discussed in this chapter. In chapter-3, the basic characteristics of the MSB FinFET as well as the fin-width effect is demonstrated and discussed. In chapter-4, the hot-carrier reliability and the back gate bias effect of the MSB FinFETs are investigated. Chapter-5 discusses the feasibility of using KFM to detect the doping profile of the tiny region. Chapter-6 describes the process window and characteristics of the TFTs with MSB S/D junction. Chapter-7 summaries the important results achieved in these three years. The publications and patents generated from the execution of this project are listed in the appendix.

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Chapter 2
Fabrication of Modified Schottky Barrier FinFETs

In this chapter, we present the detail of fabrication process of the proposed MSB FinFET. I was observed that fully silicidation of the source/drain region without attacking the channel region is a key process. So, the silicidation process is examined carefully.

2-1 Main Process Flow

Fig.2-1 shows the main process steps of the MSB FinFET fabrication. The starting material was boron-doped 6-in SOI wafer with a low doping concentration of around $1x10^{15}$ cm-3. The nominal Si layer and buried oxide layer thicknesses were 50 nm and 150 nm, respectively. The Si layer was thinned down to 40 nm by thermal oxidation. The device islands (including S/D region and Si fins) were defined by electron-beam (e-beam) lithography and plasma etching. A 4 nm thick SiO_2 was thermally grown as the gate dielectric. Since the gate oxide thickness on the top and sidewall of the Si fin are similar, the final device is a tri-gate FinFET. Poly-Si film of 150 nm thick was deposited and doped by BF_2^+ ion implantation for PMOS and P^+ ion implantation for NMOS at 40 KeV to a dose of $5x10^{15}$ cm^{-2}. After rapid thermal activation at 1025°C for 10 sec, a 50 nm thick TEOS oxide was deposited in a low pressure chemical vapor deposition system as hardmask. As shown in Fig.2-1(a), e-beam lithography was employed again to define the gate pattern. Following gate patterning, a SiO_2 (10nm)/Si_3N_4 (30nm) composite spacer was formed, as shown in Fig.2-1 (b). The hardmask on poly-Si was etched away during spacer etching. Self-aligned Nickel silicide (Ni-Salicide) process was then performed and the resulting structure is shown in Fig.2- 1(c). The sheet resistance of the silicide layer is about 10Ω/□ as measured by a Van der Pauw structure. This silicidation process is the key process step for the MSB FinFET and is discussed extensively in the next section.

To modify the characteristics of the Schottky barrier, BF_2^+ ions for PMOS and P^+ for NMOS were implanted to silicide at 30 KeV to a dose of $3x10^{15}$ cm^{-2} followed by a furnace annealing at 600 °C for 30 min. The silicide layer acts as a stop layer for the implanted ions and as a solid diffusion source for the lateral diffusion of ions into the silicon region to form an ultra-short SDE. Monte-Carlo simulation shows that the straggling distribution of ions is only 8 nm, which is shorter than the lateral growth of silicide [1]. Hence, all of the implanted

ions were confined in the silicide region and the channel region was not damaged. It has been reported that the ITS process forms a modified Schottky junction with characteristics between a pn junction and a pure Schottky junction [2-4]. Since the ion implantation does not directly damage the Si layer, the junction would be free of crystalline defects and low junction leakage current could be expected. During the post-implantation annealing, boron atoms were diffused out of the silicide and piled up at the Si/silicide interface to form an ultra-short SDE uniformly as indicated in Fig.2-1 (d). In this ITS technique, since the annealing temperature is not determined by the annihilation of ion implantation induced damages, the thermal budget is greatly reduced.

Typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. For comparison, a simple Schottky barrier (SB) FinFET without the ITS process step and conventional (CN) FinFET without S/D silicidation were also fabricated. The post S/D implantation annealing was performed at 1025°C for 20 sec in N2 ambient for the CN FinFET.

2-2 Ni-salicide Technique

Ni reacts with Si to form Ni-rich silicide at temperatures as low as 200°C, so the Ni-silicide is typically formed by one-step rapid thermal annealing at 400-600°C for 30-60 sec. The unreacted Ni can be selectively removed using a H_2SO_4+H_2O_2 mixture. Since the dominant diffuser during silicide formation is Ni, the Ni-silicide is confined at the Si region and the gate to S/D isolation can be controlled easily. However, as the Si region becomes small, a large number of Ni atoms can be supplied from the Ni film deposited on the isolation region. It has been reported that excess silicidation occurs in the conventional one-step rapid thermal annealing at 500~600°C due to the fast diffusion of Ni atoms from regions surrounding the small silicon region [5]. In bulk CMOS, the failure modes are poly-Si gate depletion and S/D junction leakage current. In the fully depleted SOI devices, excess silicidation may result in different failure modes.

According to the volume ratio of Ni silicidation, a 22 nm thick Ni film was deposited by a DC sputtering system to completely convert the 40 nm thick Si to silicide. Fig.2-2 shows the cross-sectional transmission electron micrograph of an MSB device after one-step rapid thermal silicidation at 600°C for 30 seconds. As expected, no silicide was observed on the sidewall spacer. However, it is surprising that the poly-Si gate was fully silicided and the silicide extended from S/D into the channel region so that the whole channel region was

converted to silicide and the gate was directly shorted to S/D. The S/D to gate leakage current was measured for all devices.

To completely convert the Si layer in the S/D region into silicide with suitable lateral growth and without excess silicidation, a two-step annealing technique must be employed. Initially, the wafer deposited with 22 nm thick Ni film was annealed in vacuum chamber at 300°C for 80 min to form Ni_2Si at the S/D and the poly-Si gate regions. At this low temperature, Ni diffusion from the surrounding regions is slow and is insignificant to cause excess silicidation problem. After selective removal of unreacted Ni, the wafer was rapidly thermally annealed in ambient N_2 at 600°C for 30 sec. During this annealing step, there was no excess Ni atoms surrounding the small active region, so, the excess silicidation problem was avoided. Fig.2-3 shows the schematic layout and cross-sectional TEM micrographs of the MSB FinFET with gate length (L_g) of 25 nm, fin thickness (W_f) of 40 nm, and fin height (T_{Si}) of 40 nm. The thickness and lateral growth of silicide are well controlled, and it is confirmed that the SDE was defect-free.

Fig.2-4 shows the electron diffraction pattern at the positions of A, B (S/D region), and C (gate region) indicated in Fig.2-3(b). The silicide phases at the gate region and S/D region were identified as NiSi and NiSi2, respectively. This phase difference is presumably caused by the differing stresses in the S/D region and gate region [6].

The doping profile of the ultra-short SDE is critical. However, since the volume of the SDE is so small, neither Secondary Ion Mass Spectroscopy (SIMS) nor Spreading Resistance Profiling (SRP) could be applied. The spatial resolution of Scanning Capacitance Microscopy (SCM) was also not sufficient. Kelvin probe Force Microscopy (KFM) with a carbon nano-tube probe might be a solution but great efforts would be needed to implement this technique. The feasibility of KFM for doping profiling will be discussed in chapter-5. We could not correctly determine the doping profile of the SDE in this project. However, electrical characteristics of the MSB devices shown in the following chapters clearly support the existence of the SDE.

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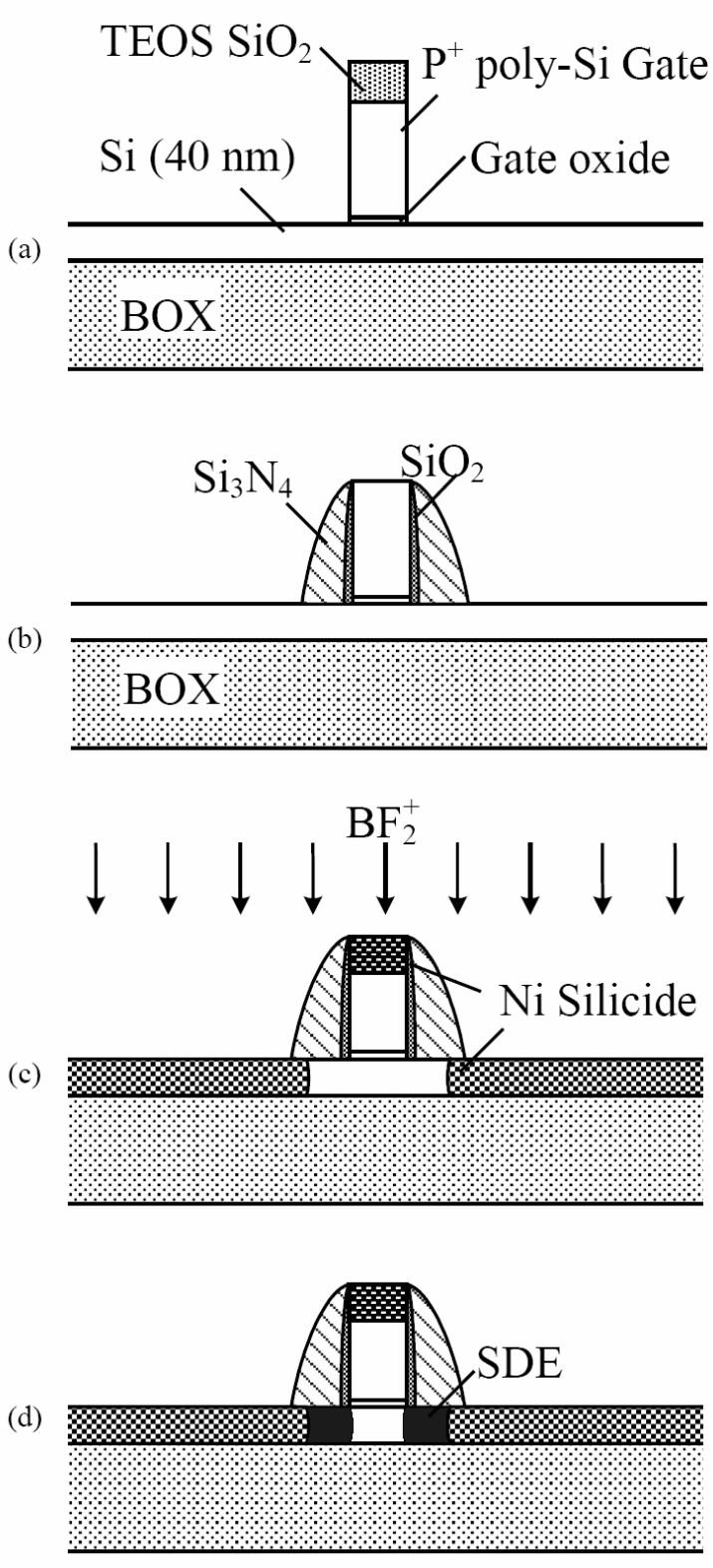

Fig.2-1. Main process flow of the modified Schottky barrier FinFET.

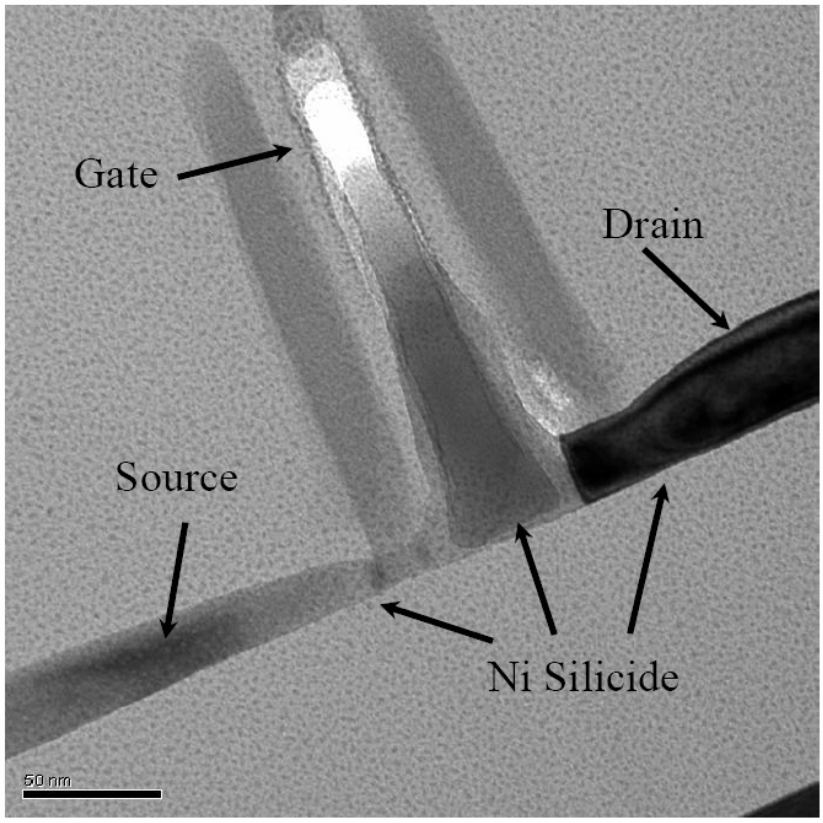

Fig.2-2. Cross-sectional transmission electron micrograph of the 25 nm MSB FinFET fabricated by one-step rapid thermal silicidation at 600°C for 30 seconds.

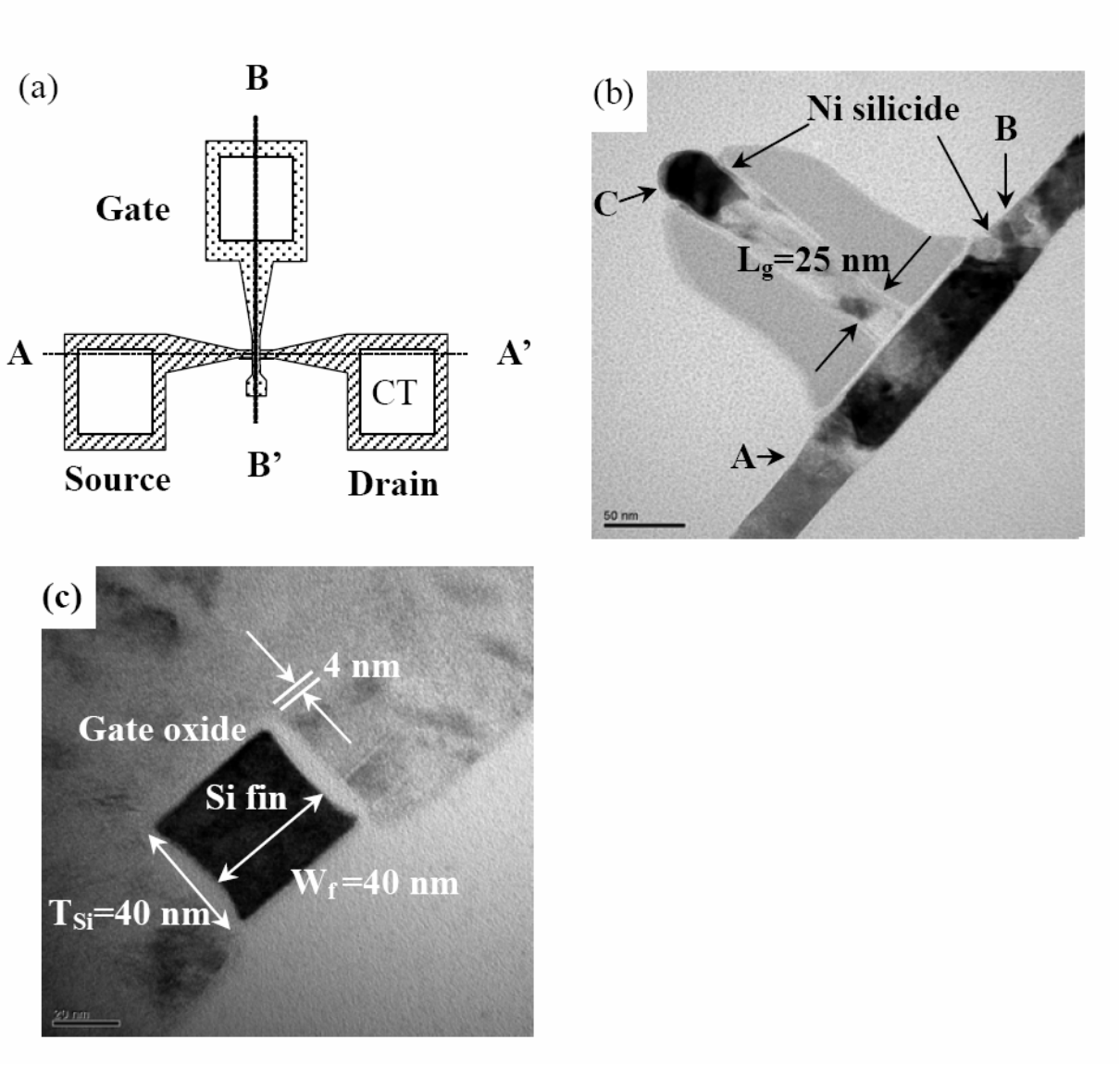

Fig.2-3. (a) Schematic layout, (b) cross-sectional TEM micrograph along line A-A' in (a), and (c) cross-sectional TEM micrograph along line B-B' in (a) of the MSB FinFET with L_g = 25 nm, W_f = 40 nm and T_{Si} = 40 nm.

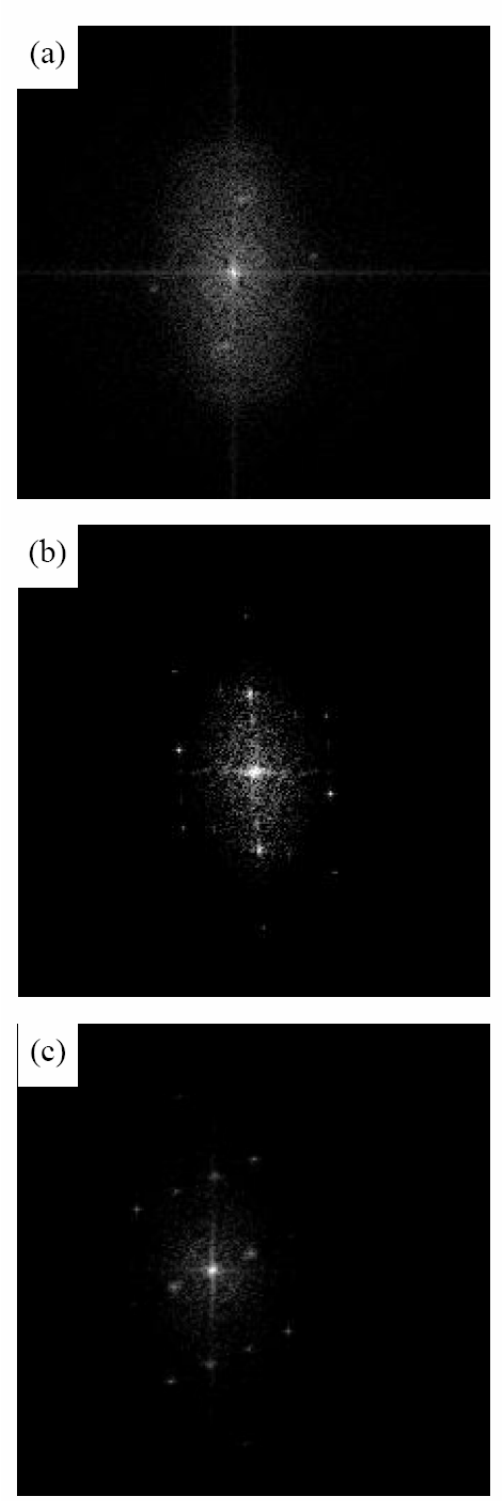

Fig.2-4. Electron diffraction pattern of the Ni silicide at (a) position A, (b) position B, and (c) position C, as indicated in Fig.2-3 (b). Phases at the source/drain region and gate region are $NiSi_2$ and NiSi, respectively.

Chapter 3
Characteristics of Modified Schottky Barrier FinFETs

3-1 Basic Electrical Characteristics of p-channel MSB FinFETs

Fig.3-1 shows the typical output characteristics of the MSB FinFET and the SB FinFET with L_g= 25 nm, W_f = 40 nm, and T_{Si} = 40 nm. It is known that for conventional SB devices, the “sublinear” phenomenon is pronounced in the linear region due to the Schottky barrier and the channel-S/D offset. For our SB FinFET, the large channel-S/D offset should be the dominant mechanism, although the effect of Schottky barrier cannot be ignored. For the MSB FinFET, the ultra-shallow SDE will bridge the channel and S/D silicide. Furthermore, the Schottky barrier thickness, i.e. the carrier injection resistance from source to channel, is reduced by the high concentration of ultra-short SDE. Therefore, the “sublinear” phenomenon is not observed. On the other hand, the parasitic series resistance is also effectively reduced by the fully silicided S/D structure. The driving current of the 25 nm MSB FinFET at $|V_{ds}|$ = $|V_{gs}-V_{th}|$ = 1 V exceeds 108 μA/μm under the definition of channel width W= $2*T_{Si} + W_f$, or 325 μA/μm under the definition of channel width W= W_f. It should be noted that the Ion could be further improved by shorter spacer length and thinner gate oxide thickness.

Fig.3-2 presents the transfer characteristics of the MSB FinFET with L_g= 25 nm, W_f= 40 nm, and T_{Si}=40 nm. By inserting an ultra-short SDE to modify the Schottky barrier property, the MSB FinFET can turn on more steeply and it had an extremely high I_{on}/I_{off} current ratio, exceeding 10^9. The 25 nm MSB FinFET also shows superior subthreshold characteristics with a swing of 83 mV/decade and a drain-induced-barrier-lowering (DIBL) of 235 mV/V. These values are close to the 3-dimensional simulation results and could be further improved by reducing of the fin height and fin thickness to get better gate controllability [1].

The transfer characteristics of MSB, SB and CN FinFETs with L_g= 49 nm, W_f= 60 nm, and T_{Si}= 40 nm are compared in Fig.3-3. The poor driving capability of the CN FinFET can be explained by the high S/D resistance due to the un-silicided S/D region. The better DIBL of the MSB FinFET than that of the CN FinFET confirms the advantage of the low thermal budget of the MSB process. The 49 nm MSB FinFET shows an excellent subthreshold swing (60.4 mV/decade), excellent DIBL (39 mV/V), and extremely high I_{on}/I_{off} current ratio (>10^9). These results are better than those reported from conventional FinFETs and SB MOSFETs. Conversely, in the case of SB FinFET, a typical ambipolar operation is observed. For the

p-channel operation, the SB FinFET has poor subthreshold swing and an I_{on}/I_{off} current ratio of lower than 10^3. It has been proposed that the effective Schottky barrier height of thin-body SOI SB MOSFET is higher than that of the bulk SB MOSFET due to quantum confinement in the direction normal to the channel so that the on-state current is low [2]. The effective Schottky barrier at the off-state is lowered by the GIDL-like mechanism, which makes the off-state characteristic of the SB FinFET undesirable [3].

According to the above observations, band diagrams of devices at the on-state and off-state are schematically illustrated in Fig.3-4 and Fig.3-5, respectively. When the device operates at the on-state, the high concentration ultra-short SDE effectively thins out the Schottky barrier width between source silicide and the inverted channel so that the holes can tunnel through the barrier much more easily. On the other hand, when the device operates at the off-state, due to the ultra-short SDE, the modified Schottky barrier at the drain contact is wider and higher than the conventional SB devices, so it can effectively block electron tunneling. Therefore the proposed MSB FinFET exhibits excellent on/off performance.

To further understand the conduction mechanism of the off-state leakage current, the I-V characteristic of the MSB FinFET with L_g= 65 nm was measured at different temperatures from 100 K to 500 K, as shown in Fig.3-6. At room temperature, the MSB FinFET exhibits a subthreshold swing of 78 mV/decade at V_{ds}=-1V and extremely high I_{on}/I_{off} current ratio, exceeding 10^9. The I_{off} decreases at lower temperatures, so that the I_{on}/I_{off} current ratio well exceeding 10^{10} and the subthreshold swing better than 74 mV/decade are achieved at 100 K. The Arrhenius plot of Ioff for the 65 nm MSB FinFET and CN FinFET at V_{ds}=-1 V and V_{gs}-V_{th}=0.75 V are shown in Fig.3-7. The activation energies are 0.51 eV and 0.54 eV for MSB FinFET and CN FinFET, respectively. The fact that there is almost the same activation energy implies that the MSB junction is very close to the pn junction and the low temperature process of 600°C is sufficient to drive dopants out of the silicide. Since the S/D implantation does not directly damage the Si region of the MSB FinFET and the CN FinFET experiences high temperature post-S/D implantation annealing, the low activation close to half of the energy gap cannot be explained by the defects in the Si region. The leakage current mechanism of pn junction formed by the ITS process has been investigated in the literature [4, 5]. Since the Si region is almost defect-free, the area component of leakage current is dominated by the diffusion mechanism even at room temperature. However, the peripheral component of leakage current is dominated by the surface generation current due to the surface states at the isolation edge within the depletion region. For a square junction with area smaller than 10 μm^2, the leakage current will be dominated by the peripheral component at

temperatures lower than 200°C. For fully depleted SOI devices, the junction area $T_{Si}xW_f$ is very small. The leakage current would be dominated by the surface generation current due to the surface states at the interface between gate oxide/Si and buried oxide/Si, so the low activation energy becomes reasonable. It is thus proposed that to further reduce the I_{off} of MSB FinFET, the interface quality of gate oxide and buried oxide must be improved.

3-2 Fin Width Effect

The short channel effect of FinFETs has been studied numerically and experimentally by several research groups [6-8]. Pei et al. proposed that in order to suppress SCE, the fin thickness must be less than one third of the channel width [6]. Chau et al. reported that to maintain full substrate depletion, the Si body thickness should be about 1/3 or 2/3 of the gate length in the case of single gate or double gate structures, respectively [7]. In the case of a tri-gate structure, the required Si body thickness becomes equal to the gate length [8]. In fact, the threshold channel length depends on the gate structure and the fin concentration. Fig.3-8 shows the subthreshold swing of the MSB and CN FinFETs as a function of fin thickness with L_g=49 nm and 130 nm. The CN FinFETs shows weak fin thickness dependence, which is quite different from the results in some earlier reports [6, 8], which may be explained by the low fin concentration employed in this work. Here, the top gate alone can fully deplete the channel, so the fin thickness does not clearly affect the SCE apparently. The subthreshold swing of the CN FinFETs is worse than that of the MSB FinFETs in Fig.3-8, which may result from the induced higher interface state density induced by the boron penetration.

For the MSB FinFET, thinner fin thickness results in lower subthreshold swing. However, the extent of improvement differs for MSB and CN FinFETs. Furthermore, the 130 nm MSB FinFETs exhibit better swing than the 49 nm MSB FinFETs at all fin thicknesses. Since the CN FinFETs do not show this phenomenon, it cannot be explained by the gate control capability. We suspect that this unusual phenomenon is related to the S/D silicidation.

Fig.3-9(a) and (b) show the plane-view TEM micrographs of the MSB FinFETs with W_f=49 nm and 200 nm, respectively. The silicided narrow fin shows a bamboo structure and only a single grain exists at the front edge of the S/D region. As the fin thickness becomes larger, the S/D region consists of multiple grains. The multi-grain structure results in a non-uniform front edge of the silicide, which in turn results in non-uniform front edge of the ultra-short SDE, as shown schematically in Fig.3-10. As the channel length is short, a minimal non-uniformity of the S/D junction front edge clearly affects the device subthreshold

characteristic. This postulation is also supported by the weak fin thickness dependence of subthrehold swing for the CN FinFETs shown in Fig.3-8 because the CN FinFETs have a smooth S/D junction front edge. For thin fin devices, the CN FinFETs show worse swing than the MSB FinFETs. The high external resistance of the un-silicided S/D of the CN FinFETs could explain this phenomenon.

Fig.3-11 shows the DIBL of the MSB and CN FinFETs as a function of fin thickness, indicating a trend similar to the swing. It can be observed that with suitable combination of channel length and fin thickness, MSB FinFETs can be achieved with an excellent performance of nearly ideal subthreshold swing of 60.4 mV/decade and DIBL of 39 mV/V.

3-3 Conclusions

This chapter demonstrates a novel high performance MSB FinFETs with several unique features such as fully silicided S/D, ultra-short SDE, defect free S/D junction, and low temperature processing. A two-step Ni-salicide process is developed to completely convert the Si layer at the S/D region to silicide with controlled lateral silicidation. By inserting an ultra-short SDE using the ITS technique, the Schottky barrier is modified so that the barrier width is suppressed at the on-state and is increased at the off-state. In addition, the triple gate wrapping around the fin also effectively diminished the Schottky barrier by the gate-fringing effect. With a 4 nm thick gate oxide, the I_{on}/I_{off} current ratio over 10^9 is achieved, and the room temperature subthreshold swings of 25 nm and 49 nm MSB FinFETs are as low as 83 and 60.4 mV/decade, respectively. These values are close to the theoretical limitations. The I_{on} of the 25nm MSB FinFET at $|V_d| = |V_g - V_{th}| = 1$ V is higher than 108 μA/μm or 325 μA/μm, depending on the definition of channel width. The I_{on} of 108 μA/μm is lower than the conventional devices. However, if we consider the actual deriving capability of devices with the same layout width, the I_{on} of the MSB FinFET, 325μA/μm, will be compatible with that of conventional planar MOSFETs.

Activation energy analysis indicates that the SDE effectively modifies the Schottky barrier, resulting in excellent electrical characteristics. The same activation energy of the low thermal budget MSB FinFETs and high thermal budget CN FinFETs confirms that the MSB junction is very close to the pn junction and the low temperature process of 600°C is sufficient to drive dopants out of silicide. Since the leakage current of drain junction at the off-state is dominated by the surface generation current due to the surface states at the gate oxide/Si and buried oxide/Si interface, it is thus proposed that to further reduce the I_{off} of

MSB devices, the interface quality of gate oxide and buried oxide must be improved.

Structural analysis shows that as the fin width becomes larger than the silicide grain size, the multi-grain structure results in a rough front edge of the MSB junction, which in turn degrades the short channel device performance. This result indicates that the MSB process is suitable for FinFETs.

Beyond the 65 nm technology node, it is predicted that the metal gate and high k gate dielectric must be employed to improve the device characteristics continuously. Furthermore, thermal stability between metal gate and high k dielectric is a critical issue because the conventional S/D process requires a high temperature annealing of at least 900°C. Since the MSB process temperature is around 600°C, the thermal stability issue is relaxed and the interfacial layer formation at high k dielectric and Si interface is also reduced. Furthermore, the low thermal budget produced by the ultra-short SDE helps device scale-down. It can thus be considered that the MSB FinFET is a very promising nano device.

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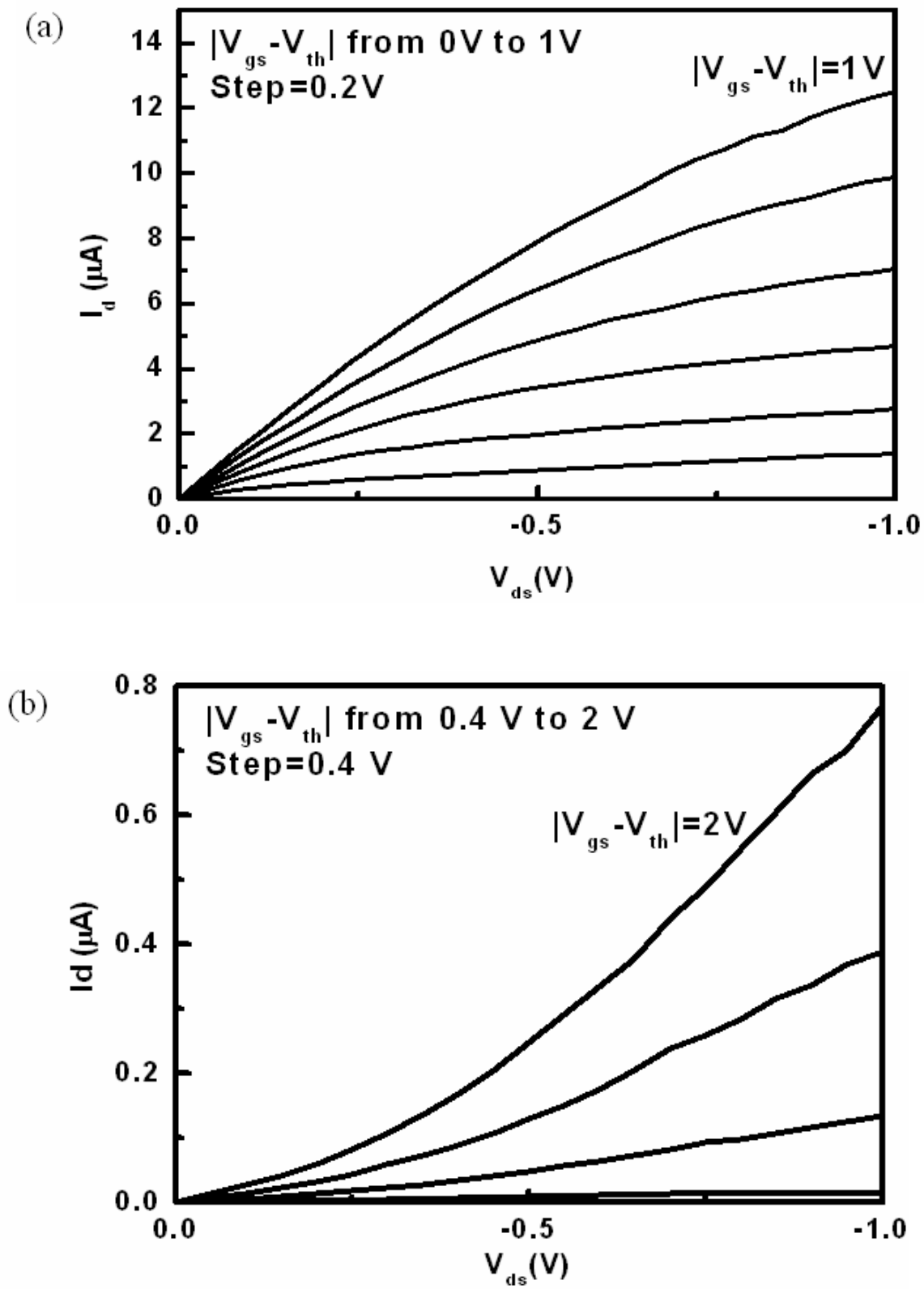

Fig.3-1. Output Characteristics of (a) the MSB FinFET and (b) the SB FinFET with L_g = 25 nm, W_f = 40 nm and T_{Si} = 40 nm.

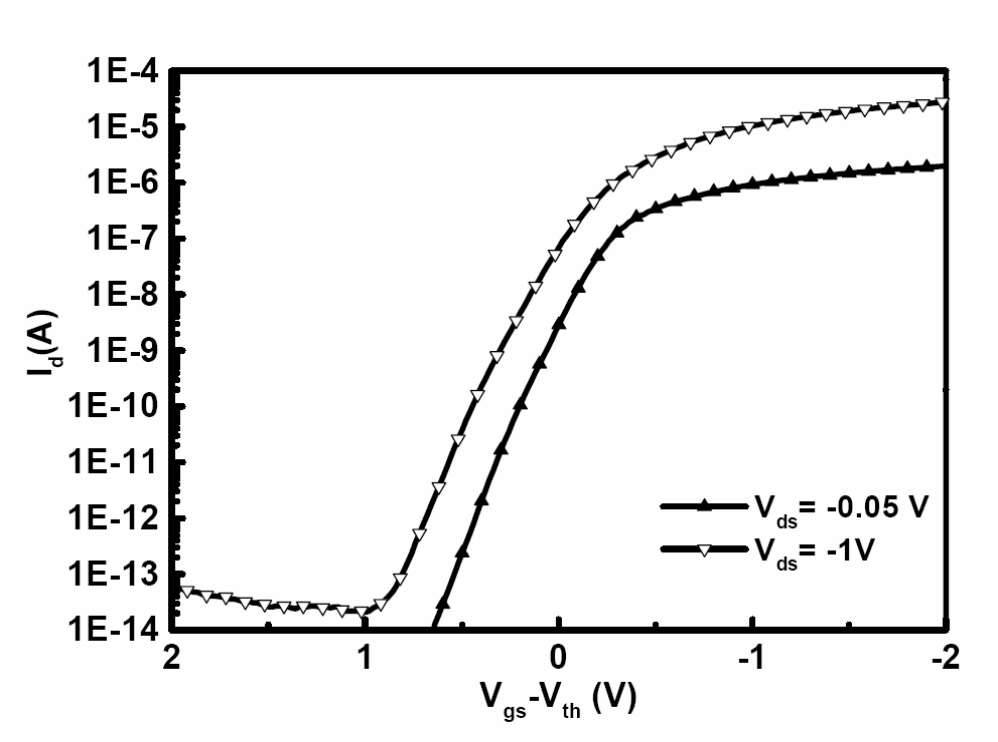

Fig.3-2. Transfer characteristics of the MSB FinFET with L_g = 25 nm, W_f = 40 nm and T_{Si} = 40 nm.

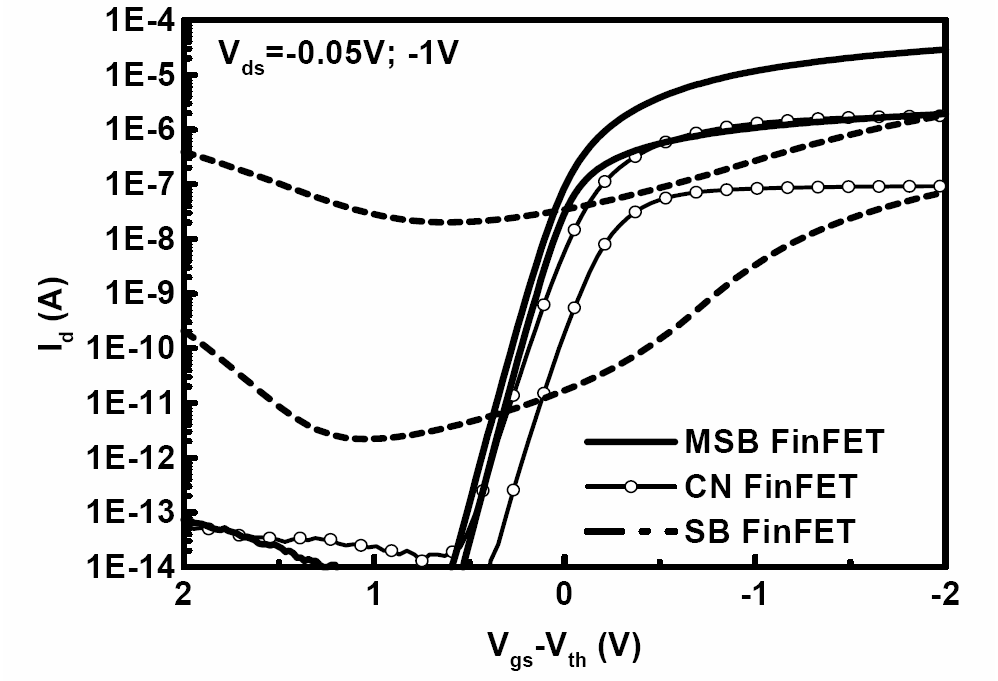

Fig.3-3. Transfer characteristics of the MSB, SB and CN FinFETs with L_g= 49 nm, W_f= 60 nm, and T_{Si}= 40 nm.

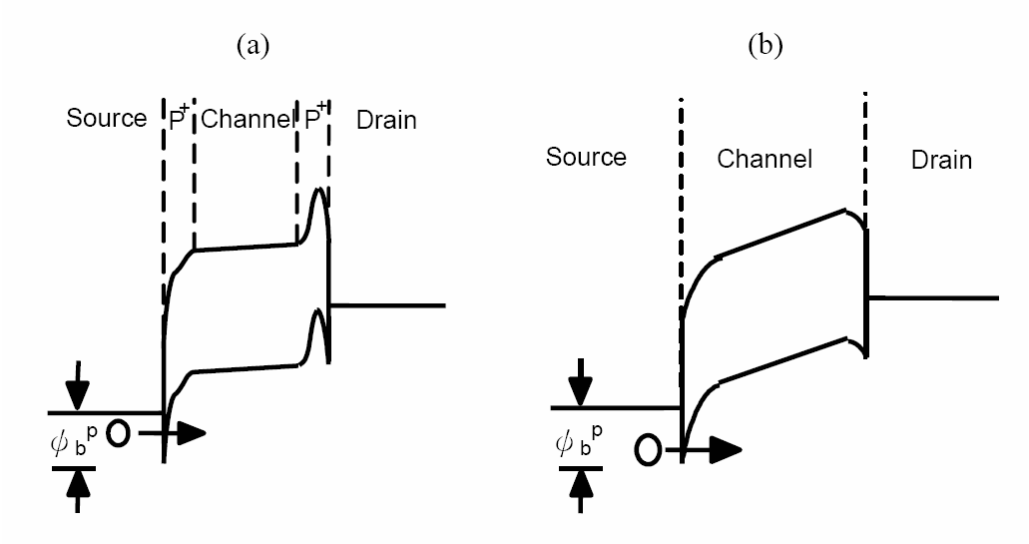

Fig.3-4. Schematic band diagrams of (a) MSB FinFET and (b) SB FinFET during the on-state.

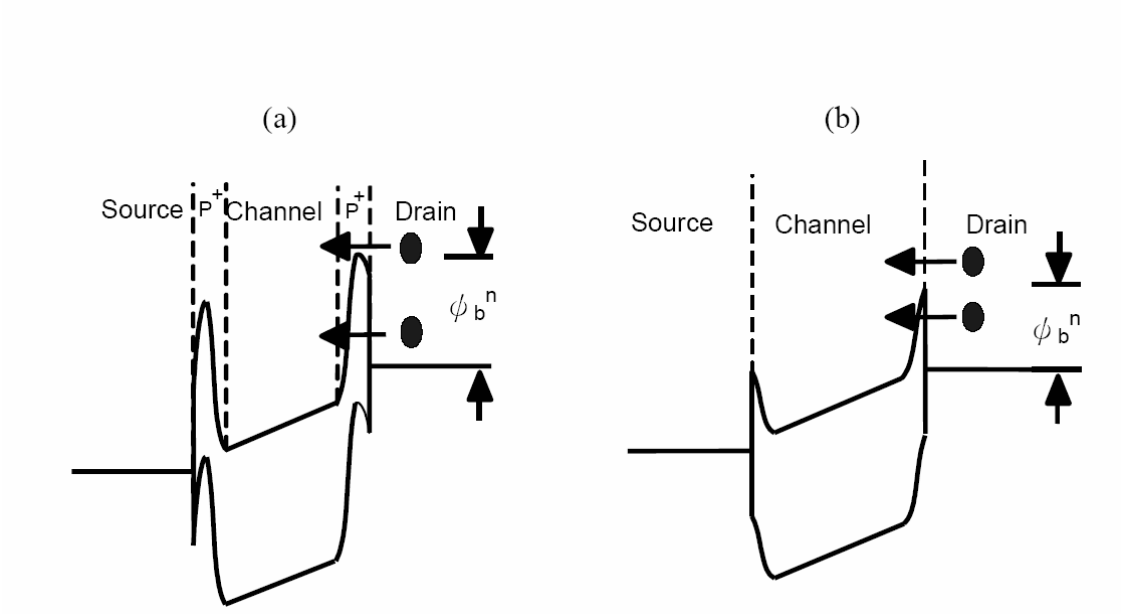

Fig.3-5. Schematic band diagrams of (a) MSB FinFET and (b) SB FinFET during the off-state.

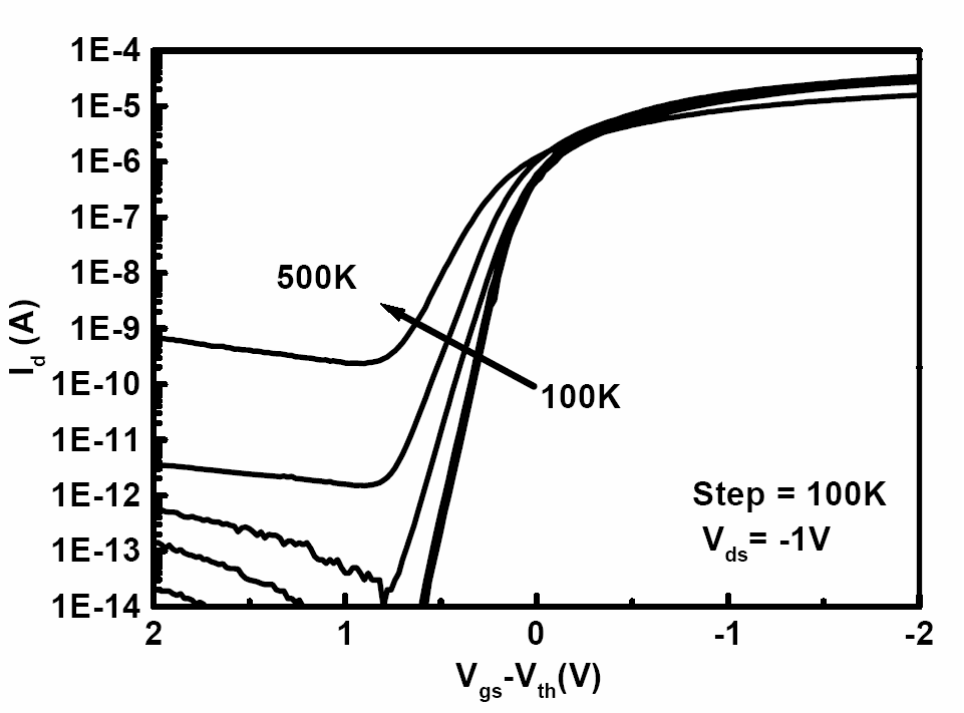

Fig.3-6. Transfer characteristics of the MSB FinFET with L_g = 65 nm W_f = 60 nm, and T_{Si} = 40 nm measured at temperatures from 100 K to 500 K.

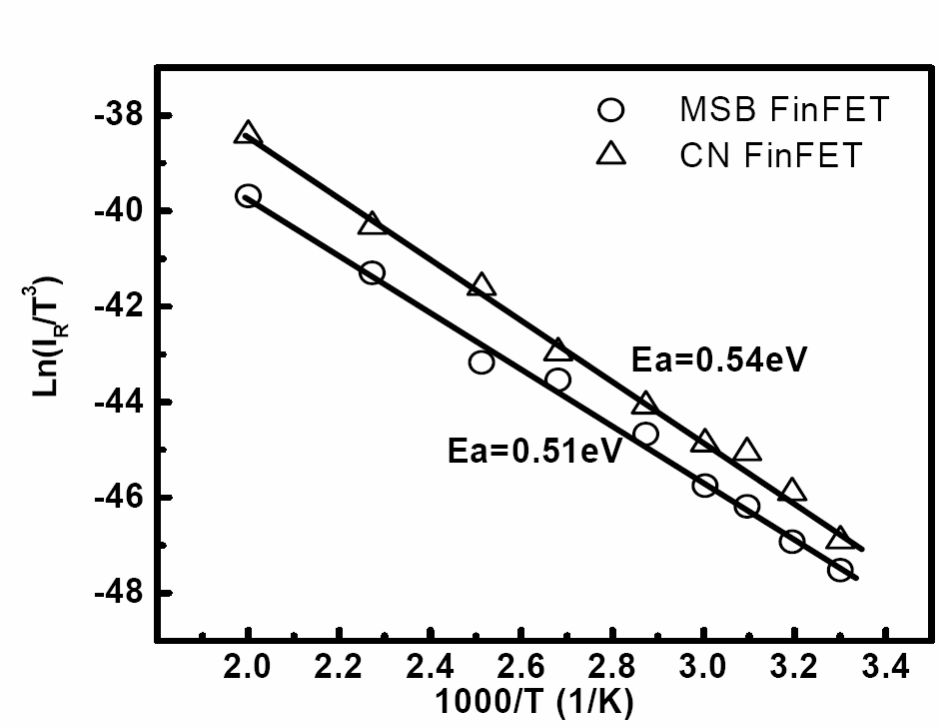

Fig.3-7. Arrhenius plots of I_{off} at V_{gs}-V_{th} = 0.75V and V_{ds} = -1V of the MSB and CN FinFETs with L_g = 65 nm W_f = 60 nm, and T_{Si} = 40 nm.

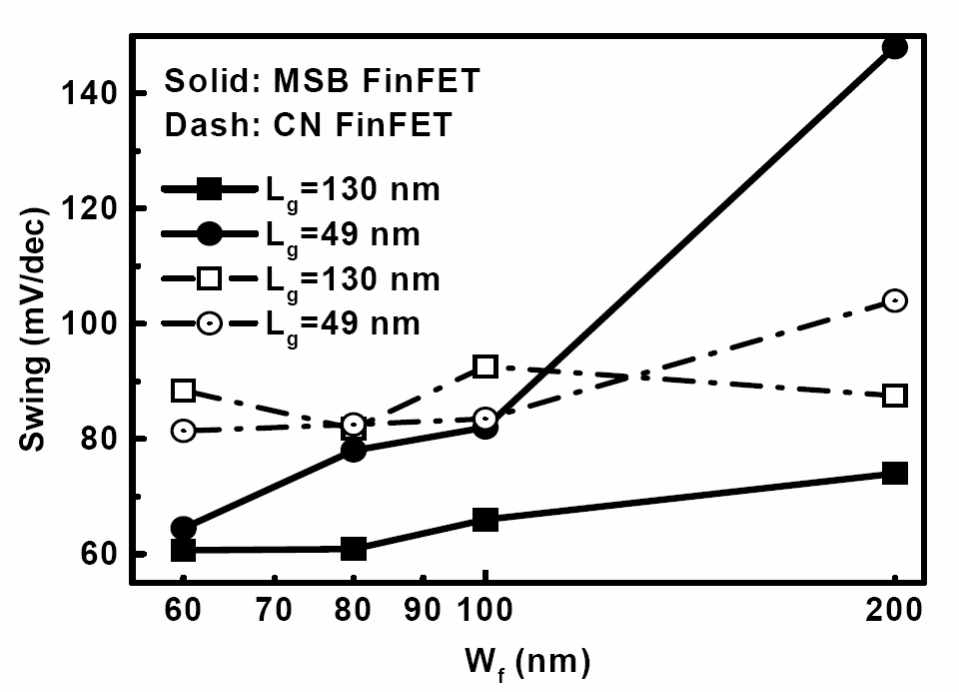

Fig.3-8. Substhreshold swing of MSB and CN FinFETs with different fin thicknesses as L_g = 130 nm and 49 nm.

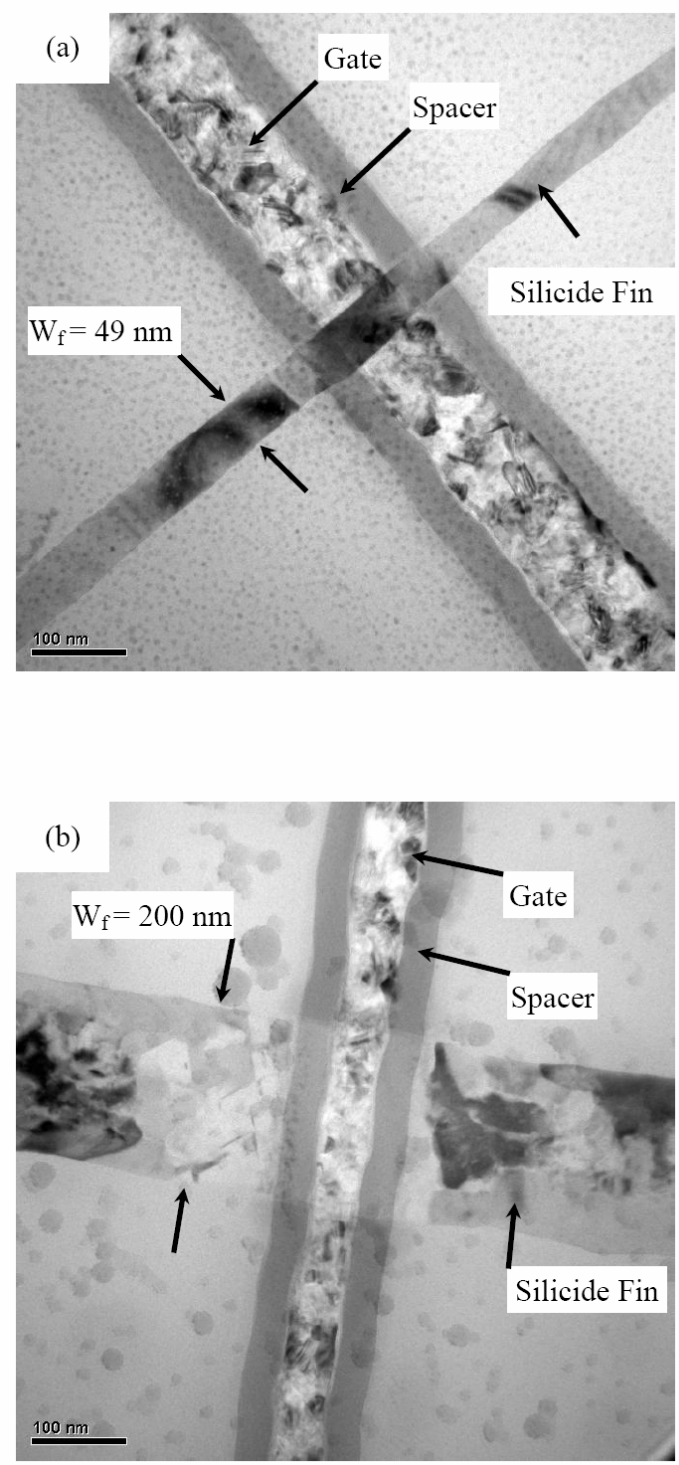

Fig.3-9. Plane view TEM micrographs of the MSB FinFETs with (a) W_f = 49 nm and (b) W_f = 200 nm.

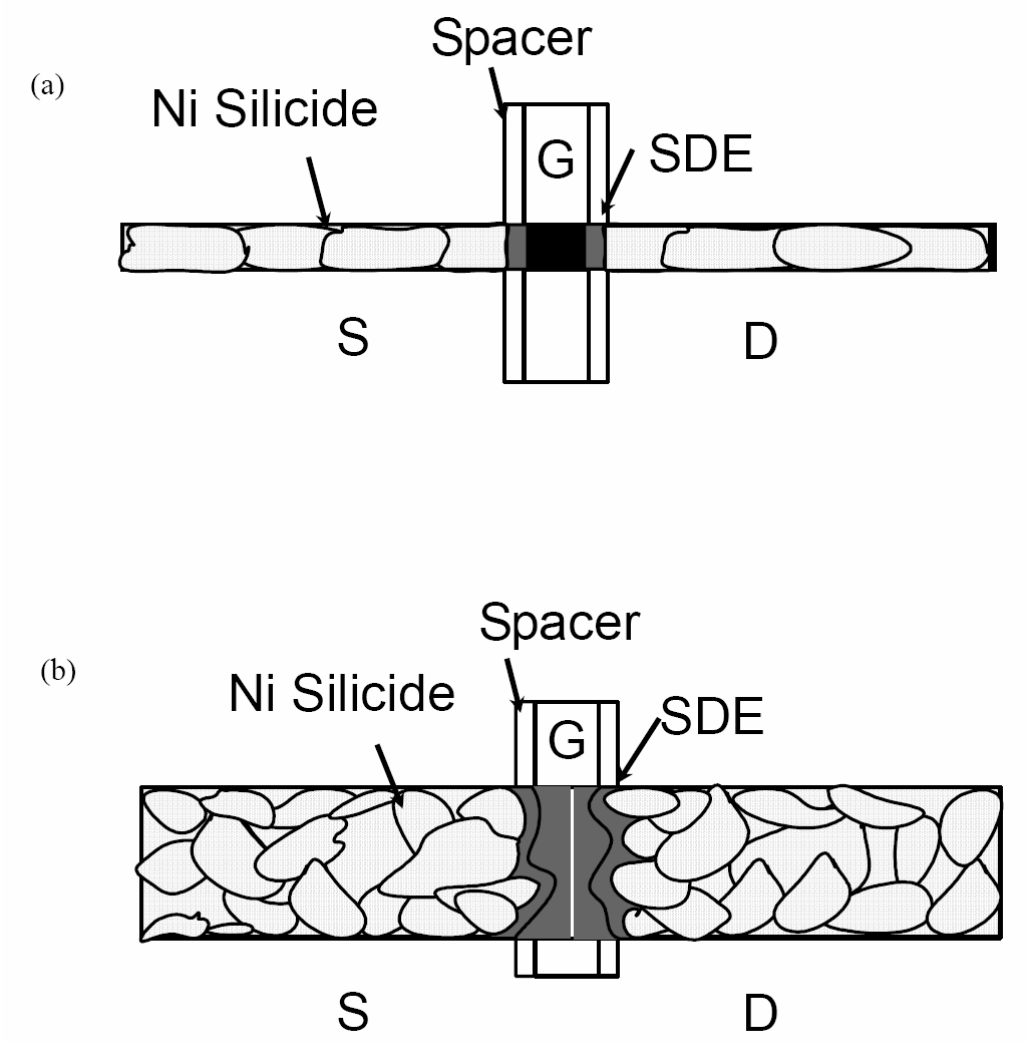

Fig.3-10. Schematic drawing of the grain structure at the S/D region and the SDE profile of the MSB FinFETs with (a) W_f = 49 nm and (b) W_f = 200 nm.

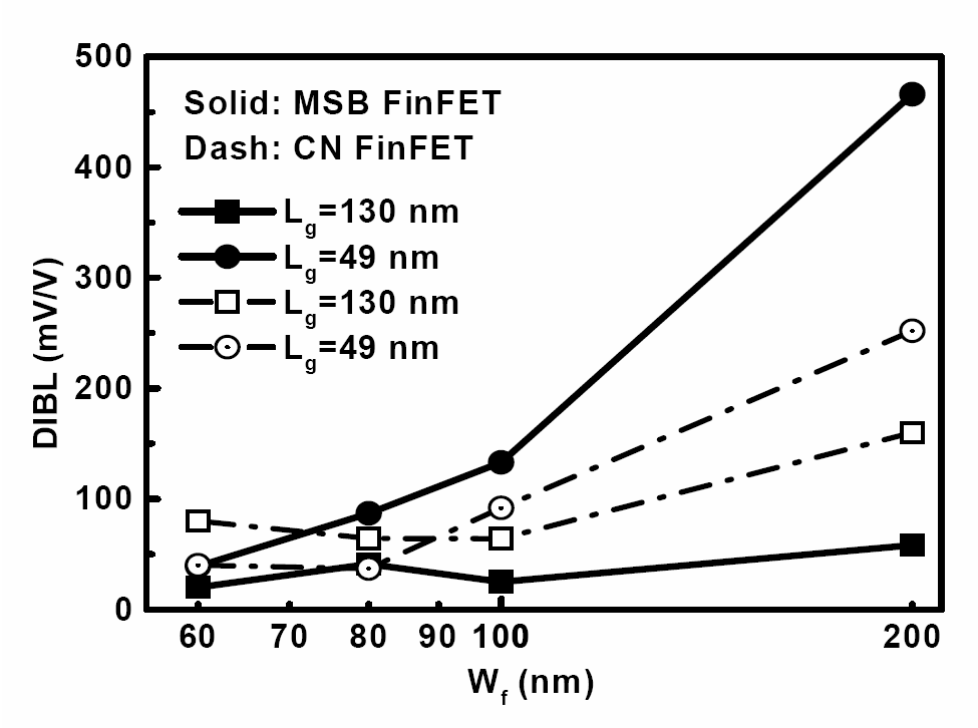

Fig.3-11. Drain-induced-barrier-lowering of MSB and CN FinFETs with different fin thicknesses (W_f) as L_g = 130 nm and 49 nm.

Chapter 7
Summary and Future Works

7-1 Summary

Several important results have been obtained during the execution of this project.

This project proposes a novel high performance MSB FinFETs with several unique features such as fully silicided S/D, ultra-short SDE, defect free S/D junction, and low temperature processing. A two-step Ni-salicide process is developed to completely convert the Si layer at the S/D region to silicide with controlled lateral silicidation. By inserting an ultra-short SDE using the ITS technique, the Schottky barrier is modified so that the barrier width is suppressed at the on-state and is increased at the off-state. In addition, the triple gate wrapping around the fin also effectively diminished the Schottky barrier by the gate-fringing effect. With a 4 nm thick gate oxide, the I_{on}/I_{off} current ratio over 10^9 is achieved, and the room temperature subthreshold swings of 25 nm and 49 nm MSB FinFETs are as low as 83 and 60.4 mV/decade, respectively. These values are close to the theoretical limitations. The I_{on} of the 25nm MSB pFinFET at $|V_d| = |V_g-V_{th}| = 1$ V is higher than 108 μA/μm or 325 μA/μm, depending on the definition of channel width. The I_{on} of 108 μA/μm is lower than the conventional devices. However, if we consider the actual deriving capability of devices with the same layout width, the I_{on} of 325μA/μm will be compatible with that of conventional planar MOSFETs.

Activation energy analysis indicates that the SDE effectively modifies the Schottky barrier, resulting in excellent electrical characteristics. The same activation energy of the low thermal budget MSB FinFETs and high thermal budget CN FinFETs confirms that the MSB junction is very close to the pn junction and the low temperature process of 600°C is sufficient to drive dopants out of silicide. Since the leakage current of drain junction at the off-state is dominated by the surface generation current due to the surface states at the gate oxide/Si and buried oxide/Si interface, it is thus proposed that to further reduce the I_{off} of MSB devices, the interface quality of gate oxide and buried oxide must be improved.

Structural analysis shows that as the fin width becomes larger than the silicide grain size, the multi-grain structure results in a rough front edge of the MSB junction, which in turn degrades the short channel device performance. This result indicates that the MSB process is suitable for FinFETs.

The MSB FinFETFs with narrower fins have better hot carrier immunity (HCI) and could more efficiently restrict the influence of buried oxide quality induced by the V_b. It is not only attributed to the decreasing of the ratio of buried oxide interface to front gate oxide interface but also attributed to the screening effect by the extension of side gate. Moreover, the roughness of SDE regions also affects the HCI, especially for which have wide W_f and short L_g. Besides, in the devices with L_g=49 nm, the uniformity of SDE diffused from the bamboo-like silicide fin relieves the HC degradation in the narrow fin devices. The extrapolated hot-carrier lifetime encourages the MSB nFinFETs as promising sub-10nm devices.

Beyond the 65 nm technology node, it is predicted that the metal gate and high k gate dielectric must be employed to improve the device characteristics continuously. Furthermore, thermal stability between metal gate and high k dielectric is a critical issue because the conventional S/D process requires a high temperature annealing of at least 900°C. Since the MSB process temperature is around 600°C, the thermal stability issue is relaxed and the interfacial layer formation at high k dielectric and Si interface is also reduced. Furthermore, the low thermal budget produced by the ultra-short SDE helps device scale-down. It can thus be considered that the MSB FinFET is a very promising nano device.

Kelvin probe force microscopy is a useful tool for 2D surface potential imaging. For semiconductor material, it is able to be applied to measure dopant type and dopant concentration. Its 2D imaging capability and high spatial resolutions are the advantages for the dopant profiling application in submicron semiconductor devices. However, because the surface potential is sensitive to the surface condition, 2D profiling on a cleaved surface is still difficult at this moment. Additional efforts must be devoted to solve this issue. Therefore, we can not measure the doping profile of the ultra-short SDE of the MSB junction fabricated in this project.

The concept of high performance FSD poly-Si TFTs with ultra-low parasitic resistance fully silicide S/D and ultra-short SDE by simple, low-temperature ITS process has been approved in this chapter. Both n-channel and p-channel FSD TFTs can be fabricated simultaneously. Detailed fabrication process, basic device characteristics, as well as the impact of activation temperature and time of ITS process are all discussed. As the annealing temperature becomes higher than 700ºC, the silicide agglomeration occurs at gate electrode and then the electrical characteristics of FSD TFTs degrade. Device degradation due to dopant deactivation of long activation time is also observed. Since the ITS process does not damage the active layer and most dopants are fast diffuser in Ni-silicide, annealing at 600ºC for 30 sec

is sufficient to produce excellent FSD n and pTFTs. Therefore, the thermal budget is suppressed effectively.

The experimental results also show that the proposed devices not only depict improved turn-on characteristics by successfully reducing the S/D parasitic resistance but also maintain the low off-state leakage current. Superior short channel characteristics are also observed, which is explained by the ultra-shallow SDE fabricated by low thermal budget for FSD TFTs. Therefore, the proposed FSD TFTs are ideally suitable for implementing high-density and high performance driver circuits on the glass panel for AMLCD, AMOLED, and system-on-panel applications.

7-2 Future Works

Although the concept of MSB FinFET has been approved and several import results have been achieved in this project. Some issues are revealed and should be resolved in the future.

The lateral growth of silicide from S/D region toward channel region must be well controlled. In this project, a 2-step annealing technique is employed to control lateral growth. However, the growth rate as well as growth mechanism are still not clear. To further scale down the MSB FinFET, systematical study on lateral growth is necessary.

Contact resistance of S/D junction becomes more and more crucial as the device becomes smaller and smaller. The fully silicidede S/D structure produce a very small S/D contact area so that the contact resistance may be high. The contact resistance of MSB devices must be examined as soon.

The doping profile of the ultra-short SDE region is still unknown. SPM is the most promising technique for dopant profiling of nano-scale area. For KFM method, surface preparation process of cleaved sample must be developed. Nano scale probe tip is the must to obtain nano scale resolution. Carbon nano-tubes may be the most suitable probe material. These techniques have to be setup in the future.

Metal gate and high-k gate dielectric will be integrated into CMOS process eventually. The MSB FinFET has the advantage of low temperature process. The integration with meta; gate and high-k dielectric must be demonstrated in next step. Strained-Si has been employed to provide higher carrier mobility. The effect of strain on MSB FinFET has not been studied and should be investigated.

Nano CMOS is a tough ask. Lots efforts must be paid. This project just demonstrates a novel device concept. Advanced study and suitable modification will proceed immediately.

Chapter 6
Fully Silicided Source/Drain (FSD) Thin-Film Transistors

6-1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFT) are attractive for many applications including the active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode display (AMOLED)[1-2]. In order to integrate peripheral driving circuits on the same glass substrate, a low-temperature process (~600°C) without compromising the device performance should be developed. Therefore, long-term post-ion-implantation annealing which is used to activate dopants and remove implantation damages is carried out using furnace annealing at around 600°C for 12-24 hours after the source/drain implantation. The prolonged process time causes low throughput in the fabrication of conventional (CN) poly-Si TFTs. To overcome this drawback, dopant activation at higher temperature of above 700°C in a rapid thermal annealing (RTA) system has been suggested to improve the activation efficiency and throughput. Nevertheless, the high temperature process is not compatible with low temperature requirement. Thus, poly-Si TFT suffers from a substantial trade-off between performance and throughput.

On the other hands, the use of a thinner active layer to obtain a higher driving current and superior short channel effect has been reported [3-4]. Nevertheless, the high parasitic resistance due to thin source/drain (S/D) regions degrades device performance such as driving capability and effective field-effect mobility (μFE). Especially for the AMOLED, the high S/D parasitic resistance not only reduces the brightness but also enlarge the fluctuations of brightness [5]. To reduce this parasitic resistance, various methods such as raised source/drain, SiGe raised source/drain, and tungsten-clad source/drain techniques were proposed [6-8]. Ni-salicide TFTs structure with process similar to salicide-CMOS was also proposed to reduce the S/D parasitic resistance [9]. However, in order to suppress the leakage current induced by source/drain silicide spiking of salicide TFTs, not only the poly-Si at source/drain cannot be fully consumed to maintain a proper S/D junction, but also an excess mask is needed to block the gate electrode. At the same time, the dopant activation is still an issue in the process of salicide TFTs.

To reduce the S/D series resistance of CN TFTs while more efficiently improves the throughput, the MSB FinFET technology is employed to fabricate a novel fully-silicided S/D

TFTs (FSD TFTs) with fully-silicided source/drain and ultra-shallow source/drain extension (SDE) at the interface of silicide and inverted channel by implant-to-silicide (ITS) technique [10, 11]. Forming the fully silicided source/drain by low temperature self-aligned salicide technique; the parasitic resistance of FSD TFTs can be decreased dramatically. Adding an extension doping in the silicon by ITS technique at about 600°C by rapid thermal annealing (RTA), on the other hand, not only drastically improves contact resistance at the Ni-silicide/poly-Si junction but also abbreviates the source/drain extension length and avoids the silicide spiking effect. This concept has been approved in n- and p-channel FinFETs and the results have been reported from chapter-2 to chapter-4.

In this chapter, we demonstrated that both n-channel and p-channel FSD TFTs can be fabricated simultaneously. The detailed fabrication process of the FSD TFTs will be described. After NH_3 plasma passivation, the characteristics of the proposed FSD TFTs are presented and discussed using conventional (CN) TFTs and simple Schottky barrier (SB) TFTs as comparison. Furthermore, the impact of activation temperature and time of the ITS process on the characteristics of FSD TFTs are also illustrated and analyzed. At last, excellent short channel effect (SCE) will also be shown. The experimental results show that proposed FSD TFT fabricated by low thermal budget ITS technique significantly improves device characteristic and is very attractive for AMLCD, AMOLED, and system-on-panel applications.

6-2 Device Fabrication

Fig.6-1 shows the key fabrication steps for the proposed FSD TFT structure. Briefly, the fabrication was begun by depositing an amorphous Si (a-Si) layer of 50 nm thick at 550ºC in a low-pressure chemical vapor deposition (LPCVD) on 6-inch Si wafers capped with a thermal oxide layer of 1 μm thick. The deposited a-Si layer was then crystallized by a solid-phase recrystallization (SPC) method at 600ºC in N_2 ambient for 24 hours. After patterning the active region, a 45 nm thick CVD gate oxide and an 100nm thick a-Si layer were deposited. The a-Si layer was then patterned to form the gat electrode, as shown in Fig.6-1(a). Then, a 100 nm thick CVD oxide layer was deposited and anisotropically etched to form a sidewall spacer abutting the a-Si gate, as shown in Fig.6-1(b).

Afterwards, a self-aligned silicidation process was performed to form the fully silicided source/drain. A thin Ni layer of 22 nm thick was deposited on the wafer. After a rapid-thermal annealing at 500ºC for 40 sec in N_2 ambient, a wet etching step in a H_2SO_4/H_2O_2 solution was

then used to selectively remove the unreacted Ni. Ni-silicide was also formed on a-Si gate simultaneously, as shown in Fig.6-1(c).

Next, implant-to-silicide (ITS) process was employed to form a shallow dopant extension (SDE) region. BF_2^+ ions were implanted to silicide at 35 KeV for p-channel FSD TFTs (FSD pTFTs) and P_{31}^+ ions were implanted to silicide at 30KeV for n-channel FSD TFTs (FSD nTFTs). Monte Carlo simulation showed that the ions straggle distribution of BF_2^+ and P_{31}^+ are only 8 nm and 9 nm, respectively, which are shorter than the lateral growth of silicide. Dopants were then diffused out of silicide to form an ultra-shallow SDE at the channel-S/D interface by a low temperature rapid thermal annealing process in N2 ambient at temperatures of 600, 650, 700 and 750ºC for 30, 90, and 150 sec. Because of the low solid state solubility of phosphorous and boron atoms in Ni silicide, they diffused out and piled up at the Si/silicide interface to form an ultra-short SDE as shown in Fig.6-1(d). The cross-sectional transmission electron microscopy (TEM) image of the proposed FSD TFTs is shown in Fig.6-2. The fully silicided source/drain region shows a sheet resistance of about 10Ω/□; whereas the nonsilicided one shows a sheet resistance of about 800Ω/□. Since the a-Si gate was also silicided, the gate resistance was also improved by a factor of 40 compared with a nonsilicided a-Si gate. Moreover, the contact resistance between silicide/poly-Si is reduced by the ultra-shallow SDE region. Since the ion implantation process does not damage Si layer directly, the junction would be free of implantation damage and low junction leakage current could be expected.

Typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. For comparison, CN TFTs were fabricated, as schematically shown in Fig.6-3(a). The S/D was implanted after gate patterning followed by activation annealing at 600ºC for 24hrs without silicidation. Simple SB TFTs without the ITS process step were also fabricated. The schematically cross-sectional structure is shown in Fig.6-3(b). In order to improve the I-V characteristics, NH_3 plasma treatment in a plasma-enhanced CVD (PECVD) system at 350ºC for 30 minutes was enforced to effectively reduce trap density and improve interface quality of channel region.

The I-V characteristics of the fabricated devices were measured using a semiconductor parameter analyzer of model Agilent 4156C. Various device parameters, including the threshold voltage (V_{th}), subthreshold swing (S.S.), and field-effect mobility (μ_{FE}) were extracted at a drain voltage of $|V_{ds}|$= 0.1V. The threshold voltage is defined as the gate voltage at which yields a drain current (I_{ds}) of 1 nA/μm. The maximum and minimum values of I_{ds} at $|V_{ds}|$= 5V are designated as I_{on} and I_{off}, respectively.

III. Results and Discussions

A. Basic characteristics of FSD, CN, and SB TFTs

Fig.6-4 compares the typical transfer characteristics of FSD and CN TFTs, both n- and p-channel. The nominal channel length (L) and channel width (W) are 4 μm and 1 μm, respectively. The key device parameters are summarized in Table.1(a). Obvious improvement in device characteristics is obtained for FSD nTFTs in comparison with CN nTFTs. As listed in Table 1, S.S. decreases from 0.68 to 0.45 V/Dec, μ_{FE} increases from 16.9 to 141.5 cm^2/V-sec, and I_{on}/I_{off} ratio increases from 1.4×10^7 to 3.3×10^7. Because of low resistance gate electrode contributed by partial silicide gate structure at FSD nTFTs, V_{th} slightly decreases from 3.6 V to 3.4 V. The similar excellent characteristics of FSD pTFTs are also obtained after NH_3 plasma treatment. For the CN TFTs, the low driving current can be attributed to the parasitic resistance at non-silicided source/drain. On the other hand, the superior driving capability of the FSD devices is resulted from the low series resistance due to the fully-silicided S/D and the low contact resistance of the SDE region. Since the ion implantation process does not damage poly-Si layer directly, the junction would be free of crystalline defects. Therefore, the I_{off} of FSD TFTs is almost identical to (for n-channel) or smaller (for p-channel) than that of the CN TFTs; even though an ultra-low thermal budget (600°C, 30 sec) was used in the ITS process.

Fig.6-5 shows the transfer characteristics of SB nTFT and SB pTFT. The nominal channel length (L) and channel width (W) are 4 μm and 1 μm, respectively. For the SB TFTs, although the source/drain series resistance can be effectively reduced by the fully-silicide S/D structure, low driving current is observed because of the abnormal high carrier injection resistance between silicide and channel at on-state. Moreover, at off-state, abnormal high leakage current attributed to the field emission and thermionic emission of carriers from the drain is also predicted. For example, at n-channel SB TFTs, at off state, holes at drain will inject through the Schottky barrier at interface of silicide/channel and then into channel. Similar phenomena could also be deduced at p-channel devices [12]. The measured as well as extracted key devices parameters are summarized in Table.1(b). To summarize briefly, the proposed FSD devices have superior characteristics to FSD, SB, and CN ones.

B. S/D Parasitic Resistance

Figure 6 shows the typical output characteristics (I_d-V_{ds}) of the FSD and CN nTFTs at

several different gate voltages with W/L = 1μm/4μm. Obviously, FSD TFTs exhibit a higher driving current than CN ones, especially under high gate bias. That is because for large gate bias, the channel resistance becomes smaller; hence, the dominant resistance is the S/D parasitic resistance [9]. The parasitic resistance (R_p) of FSD and CN nTFTs, in the linear region, is also extracted by plotting the width-normalized on-state resistance (R_{ON}) versus channel length (L), as shown in Fig.6-7(a) and (b), respectively [13]. In Fig.6-7(a), all of the R_{ON}-L lines merge at about L= 0.31μm and have a residual value of a gate-voltage independent R_p of 1.35 KΩ-μm. In Fig.6-7(b), the extracted R_p of CN TFTs is 17.63 KΩ-μm, which is about 13 times larger than that of FSD TFTs. As a result, the FSD n-TFTs have smaller R_p and better turn-on characteristics than CN ones.

C. Effects of Activation Temperature

The activation temperature is the most important process parameters to form SDE and to activate dopant in the ITS process. Since there are few reports about the diffusion behaviors of phosphorus and boron in Ni-silicide, a heavy dose of $5x10^{15}cm^{-2}$ was used to study the effect of activation temperature in order to avoid the influence of dopants segregation [14]. The transfer characteristics of FSD n and pTFTs experienced different activation temperatures without NH3 plasma treatment are shown in Fig.6-8(a) and (b), respectively. The extracted device parameters of FSD n and p TFTs are listed in Table.2(a) and (b), respectively.

The devices activated at 600ºC and 650ºC result in the best performance for both FSD n and pTFTs. The slight deviation of V_{th}, S.S., μ_{FE}, as well as I_{on}/I_{off} current ratio may come from the process deviation. By increasing the RTA temperature to higher than 700ºC, the degradation of absolute value of V_{th}, S.S., and μ_{FE} are clearly observed. However, the off-state current (I_{off}) slightly decreases with the increase of RTA temperature. It is well known that the I_{off} of TFT device is dominated by the quality of the S/D junction [15]. The continuous reduction of Ioff implies that the higher activation temperature results in deeper diffusion length and higher dopant concentration of SDE.

Since the S/D integrity is maintained, the device degradation mechanism may be related to the gate electrode. It is known that the thermal stability of Ni-silicide is not as good as that of Ti-silicide or Co-silicide [16, 17]. Annealing at temperature higher than 700ºC usually results in agglomeration of Ni-silicide [10]. Moreover, the agglomeration temperature of Ni-silicide on poly-Silicon is lower than that on oxide layer. It is postulated that the agglomeration of silicide at gate electrode may degrade device performance. Fig.6-9(a)-(d) shows the surface morphology of the FSD TFTs inspected by scanning electron microscope

(SEM) after ITS process and annealing at different temperatures from 600~750ºC. The agglomeration of silicide at gate region occurs when the activation temperature is above 700ºC; while the silicide at S/D region keeps continuous. This observation may be explained by the different thermal stress at gate region and S/D region [18, 19]. The vertical structures at gate region and S/D region are different. At gate region, Ni-silicide is stacked on un-reacted poly-Si layer, TEOS gate oxide, Si active layer, and buried oxide; while the Ni-silicide at S/D region is stacked on buried oxide only. The thermal stress is quite different at high temperature. It is possible that the thermal stress at gate region is higher than that at S/D region; therefore, thermal stress induced agglomeration may occur at gate region earlier.

The un-agglomeration of silicide at S/D region is consistent with the non-degradation of I_{off}. Since the a-Si gate was not doped before silicide formation, once the silicide at gate region agglomerated, gate voltage cannot be applied to the gate region uniformly. Therefore, higher gate voltage is required to form inverted channel at where the silicide film is broken. That's why the absolute value of V_{th} increases for both n and pTFTs with the increase of activation temperature. The degradation of S.S. and μ_{FE} can also be explained by the same reason.

We can have a short summary now. A 600ºC or 650ºC RTA is sufficient to form excellent FSD pTFTs and nTFTs simultaneously. The fully silicided S/D region can sustain thermal annealing up to 750ºC. If gate electrode is also fully silicided, the sustainable process temperature is expected to be 750ºC at least. For the application of LTPS TFTs, 600ºC is chosen to be the annealing temperature of the ITS process.

D. Effects of Activation time

Fig.6-10 (a) and (b) show the transfer characteristics of FSD n and pTFTs with different RTA activation times at 600ºC, respectively. The extracted parameters are listed in Table.3. For FSD pTFTs, an activation annealing at 600ºC for 30 sec is sufficient to achieve excellent performance and the on/off current ratio can be higher than 10^7 without using hydrogenation treatment. However, it should be noted that device performance degrades with the increase of activation time. One of the possible causes is dopant deactivation [14]. In poly-Si, grain boundaries act as sinks for impurity segregation and also trap carriers at defects due to incomplete atomic bonding. The thermal equilibrium concentration for dopants increases with temperature and the major driving force for deactivation is dopant supersaturation. In the ITS process, the heavy dose not only forms ultra shallow SDE but also fills grain boundaries in the short activation time. More activated dopants fill grain boundaries with the longer

activation time and dopants deactivate during cool-down from activation temperature to room temperature. Dopant deactivation reduces the concentration of the SDE, and therefore, can explain the degradation of some device performances including V_{th}, S.S., μ_{FE} and I_{on}.

For FSD nTFTs, similar to FSD pTFTs, ultra shallow SDE is also formed after a short activation time of 30 seconds. Unlike boron, phosphorus has small diffusivity [20]. A 30 sec activation may be insufficient to form intact SDE. By increasing activation time, dopant diffuse out of silicide and all of the Ni-silicide grains are surrounded by SDE. Therefore, some device characteristics such as S.S. and Ioff are improved. For the reduction of mobility and on-state current (I_{on}), dopant deactivation is still a possible reason. Although Ion slightly reduces, the I_{on}/I_{off} current ratio increases with the increase of activation time. This is explained by the obvious reduction of Ioff. According to the above discussion, 30 seconds RTA is a suitable activation time for both FSD n and pTFTs.

E. Short Channel Behavior

The short channel effect (SCE) of the FSD and CN TFTs (both n and p-channel) as evaluated by the threshold voltage drop with channel length reduction is shown in Fig.6-11. The V_{th} here is defined as the differences between the V_1 of short channel devices and the V_{th} of a 10 μm device. Because of long dopant diffusion length ascribed to long-time activation process and fewer grain boundary in the short channel devices, V_{th} of CN nTFTs obviously reduces from 7.11 to 2 V and that of CN pTFT reduces from -8.1 to -3.9 V as channel length decreases from 10 μm to 1.2 μm [21]. In the FSD TFTs, the excellent short channel effect attributed to not only the shorten SDE by the low thermal budget ITS process, but also the SDE/silicide interface trap density [22].

6-4 Conclusions

The concept of high performance FSD poly-Si TFTs with ultra-low parasitic resistance fully silicide S/D and ultra-short SDE by simple, low-temperature ITS process has been approved in this chapter. Both n-channel and p-channel FSD TFTs can be fabricated simultaneously. Detailed fabrication process, basic device characteristics, as well as the impact of activation temperature and time of ITS process are all discussed. As the annealing temperature becomes higher than 700ºC, the silicide agglomeration occurs at gate electrode and then the electrical characteristics of FSD TFTs degrade. Device degradation due to dopant deactivation of long activation time is also observed. Since the ITS process does not damage

the active layer and most dopants are fast diffuser in Ni-silicide, annealing at 600ºC for 30 sec is sufficient to produce excellent FSD n and pTFTs. Therefore, the thermal budget is suppressed effectively.

The experimental results also show that the proposed devices not only depict improved turn-on characteristics by successfully reducing the S/D parasitic resistance but also maintain the low off-state leakage current. Superior short channel characteristics are also observed, which is explained by the ultra-shallow SDE fabricated by low thermal budget for FSD TFTs. Therefore, the proposed FSD TFTs are ideally suitable for implementing high-density and high performance driver circuits on the glass panel for AMLCD, AMOLED, and system-on-panel applications.

Table.1 Electrical parameters of (a) FSD & CN TFTs and (b) SB TFTs.

(a)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
FSD nTFT	3.4	0.45	141.5	3.3E7
FSD pTFT	-6.3	0.72	55.2	2.2E7
CN nTFT	3.6	0.68	16.9	1.4E7
CN pTFT	-6.4	0.85	10.7	1.3E5

(b)

	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
SB nTFT	5.1	0.97	49.6	3.1E4
SB pTFT	-9.3	0.55	21.4	2.63E6

Table.2 Electrical parameters of (a) n-channel and (b) p-channel FSD TFTs after different annealing temperatures from 600ºC to 750ºC for 30sec without NH_3 plasma treatment.

(a)

RTA Temperature (ºC)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
600ºC	7.18	1.6	70.6	1.77E6
650ºC	4.7	1.4	49.9	2.13E6
700ºC	16.96	1.88	7.3	5.41E5
750ºC	>20	2.18	0.4	1.66E4

(b)

RTA Temperature (ºC)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
600ºC	-6.7	1	33.6	1.52E7
650ºC	-8.5	1	35	6.8E6
700ºC	-15.3	1.2	9.7	8.6E5
750ºC	-19.5	2.8	2.9	1.1E5

Table.3 Electrical parameters of (a) n-channel and (b) p-channel FSD TFTs after different activation times from 30 sec to 150 sec at 600ºC without NH_3 plasma treatment.

(a)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
30	7.2	1.6	70.6	1.8E6
90	6.2	1.5	57.6	3E6
150	8.3	1.2	33.9	1E7

(b)

RTA Time (sec)	$V_{th,lin}$ (V)	S.S. (V/Dec)	μ_{FE} (cm^2/ V-sec)	I_{on}/I_{off} @V_{ds}=5V
30	-6.7	1	33.6	1.5E7
90	-7.1	1	40.1	1.2E7
150	-10.6	1.3	20.7	5.2E6

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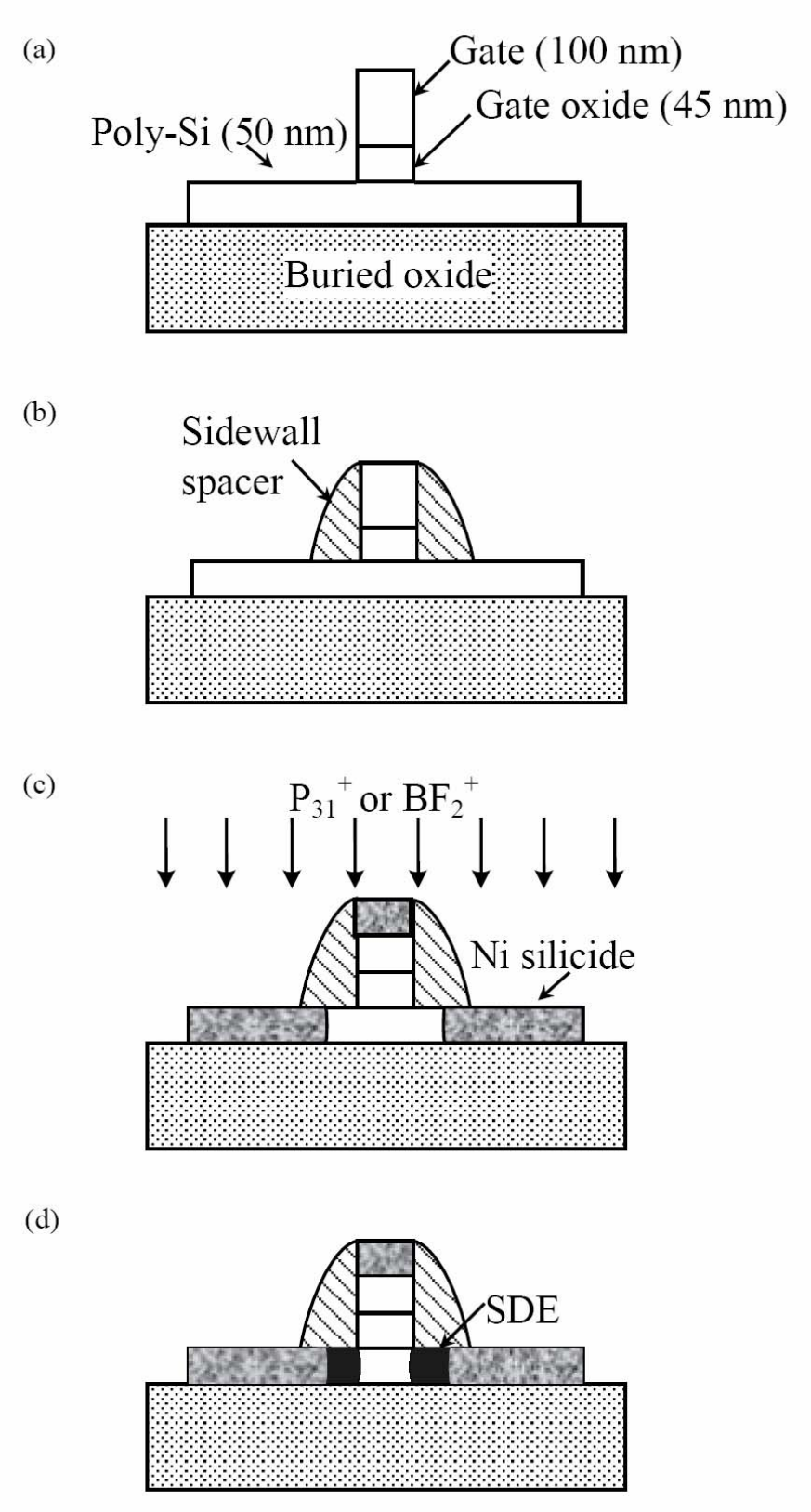


Fig.6-1. Key fabrication steps of the proposed FSD TFTs.

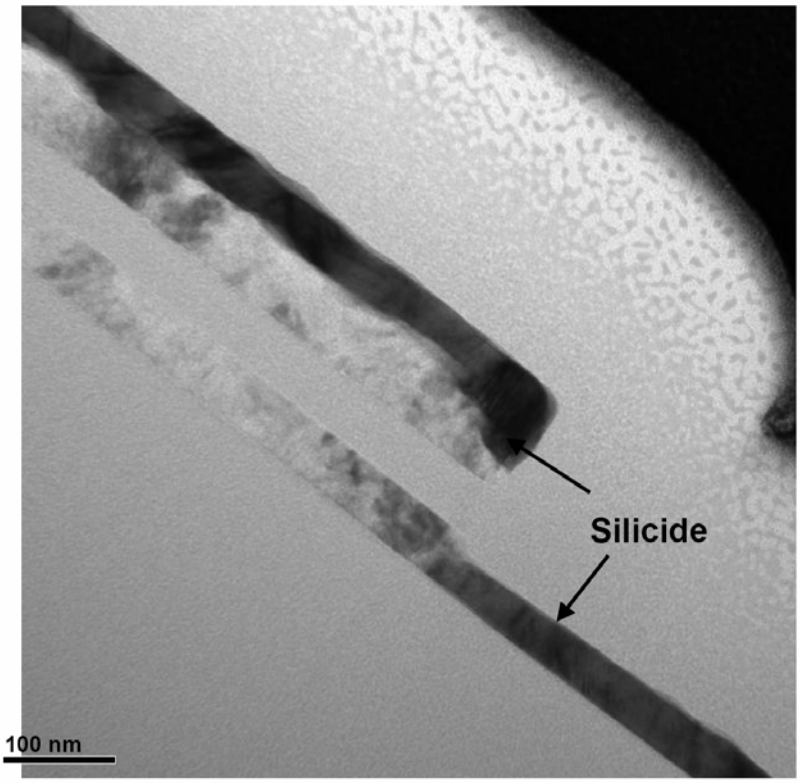


Fig.6-2. Cross-sectional transmission electron microscopy (TEM) micrograph of the proposed FSD TFTs.

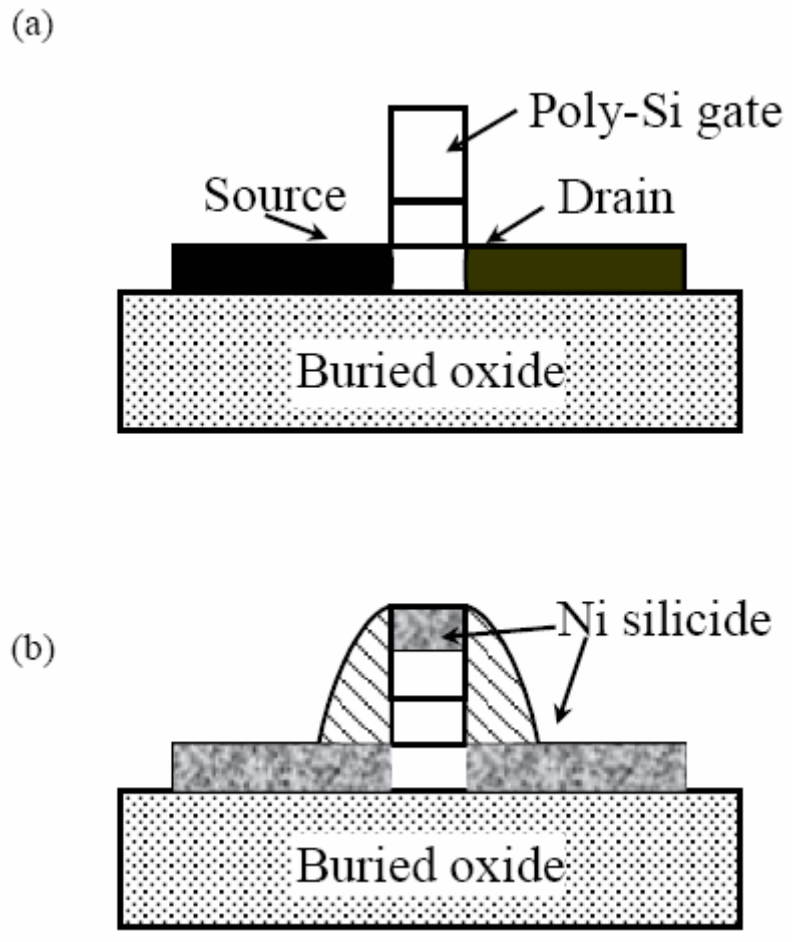
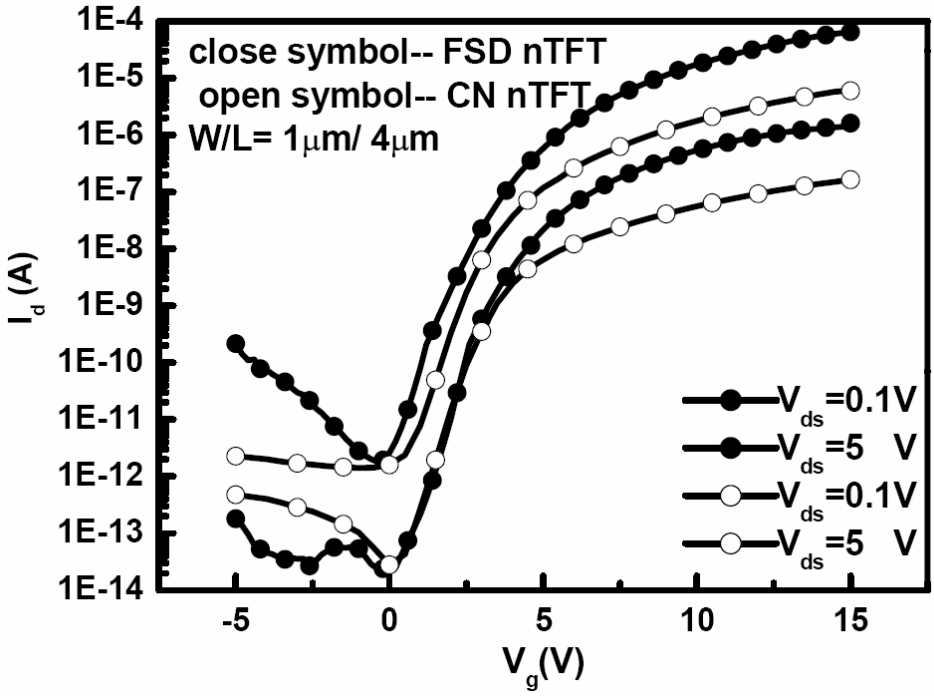


Fig.6-3. Schematic cross-sectional drawings of (a) CN TFTs, (b) SB TFTs.

(a)



(b)

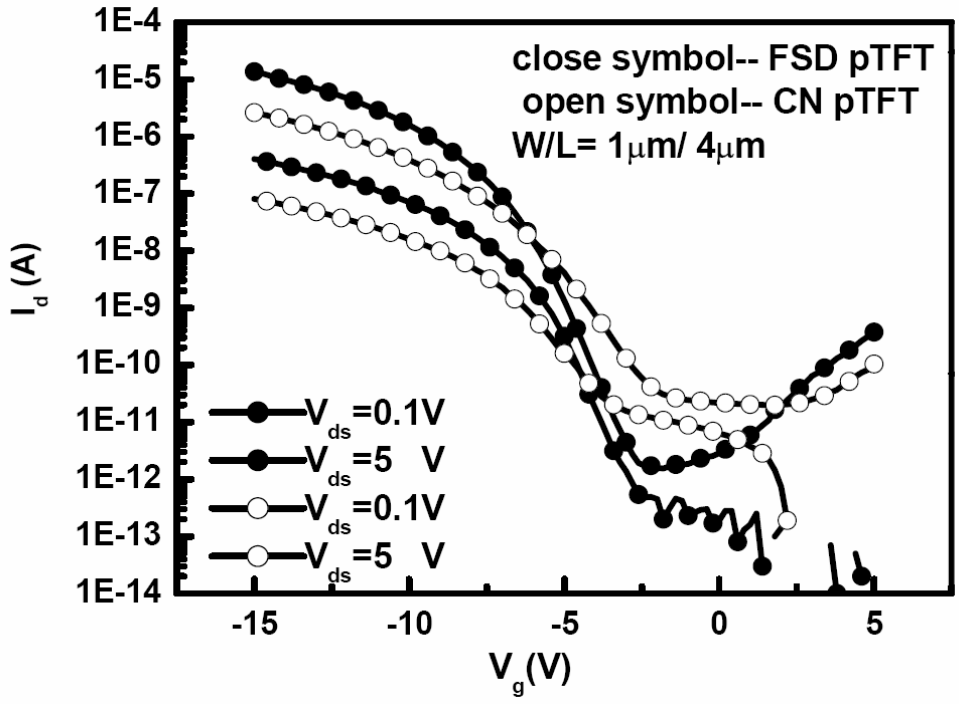


Fig.6-4. Transfer characteristics of (a) n-channel (b) p-channel FSD and CN TFTs after NH3 plasma treatment.

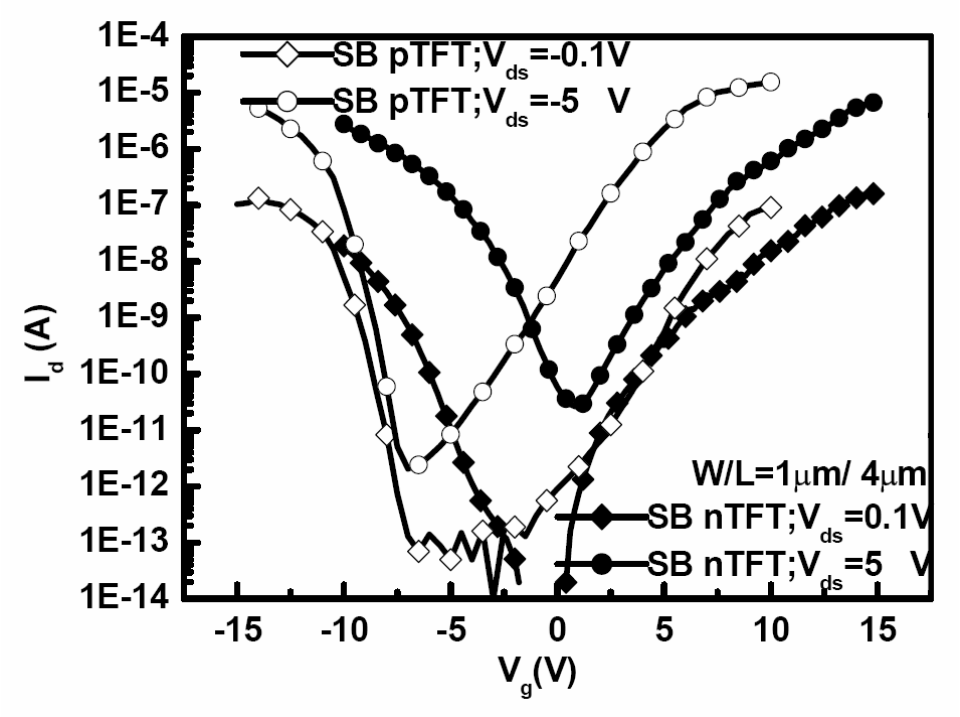


Fig.6-5. Transfer characteristics of SB n- and p-channel TFTs after NH3 plasma treatment.

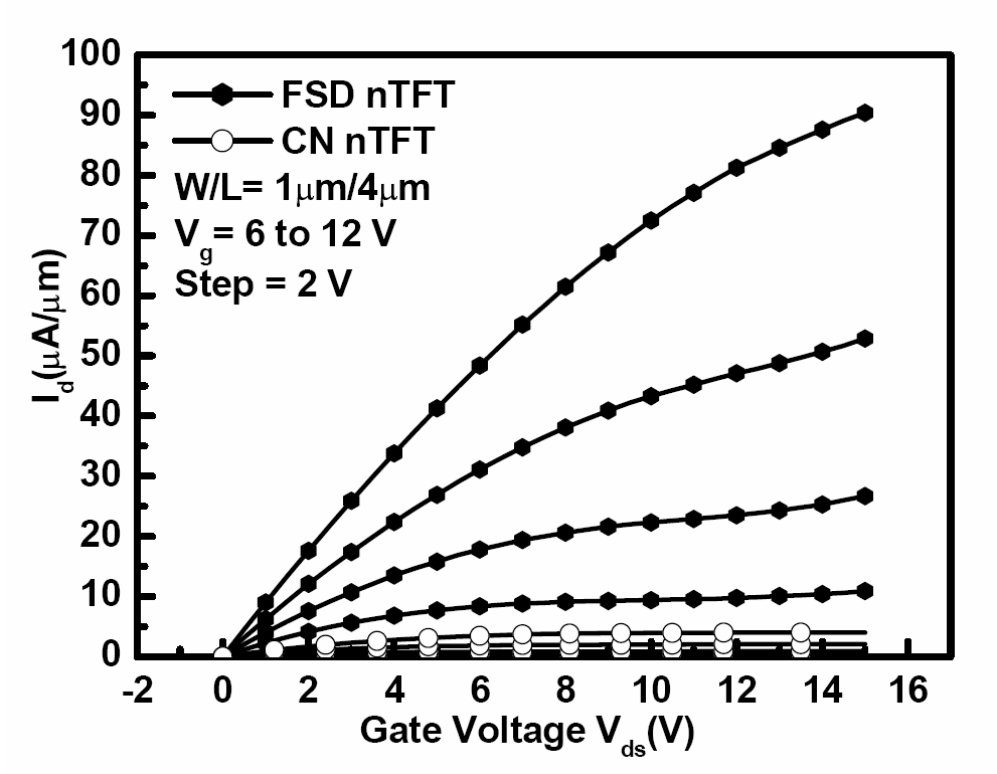


Fig.6-6. Typical output characteristics (Id-Vds) of the n-channel FSD and CN nTFTs after NH3 plasma treatment.

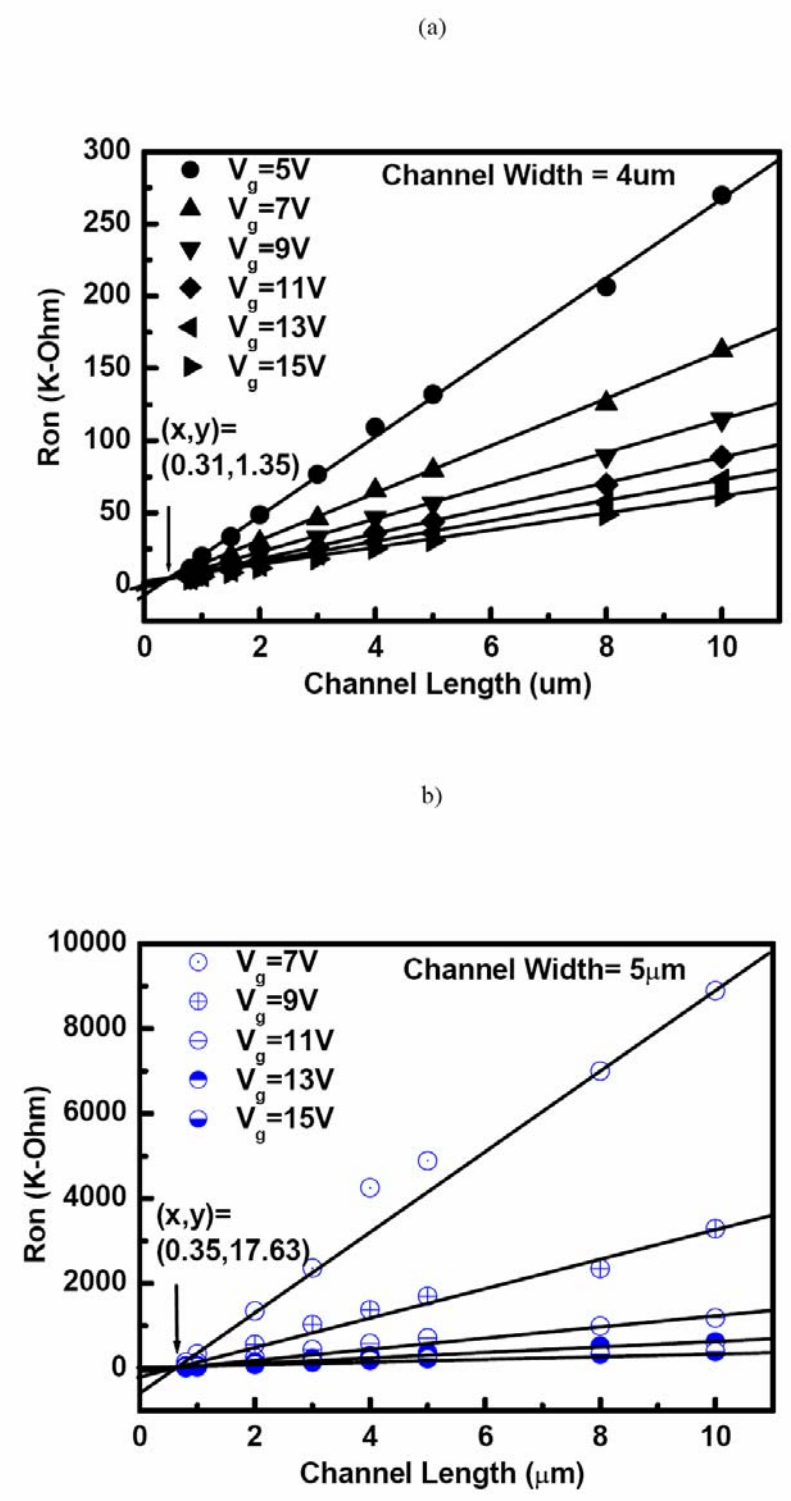
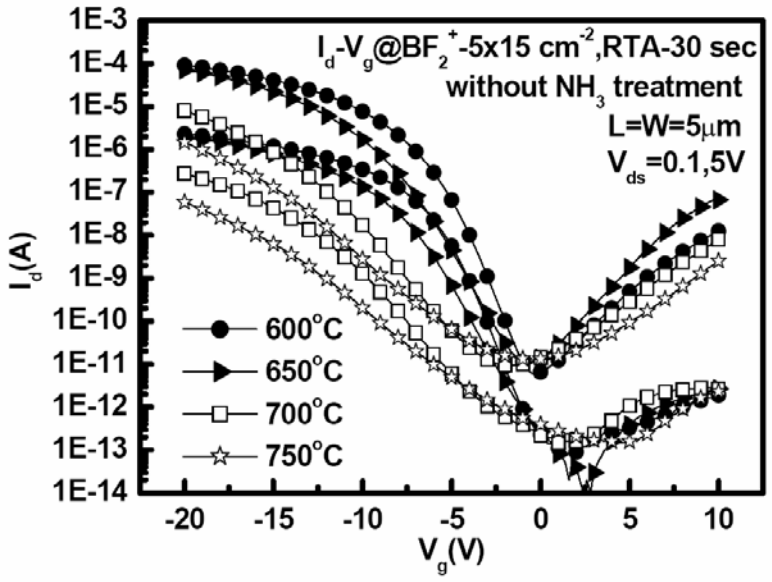


Fig.6-7. Channel width-normalized on-state resistance (RON) as a function of channel length (L) of (a) FSD nTFTs and (b) CN nTFTs.

(a)



(b)

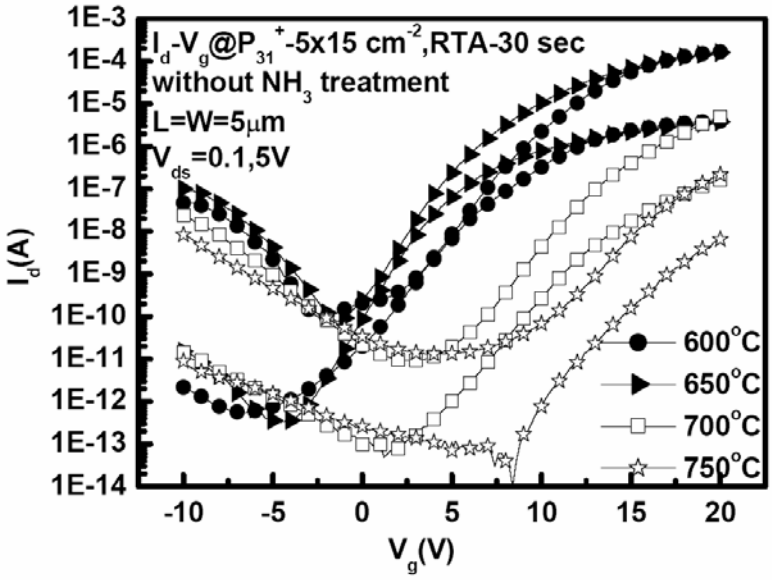


Fig.6-8. Transfer characteristics of (a) n-channel and (b) p-channel FSD TFTs experienced different activation temperatures without NH3 plasma treatment.

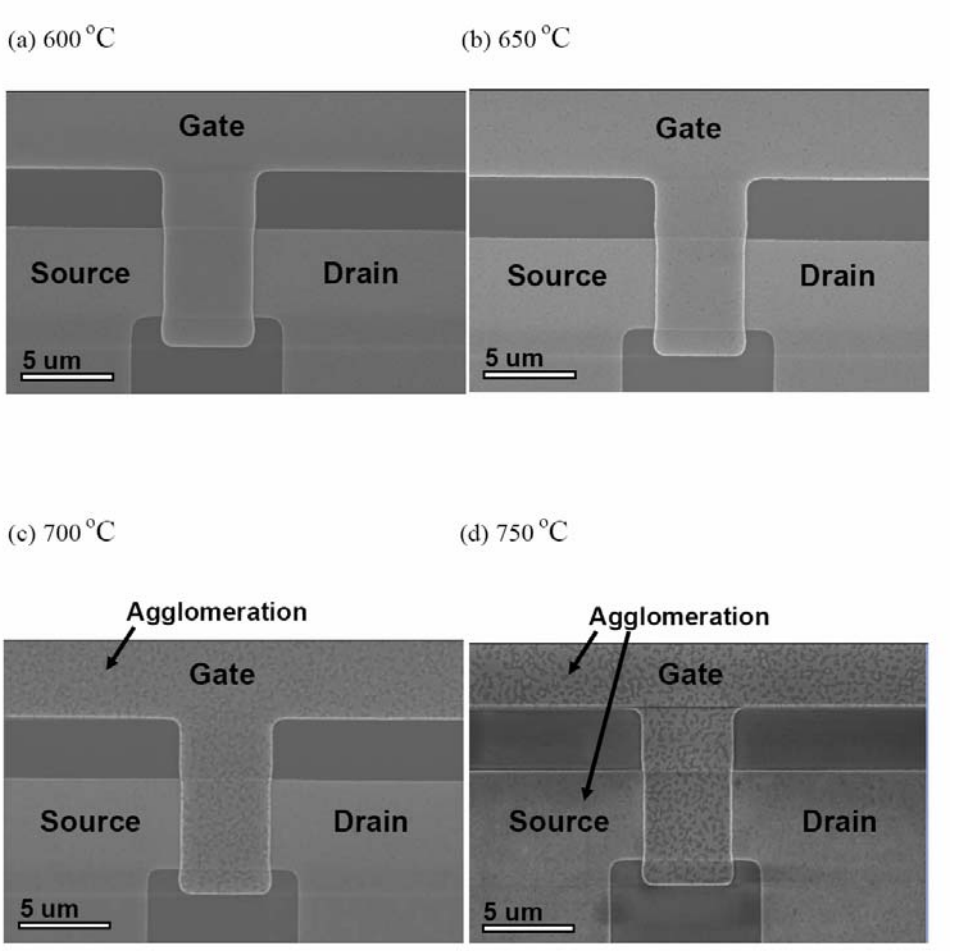


Fig.6-9. Plane view scanning electron microscope (SEM) micrographs of FSD TFTs after annealing at different temperatures : (a) 600ºC, (b) 650ºC, (c) 700ºC, and (d) 750ºC.

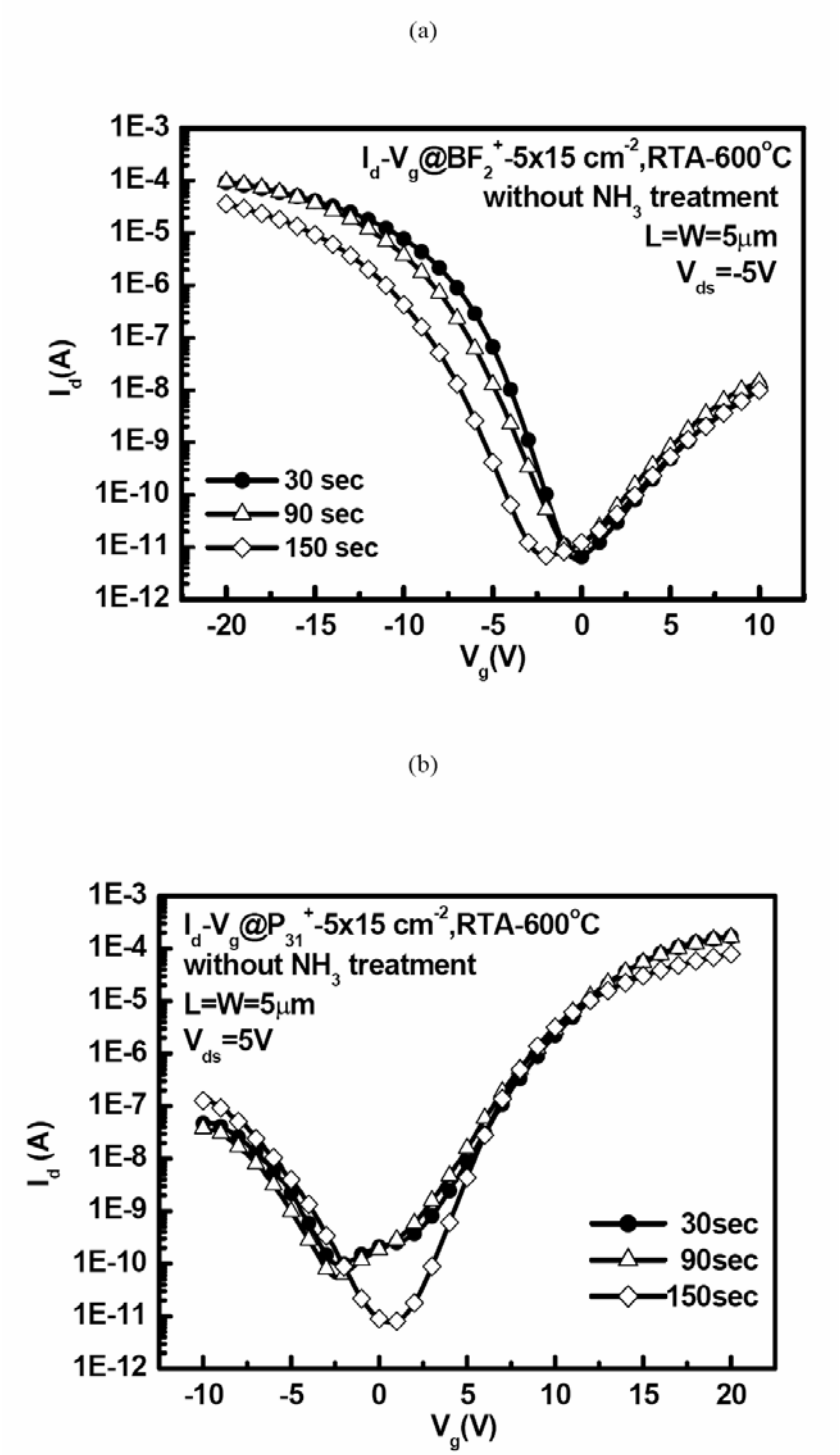


Fig.6-10. Transfer characteristics of (a) n-channel and (b) p-channel FSD TFTs experienced different activation time without NH3 plasma treatment.

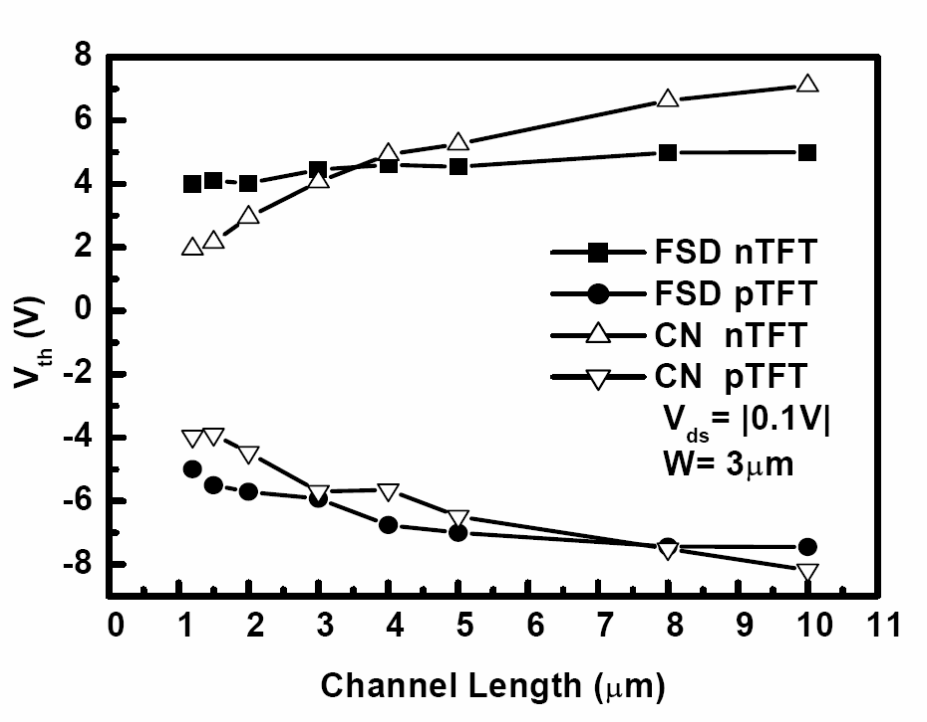


Fig.6-11. Threshold voltage (Vth) roll-off of FSD and CN TFTs. The channel width (W) is fixed at 3 μm.

Chapter 5
Dopant Profiling by Kelvin Probe Force Microscopy

5-1 Introduction

As stated in chapter-2, a dopant profiling technique which can measure dopant distribution in a nano scale region is needed to characterize the ultra-SDE of the MSB devices. Conventional techniques, such as secondary ion mass spectroscopy (SIMS), have been used as a popular dopant profiling technique or a long time but it lacks lateral resolution capabilities. Some attempts have been made to realize lateral dopant profiling by applying scanning probe microscopy (SPM) techniques [1]. However, resolution is limited by the required minimum capacitance. Kelvin probe force microscopy (KFM), which has potential to be a tool for two-dimensional (2D) dopant profiling with high resolutions, is another one possible methodology. KFM can image surface potential by sensing the potential differences between the probe and the sample surface. Since the work function of tip is known, the work function of surface under test can be detected. In the case of semiconductor materials, work functions depend on dopant type and dopant concentrations. For this reason, it is possible to infer the dopant profile by measuring the surface potential [2].

5-2 Measurement Principle of KFM

Fig.5-1 is the schematic diagram of the KFM measurement system. The principle of KFM is to measure the electric interaction force by applying an ac voltage between a conductive tip and sample surface. In order to keep the distance between tip and sample constant, we employ the tip oscillating at frequency ω_1, near the resonant frequency ω_0. By sensing the variation of ω_1, the distance can be controlled.

Furthermore, an ω_2 frequency signal is still applied between the tip and the sample for the sensing the surface potential. Assuming that there are no electric charges and surface potential $-V_s$ on the sample surface, the electrostatic force is given by

$$F = \frac{1}{2}\frac{\partial C}{\partial z}V^2 = \frac{1}{2}\frac{\partial C}{\partial z}\left[\left(V_{dc} - V_s\right) + V_{ac}\sin\omega_2 t\right]^2$$

,where V_{dc} (V_{ac}) is the dc (ac) components of the applied voltage between the tip and the sample, C is the effective capacitance, z is the distance between them, and ω2 is the frequency

of the applied ac voltage. By expanding the terms, the force can be written by

$$F = \frac{1}{2}\frac{\partial C}{\partial z}(V_{dc} - V_s)^2 + \frac{\partial C}{\partial z}\frac{V_{ac}^{\ 2}}{4} + \frac{\partial C}{\partial z}(V_{dc} - V_s)\cdot V_{ac}\sin\omega_2 t - \frac{\partial C}{\partial z}\frac{V_{ac}^{\ 2}}{4}\cos(2\omega_2 t)$$

Three components, V_{dc}, ω_2, $2\omega_2$, are in the force equation. The ω_2-component of the force depends on the dc voltage V_{dc} and surface potential $-V_s$; the $2\omega_2$-component depends only on the ac voltage V_{ac} and the capacitance C between the tip and the sample. Using a lock-in amplifier, it is easy to obtain the amplitude of the $2\omega_2$ component. During KFM measurement, the V_{dc} must be modulated in order to nullify the output signal of the lock-in amplifier. In other words, the relation V_{dc}-V_s=0 is always maintained by controlling V_{dc}, and the surface potential -V_s is just V_{dc} exactly [3].

Fig.5-2 shows a p-n junction measured by KFM [4]. Fig.5-2 (a) is a simplified diagram of the probe and the sample connection. When no voltage is applied, the Fermi level of the semiconductor sample and the tip is aligned as shown in Fig.5-2 (b). For KFM measurement, the vacuum level difference is reduced to zero by adjusting the applied V_{dc}. When the tip is over an n-type region, the dc bias (V_m-V_n) is applied to nullify the vacuum level difference as shown in Fig.5-2 (c). When the tip is over a p-type region, the dc bias (V_m-V_p) is applied as shown in Fig.5-2(d). Thus, the surface potential difference between the two regions is obtained as the applied bias difference.

5-3 Experiments and Results

5-3-1 Sample preparation

A p-type silicon wafer was patterned by typical photo-lithography technique, then As^+ ions were implanted at 20KeV or 50 KeV to various dosages. After implantation, photoresist was removed, and a 250 nm thick SiO_2 was deposited in a plasma-enhanced chemical vapor deposition system to passivate the sample surface. Samples were then annealed at 950°C in N_2 ambient for 30 min to activate the n-type dopants. The passivation oxide was removed before KFM measurement.

5-3-2 Surface treatment

Since the KFM method detects the surface potential of sample, it is sensitive to surface condition. Therefore, the surface treatment before KFM measurement was studied a first. Initially, the sample was dipped into a 1% HF solution for about 20 sec to remove the native

oxide, and ultrasonically oscillated in acetone for 3 min. Then, it was immersed in D.I. water. The potential image of the sample is shown in Fig.5-3(a). The image measured immediately after HF dip is shown in Fig.5-3(b). Compared to the previous one, the potential image is blurred which possibly result from the residual fluorine bond on the sample surface.

We also attempted to measure the samples with oxidized surface. Fig.5-4 (a) shows the potential image of sample after rapid thermal oxidation at 900°C for 1 min. Fig.5-4(b) shows the potential image of sample after immersing in H_2SO_4 : H_2O_2 3 : 1 solution at 100°C for 10minutes. The quality of potential image of these two samples is also very poor. The clearest image can be obtain is the sample which was dipped in diluted HF, oscillated in acetone, and the rinsed in D. I. water.

5-3-3 PN junction potential difference

Fig.5-5(a), (b), and (c) shows the potential image of the sample with As^+ implantation at 50 KeV to a dose of $2x10^{15}$, $2x10^{14}$, $2x10^{13}$ cm^{-2}, respectively. The bright lines are un-implanted p-type regions, and the dark regions are As^+ ions implanted n-type regions. The brighter color represents the higher potential, so we can differentiate between the two type regions by the potential height. The potential difference is 138, 73, and 30 mV with respect to the dosage of $2x10^{15}$, $2x10^{14}$, $2x10^{13}$ cm^{-2}.

In Fig.5- 6 (a), (b), and (c), there are the surface potential images of 20 KeV energy and $2x10^{15}$, $2x10^{14}$, $2x10^{13}$ cm^{-2} dose, and the potential difference are 133, 73, 34 mV, respectively.

Fig.5-7 are the SIMS profiles of the implanted samples. The implant condition is at 20 KeV to a dose of $2x10^{15}$ and $2x10^{13}$, respectively. We can find that higher implant dose caused higher surface dopant concentration. It is corresponds to the KFM results shown above. For this reason, we can measure the dopant profile qualitatively by means of KFM surface potential difference.

5-4 Conclusions

Kelvin probe force microscopy is a useful tool for 2D surface potential imaging. For semiconductor material, it is able to be applied to measure dopant type and dopant concentration. Its 2D imaging capability and high spatial resolutions are the advantages for the dopant profiling application in submicron semiconductor devices. However, because the surface potential is sensitive to the surface condition, 2D profiling on a cleaved surface is still

difficult at this moment. Great efforts must be devoted to solve this issue. Therefore, we can not measure the doping profile of the ultra-short SDE of the MSB junction fabricated in this project.

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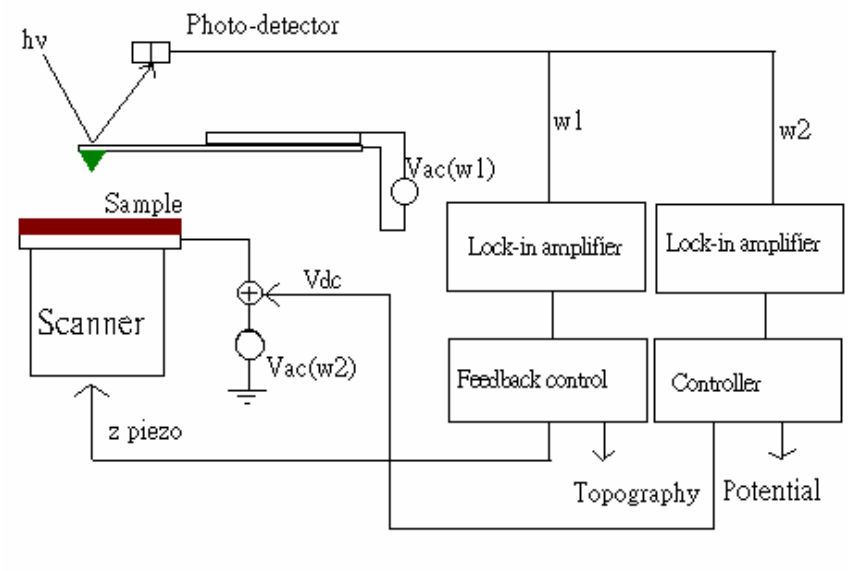


Fig.5-1. Schematic diagram of Kelvin probe force microscope system.

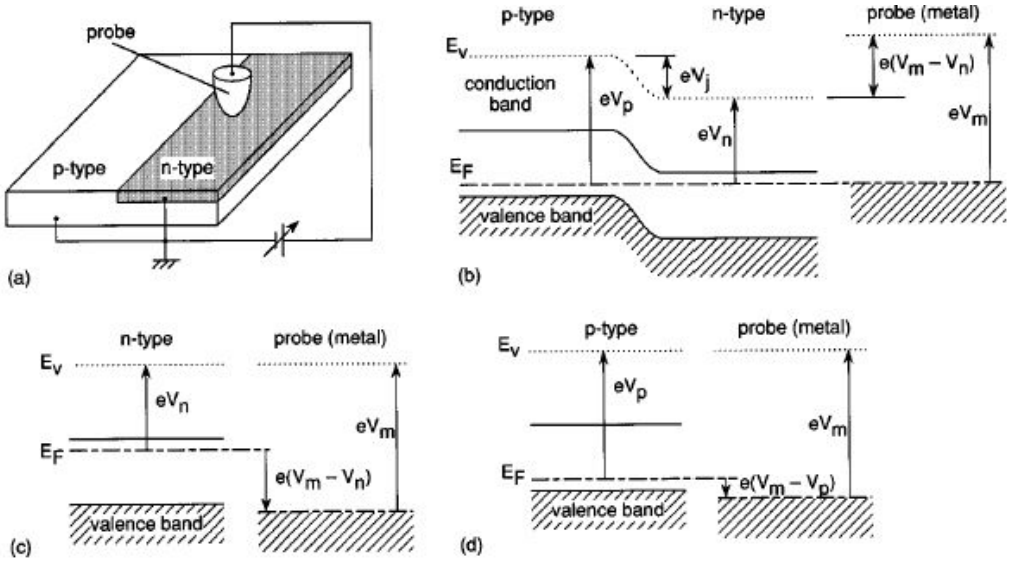
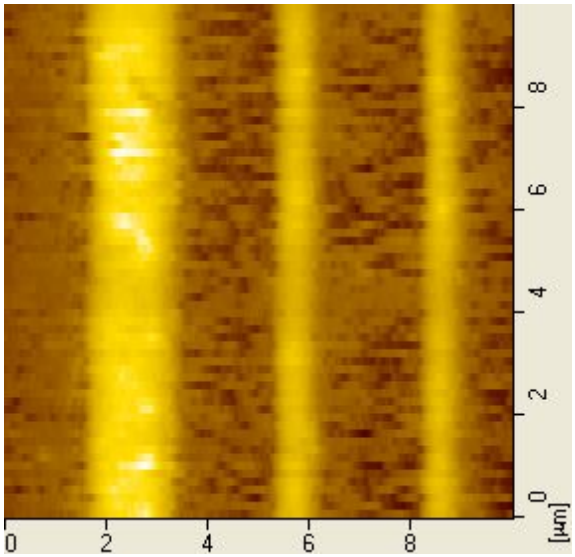
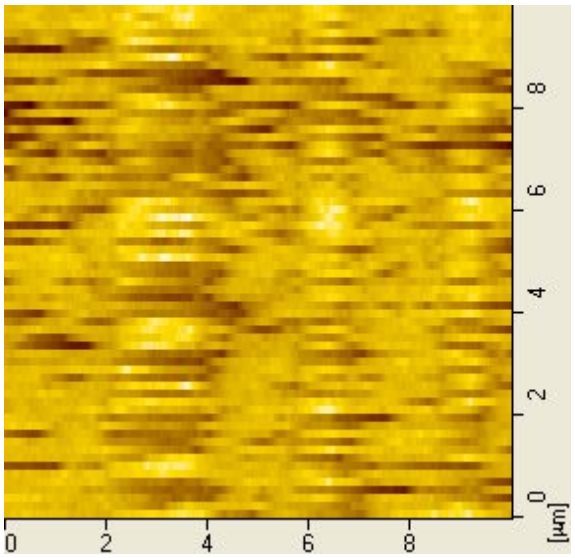


Fig.5-2. Energy diagram of pn junction imaging. E_F: Fermi level, E_p: vacuum level, eV_p: work function in p-type region, eV_n: work function in n-type region. (a) Simplified diagram of the connection. (b) Energy band diagram when no bias applied. (c) Over an n-type region. (d) Over a p-type region. [4]

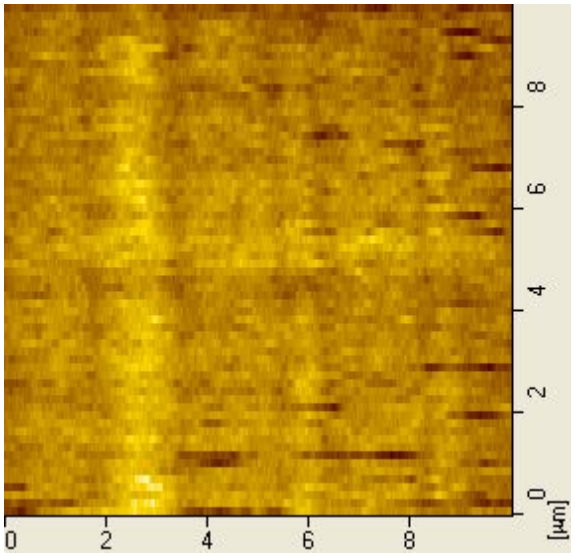


(b)

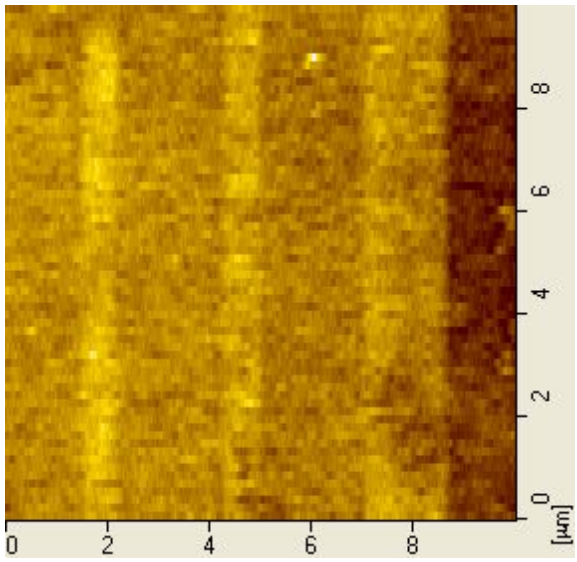


(b)

Fig.5-3. (a) The image of sample dipped HF, oscillated in acetone, and posited in D. I. water. (b) The image of sample only dipped HF.



(a)



(b)

Fig.5-4. (a) The image of the sample with RTO oxide. (b) The image of the sample with chemical oxide.

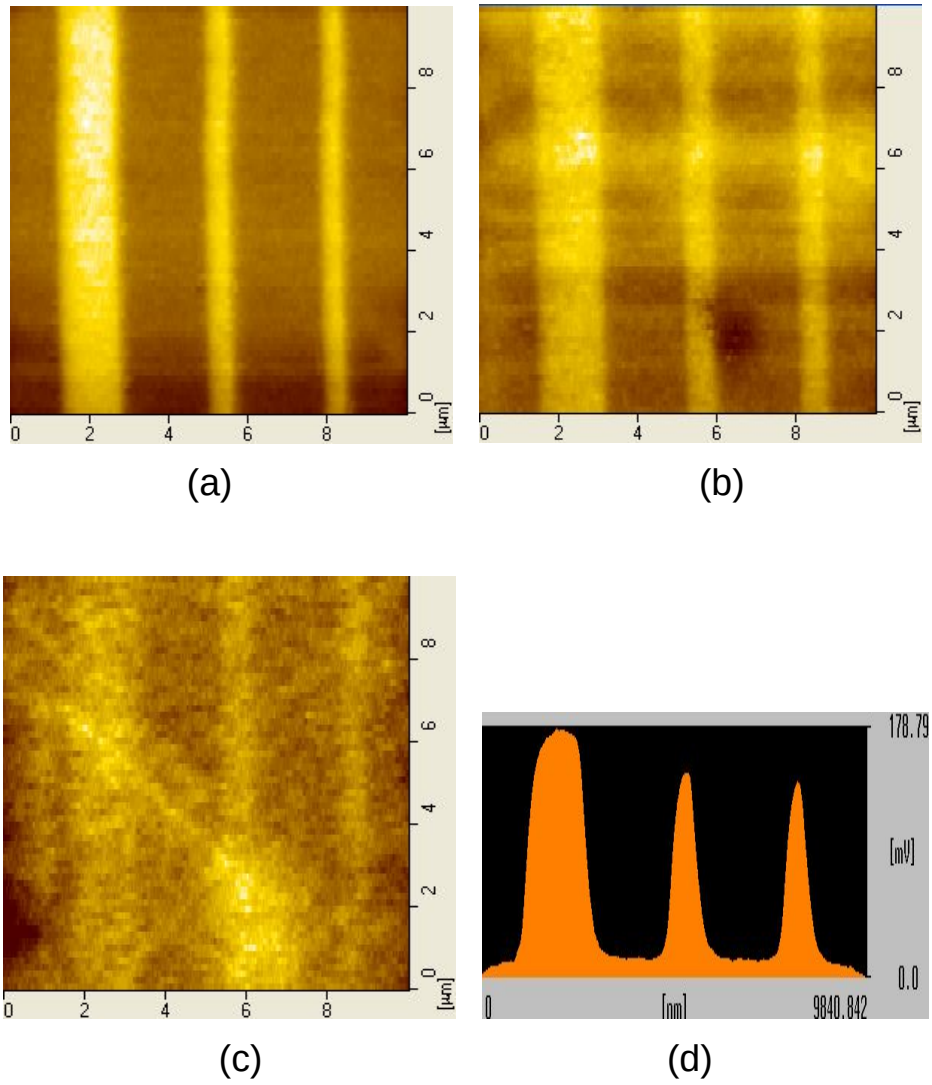
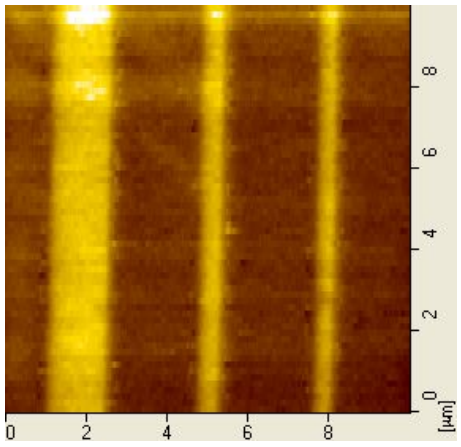
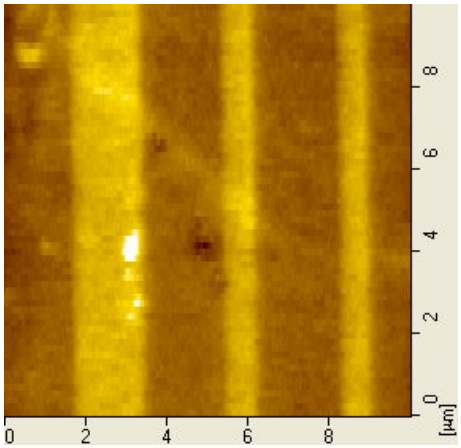


Fig.5-5. The potential image of the samples with implantation energy at 50 KeV and dose of (a) $2x10^{15}$, (b) $2x10^{14}$, (c) $2x10^{13}$ cm^{-2}. (d) shows the surface potential across the sample shown in (a).



(a)



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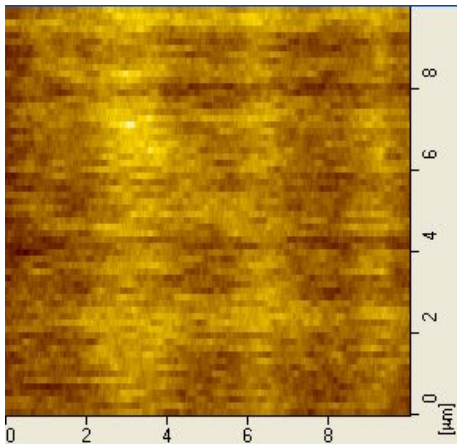
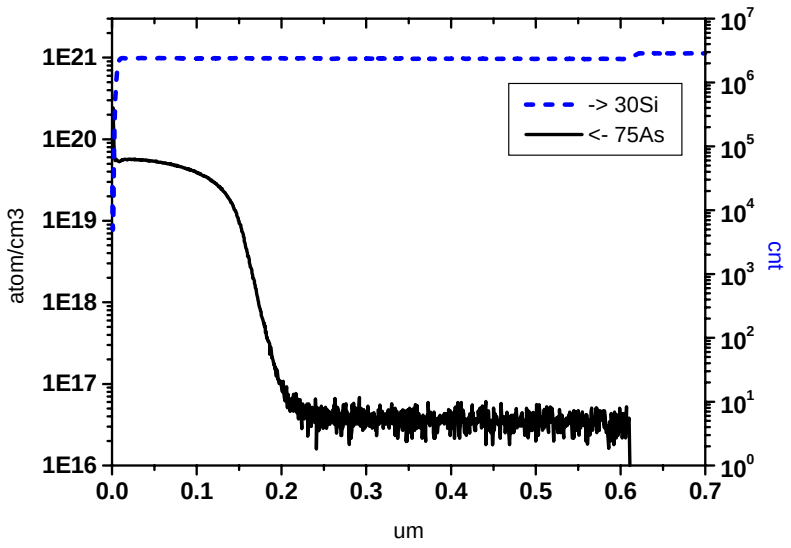
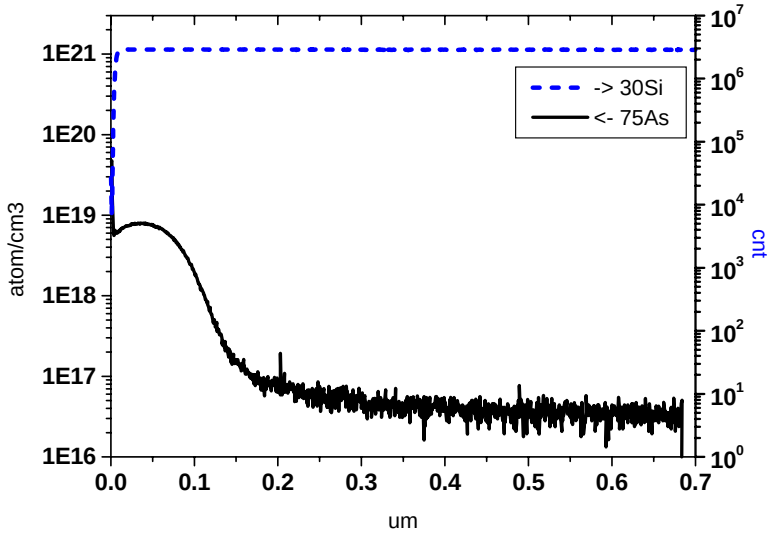


(c)

Fig.5-6. The image of the samples with implant energy 20 KeV and dose (a) $2x10^{15}$, (b) $2x10^{14}$, (c) $2x10^{13}$ cm^{-2}.



(a)



(b)

Fig.5-7. The SIMS profiles of the samples of implant energy 20 KeV and dose (a) $2x10^{15}$, (b) $2x10^{13}$ cm^{-2}.

Chapter 4
Hot Carrier Effect of Modified Schottky Barrier FinFETs

4-1 Introduction

The high performance modified SB FinFET (MSB FinFET) with ultra-short source/drain extension (SDE) at the interface of silicide and inverted channel has been reported in the previous two chapters. Adding an extension doping in the silicon drastically improves Schottky limit for Ion by thinning and reducing the SB at the source/body junction at on-state and shows significantly lower I_{off} than the conventional SB devices because of the high and broad Schottky-barrier at drain/body junction at off-state. However, when the devices are scaled down, MSB FinFETs also suffer from hot-carrier (HC) effects. For the prediction of the long-term reliability of the proposed tri-gate MSB FinFETs; therefore, the HC reliabilities of the proposed devices are firstly investigated for various bias stress conditions and device dimensions. The superior HC reliability of the devices with narrow fins is confirmed. It is also pointed out that the proper balance of gate electrical field in the ultra narrow is the major reason of extraordinary hot carrier immunity in MSB FinFET with long gate length (L_g). On the other hand, as the L_g decreases, the quite exceedingly uniform of the SDE region in the narrow Fins is also regarded as the possible dominative mechanism of excellent HC reliability of MSB pFinFETs.

4-2 Hot Carrier Effect of p-channel MSB FinFETs

4-2-1 Experiments

Fabrication process details for the MSB pFinFETs have already been reported in chapter-2. The cross sectional TEM images of the Si fin with Wf= TSi= 40 nm is shown in Fig.4-1(a). The schematic cross-sectional structure is shown in Fig.4-1(b). To investigate the HCE of the proposed MSB pFinFETs, the worst-case bias condition for HC stress was determined first. The variation of device parameters was found to be larger when the gate voltage was equal to the drain voltage (V_g=V_d), compared to V_g=1/2V_d. Therefore, all the stress experiments were performed at V_g=V_d for a wide range of stress biases at 300K. Degradation in device performance parameters under several V_g=V_d stress conditions were then tracked over time, for MSB pFinFETs with two different gate lengths (L_g=49 nm and 130 nm) and several fin widths (200 nm to 60 nm). The variations of the maximum

transconductance (G_m) and drain current (I_{lin} at V_g=1V) were measured in the linear region (V_d=50mV). Besides that, the electric field simulations of cross-sectional Si fins were also obtained for MSB pFinFETs of various W_f/T_{Si} ratios [1]. The roughness at the interface of silicide/channel of device with W_f=40 nm and 200 nm were also demonstrated by planar view TEM micrographs.

4-2-2 Results and Discussion

The stress time dependence plots of G_m variation and I_{lin} shift for the MSB pFinFETs with L_g=49 nm and different W_f stressed at V_g=V_d=-2.3 V were shown in Fig.4-2 (a) and (b). Perhaps due to the sharp Si fin corner effect and mechanical stress induced by S/D silicide; therefore, the HCI of MSB pFinFETs is slightly worse than that of conventional fully depleted SOI devices. Hole trapping at the interface of SiO_2/Si were still suggested to dominate the HC degradation, similar to the conventional bulk and fully depleted SOI pMOSFETs [2, 3]. We also discovered that the degradation of MSB pFinFETs with wider W_f was more serious than that of devices with narrower W_f. As shown in Fig.4-3 (a), HC lifetimes of the devices with different L_g (49 and 130 nm) and various W_f were plotted against the reciprocal of the drain voltage. For MSB pFinFETs, lifetimes were defined as the extrapolated time necessary to reach 10% degradation in Gm at V_g=V_d stress conditions, because that the G_m shift was the most degradable devices parameters among the shift of I_{lin}, V_{th} and G_m. As shown of Fig.4-3 (a), MSB pFinFETs with both L_g=49 and 130 nm were able to meet the 10-yr lifetime requirement under normal operating condition at V_d= 1 V [1]. The comparisons of operation voltages to 10-yr lifetime between the devices with two different L_g (49 nm and 130 nm) and different Wf were also displayed in Fig.4-3 (b).

It is surprising that when the W_f decreases from 200nm to 60 nm, the operation voltages of the proposed devices with L_g= 130 nm to 10-yr lifetime could increase steeply from 1.33V to 1.67V. Similar degradation of the proposed devices with L_g= 49 nm is from 1.04V to 1.61V. In order to explain the HC degradation dependence on W_f, the cross-sectional electrical field simulations of Si fins with different ratio of W_f/T_{Si} were suggested. First, the equipotential line plots of the proposed devices with T_{Si} =40 nm and two different W_f (200nm and 40 nm) with the same V_g (-2.3 V) were simulated by 2D numerical simulator [4]. As the gradient of equipotential line in the Si fin increases, which means that the electric field is enlarged, and then more energetic hot carriers can degrade the gate oxide. Obviously, as the fin wider, almost the energetic hot carriers are driven toward the top gate oxide as shown in Fig.4-4 (a). Nevertheless, in the narrow one, the lateral gate voltages relax the electric field in the Si fin

apparently, as shown in Fig.4-4 (b). That is because of the different direction of electric fields induced by the top gate voltage and the lateral gate voltage. As this result, the electric field and HC degradation of narrower fin is distinctly smaller than that of wide ones are confirmed.

Moreover, in order to explain the different HCI degradation rate of the devices with different L_g (49 nm and 130 nm) when the W_f decreases from 200 nm to 100 nm, the roughness of SDE was also proposed to affect the HCI, and therefore, the TEM and schematic images of the MSB pFinFET with two W_f (40 and 200 nm) are displayed in Fig.4-5 (a), (b) and (c).

Whereas the W_f becomes wider, not only the silicided fin changed from bamboo to multi-grain structure, the roughness of the Silicide/Si interface but also increases. At the same time, the uniformity of SDE length of the wider devices also degraded more than that of the narrower ones. Furthermore, the comparisons of the SDE distribution between the multi-grain and bamboo silicide fins were schematically shown in Fig.4-5 (c). For example, as shown in wide fins in Fig.4-5 (c), because of the channel length of A'A is shorter than that of BB', the lateral electric field in A is higher than that in B, and then lower the HCI of the wide devices. Therefore, the W_f dependence of operation voltages to 10-yr lifetime was apparently revealed especially for the device with shorter L_g because of the stronger lateral electrical field than that with longer L_g.

4-3 Hot Carrier Effect of n-channel MSB FinFETs

4-3-1 Experiments

Fabrication process details for the MSB nFinFETs have also been reported in chapter-2. The worst bias condition for hot-carrier stress at V_b=0 V was determined at first. The maximum transconductance (G_m) degradation and V_{th} shift were found to be the largest when the front gate voltage equals to the drain voltage. Therefore, devices with different W_f were stressed at V_g=V_d=3.2V and biased at various V_b. Three dimensional numerical simulator was also used to understand the electric field distribution [5].

4-3-2 Results and Discussion

Fig.4-6 shows the G_m degradation and the threshold voltage shift (V_{th}) of the MSB nFinFETs induced by hot-carrier stress at V_b=0Vand V_g= V_d= 3.2V. It is known that the energetic electrons trapped at the gate oxide/Si interface or in the gate oxide generated by impact ionization near drain is the major reason of positive Vth shift and Gm degradation. The

DC hot-carrier lifetime is projected in Fig.4-7. The failure criterion used here is 10% change of G_m. The MSB nFinFETs with narrower W_f could balance the electric field in Si fin induced by the front gate and result in better HCI. On the other hand, for FD SIMOX SOI devices, the back interface degradation can also influence the front channel operation owing to the poor buried oxide quality and interface-coupling effect. The degradation of Gm and V_{th} shift of the MSB nFinFETFs induced by hot-carrier stress at various V_b from 5 to -30 V is shown in Fig.4-8 (a) and (b), respectively. For devices stressed at V_b=0V, Gm degrades and V_{th} shifts to positive direction, which indicates that hot electrons are trapped in the front gate oxide and interface. Nevertheless, for devices stressed at negative V_b, the hot holes are accelerated toward the buried oxide; then, the G_m and V_{th} change toward the reverse direction relative to those of devices stressed at V_b=0 V.

The effects of back gate bias and W_f on HCI are investigated in this work. Fig.4-9(a) shows the variations of G_m of MSB nFinFETFs stressed at V_b=-20V. For the devices with W_f=40nm and stressed at V_b=-20V, the maximum variations of positive G_m shift are smaller and turn around faster than those of devices with W_f=200nm and stressed at the same conditions. This observation indicates that the effect of V_b for narrower devices is slighter than that for wider ones. Fig.4-10 shows the simulated electric field of devices with W_f= 40 nm and 200nm. For devices with 40 nm W_f, the influence of electrical field induced by back gate is smaller than that of 200 nm devices. In the narrower devices, not only the reduction of the ratio between the buried oxide interface to front-gate oxide interface but also the strong shielding effect attributed to the D_{ext} obviously terminate the penetration of field lines from the back gate under the Si fins. Therefore, the maximum positive G_m variations for the devices with different W_f as shown in Fig.4-9(b) also demonstrates that the narrower devices have greater ability than the wider ones to restrict the back bias effect during hot-carrier stress.

4-4 Conclusions

The hot-carrier effects of MSB FinFETFs with different W_f, V_b, and D_{ext} were investigated in this chapter. The MSB FinFETFs with narrower fins have better HCI and could more efficiently restrict the influence of buried oxide quality induced by the V_b. It is not only attributed to the decreasing of the ratio of buried oxide interface to front gate oxide interface but also attributed to the screening effect by the extension of side gate. Moreover, the roughness of SDE regions also affects the HCI, especially for which have wide W_f and short L_g. Besides, in the devices with L_g=49 nm, the uniformity of SDE diffused from the

bamboo-like silicide fin relieves the HC degradation in the narrow fin devices. The extrapolated hot-carrier lifetime encourages the MSB nFinFETs as promising sub-10nm devices.

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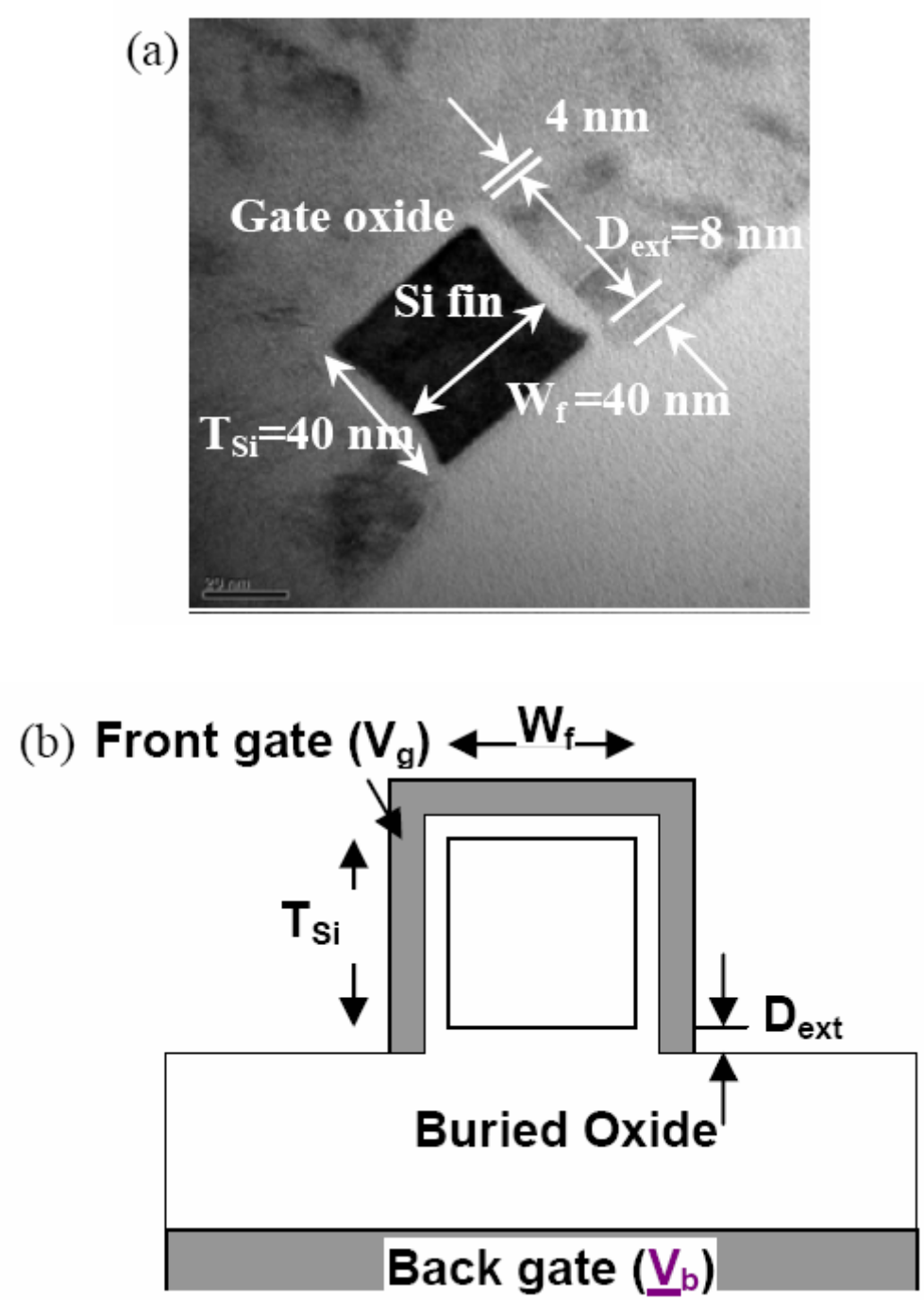


Fig.4-1. The cross-sectional (a) TEM picture and (b) schematic structure of MSB FinFET.

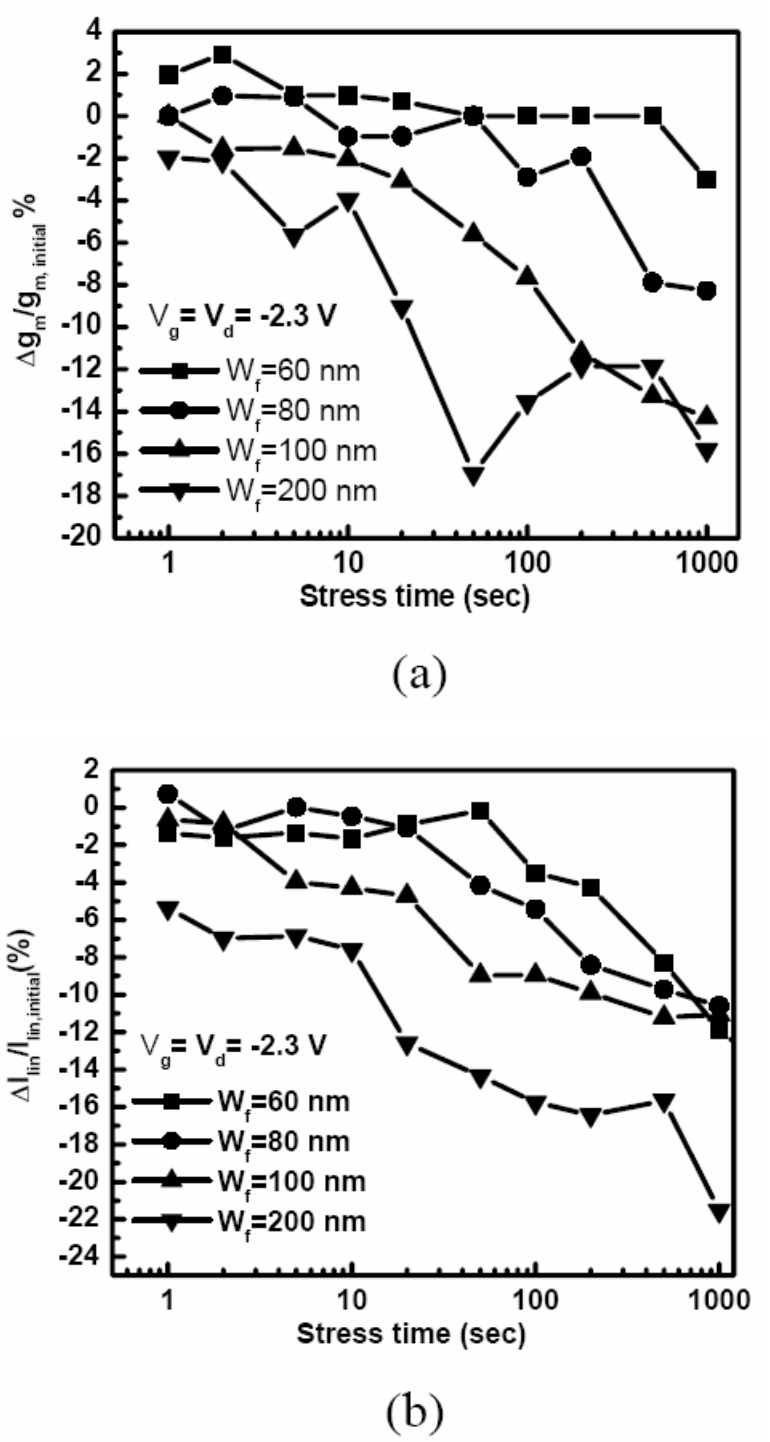
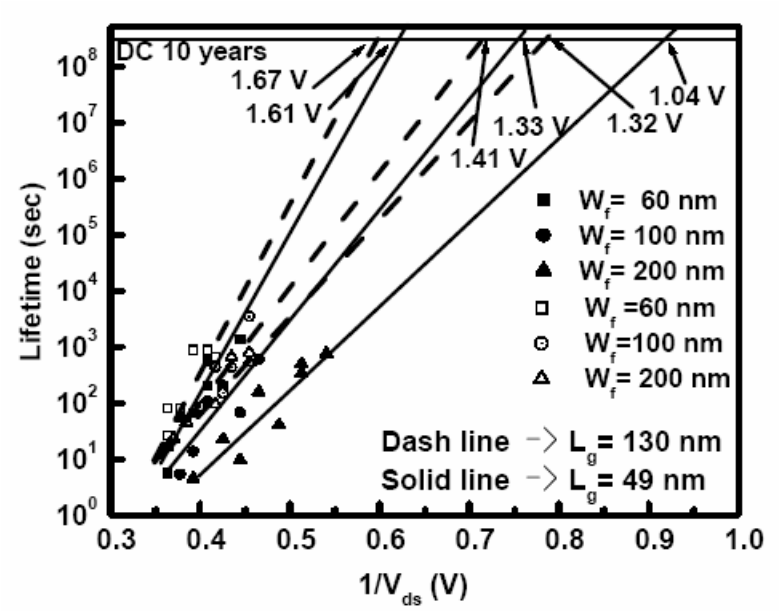
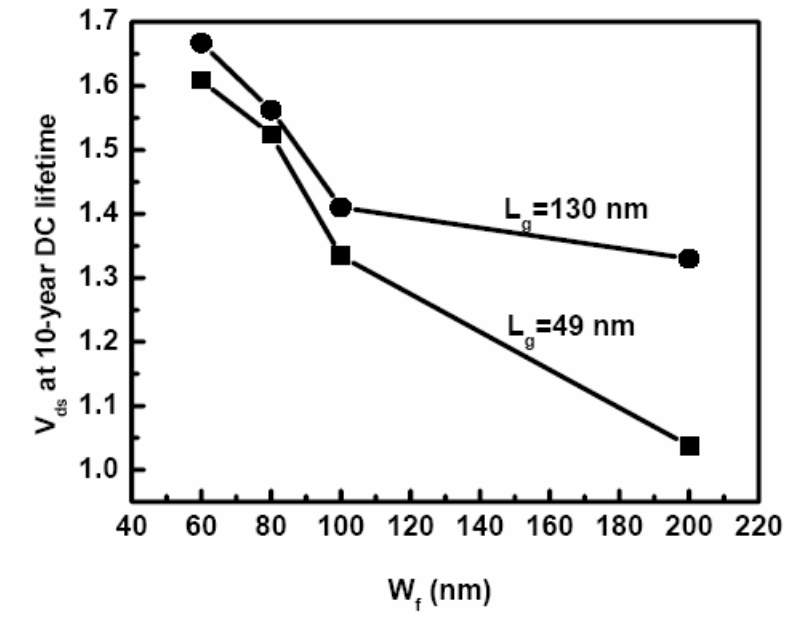


Fig.4-2. The plots of (a) the G_m shift and (b) the I_{lin} shift versus stress time for MSB pFinFETs with L_g=49 nm and different W_f (60, 80, 100, and 200 nm).



(a)



(b)

Fig.4-3. The dc HC lifetime of the devices with L_g=49 and 130 nm and various W_f versus the reciprocal of the drain voltage. (Failure criterion is 10% degradation in Gm at V_g=V_d stress conditions) (b) The comparisons of operation voltages to 10-yr lifetime between the devices with two different L_g (49 nm and 130 nm) and different W_f.

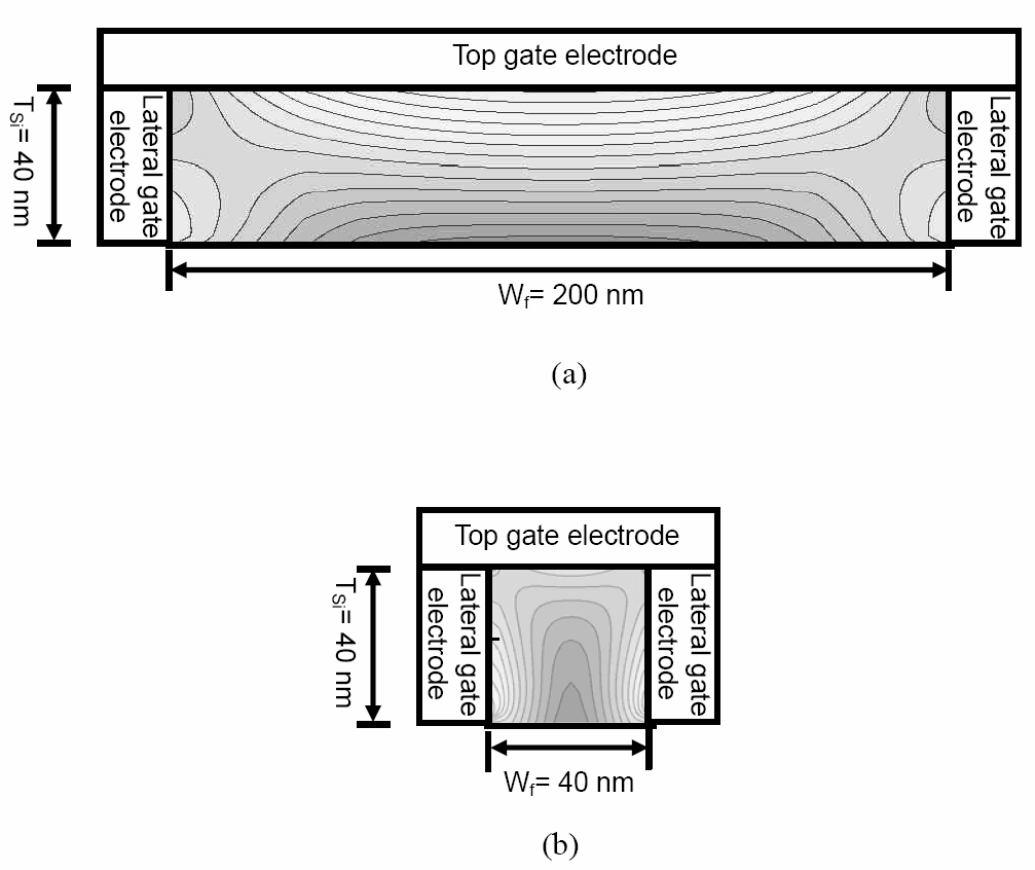
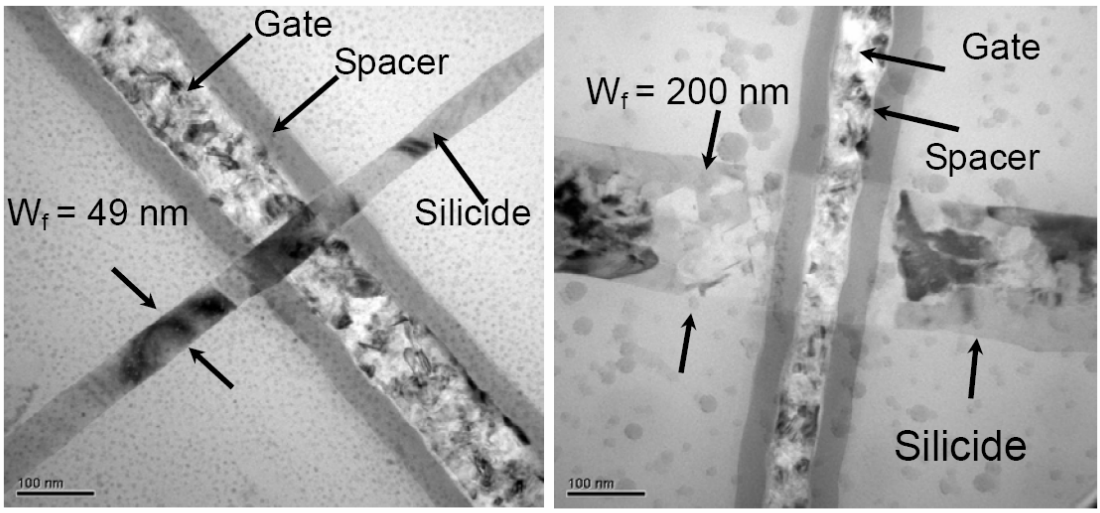
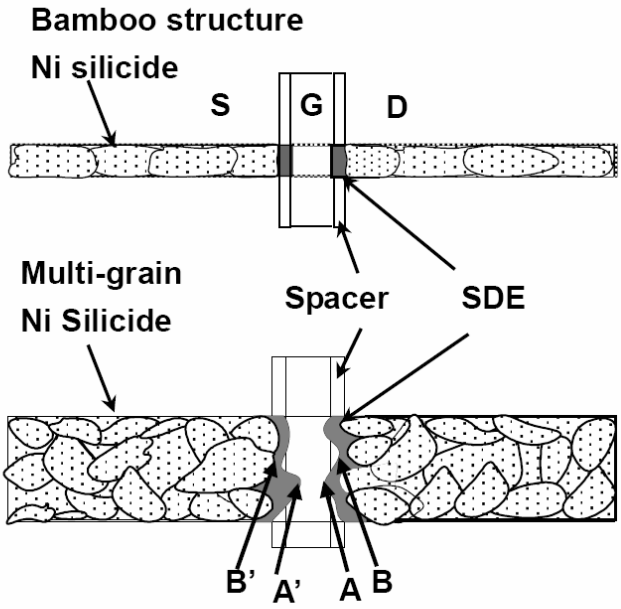


Fig.4-4. The cross-sectional equipotential line plots of Si fins with (a) W_f/T_{Si}=200/ 40 nm, (b) W_f/T_{Si}=40/ 40 nm at V_g = -2V.



(a) (b)



(c)

Fig.4-5. The planar TEM photographs of MSB pFinFETs with (a) W_f=40nm (b) W_f= 200 nm and the schematically photographs of MSB pFinFETs with (c) bamboo and multi-grain Ni silicide fin.

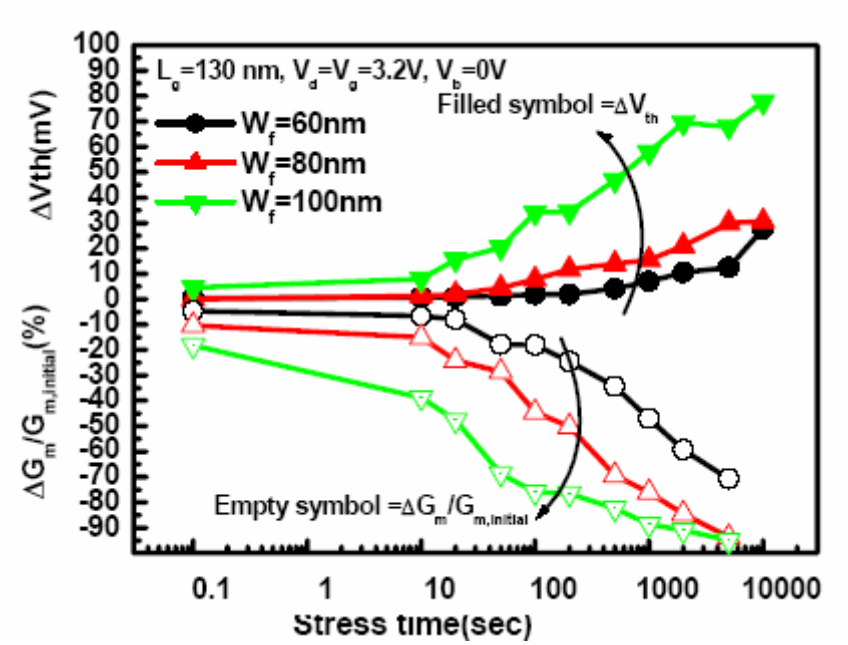


Fig.4-6. The G_m degradation and V_{th} shift of MSB nFinFETs stressed at V_g=V_d=3.2V and V_b=0V.

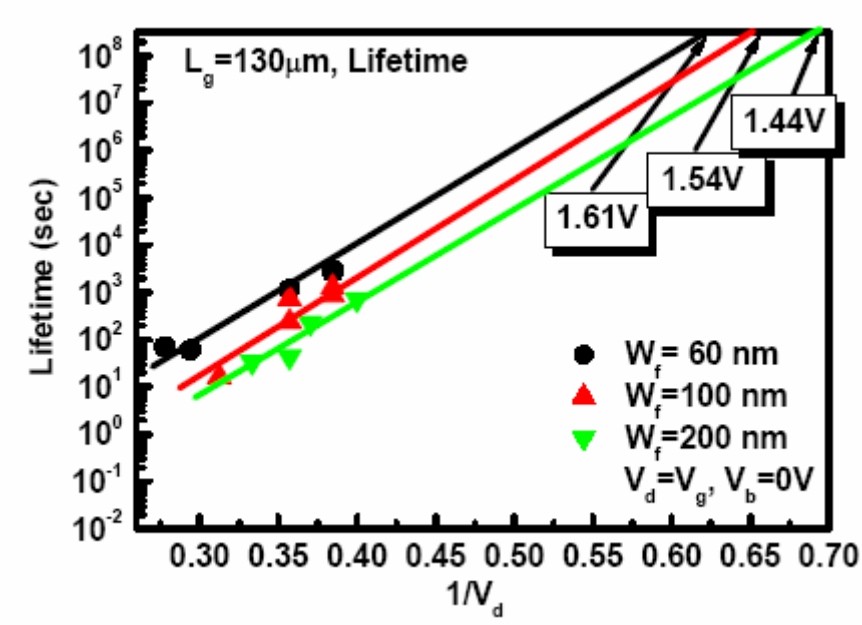


Fig.4-7. The DC hot-carrier lifetime of MSB nFinFETs with different W_f stressed at V_g=V_d=3.2V and V_b=0V.

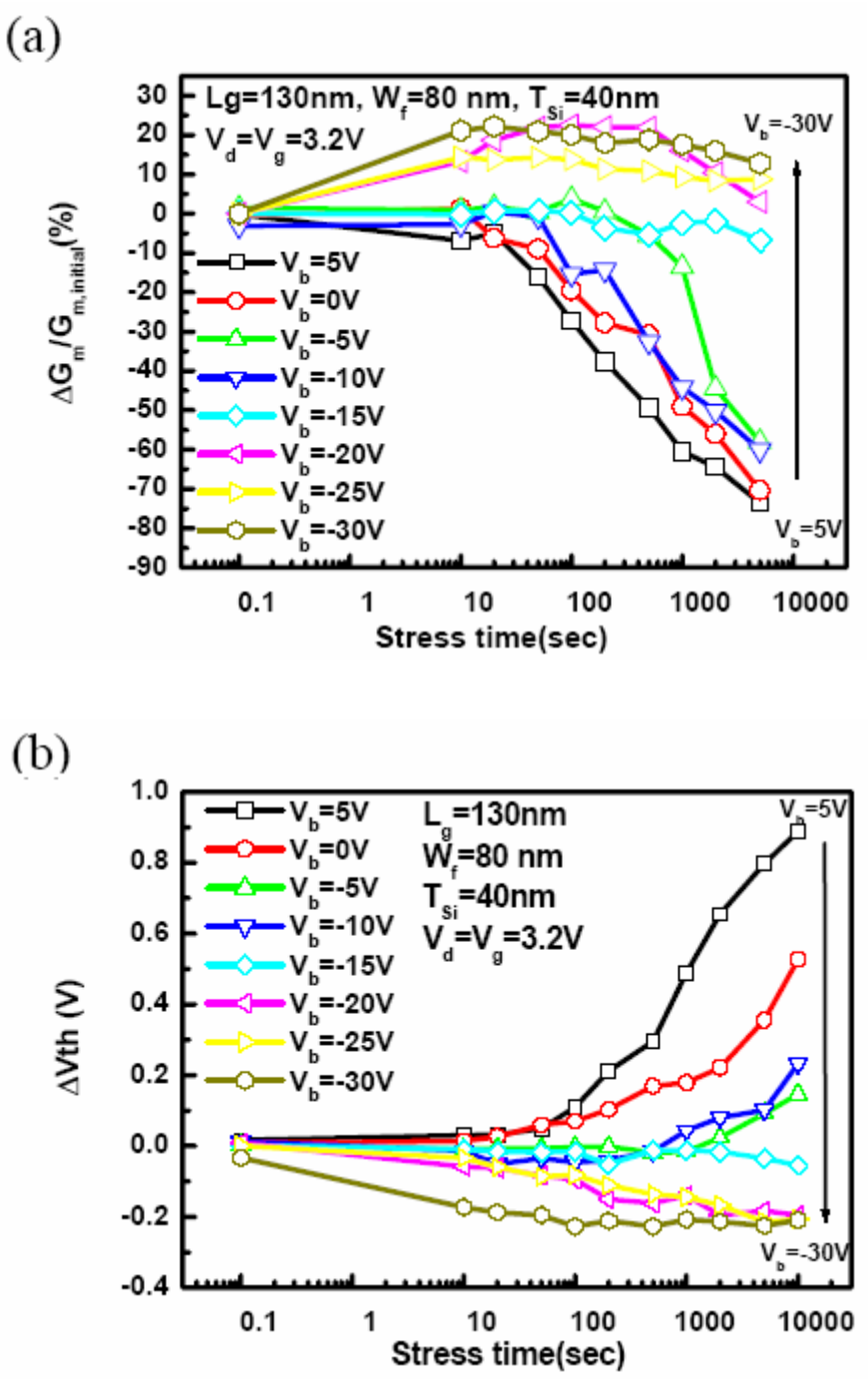


Fig.4-8. (a) The G_m degradation and (b) V_{th} shift of MSB nFinFETs stressed at V_g=V_d=3.2V and different V_b.

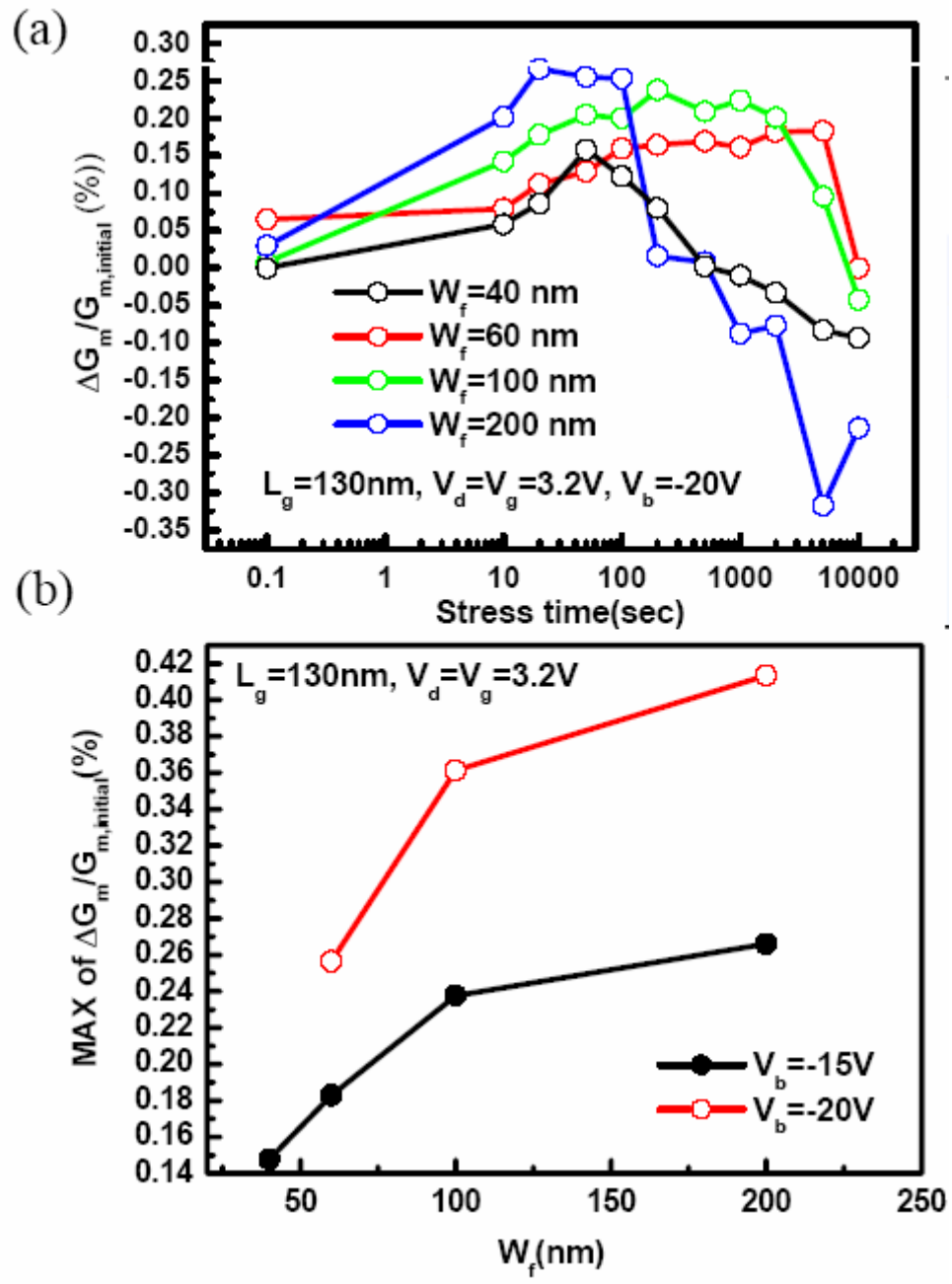


Fig.4-9. (a) The G_m degradation and (b) the maximum positive variations of G_m of MSB nFinFETs with different W_f stressed at V_g=V_d and V_b=-15 and -20 V.

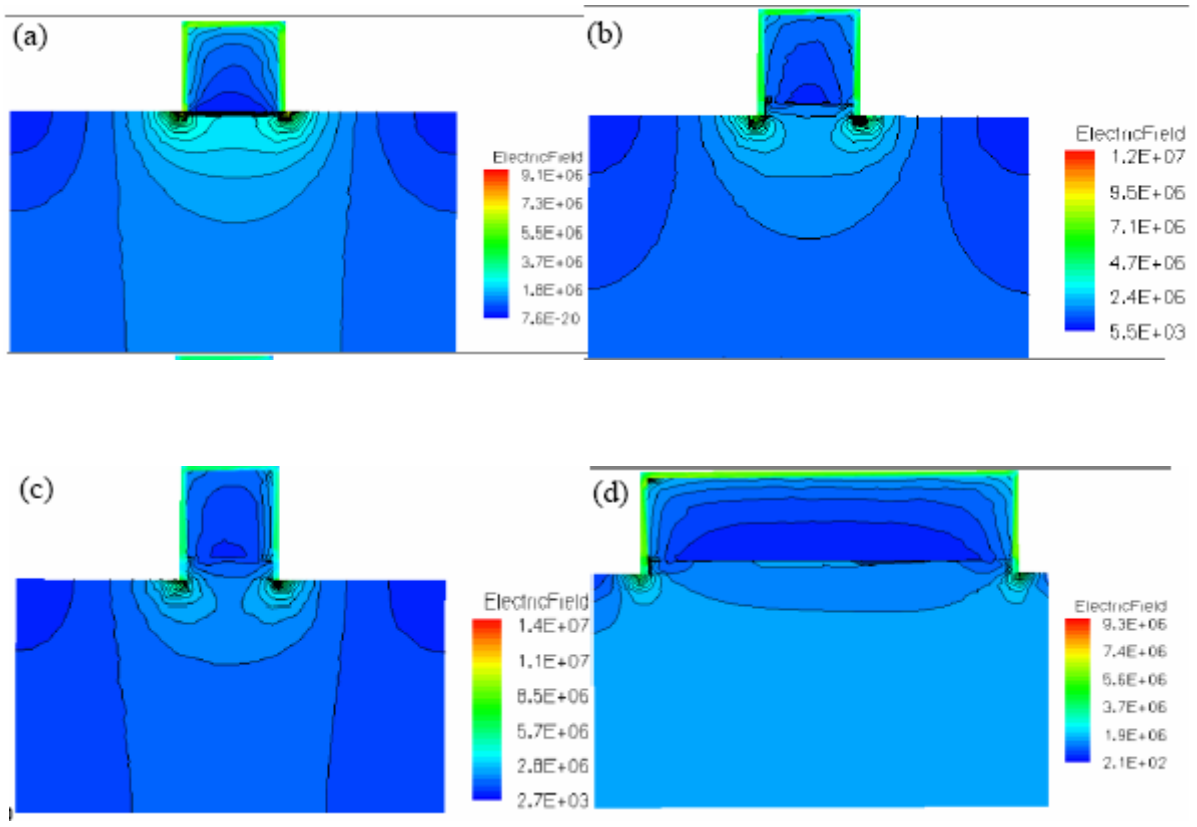


Fig.4-10. The simulated electric field of MSB nFinFETs with (a)W_f=40nm, D_{ext}= 0, (b) W_f=40nm, D_{ext}=8nm, (c)W_f=40nm, D_{ext}=16nm, and (d) W_f=200nm and D_{ext}=8 nm biased at V_g=V_d=3.2V and V_b=-20V.

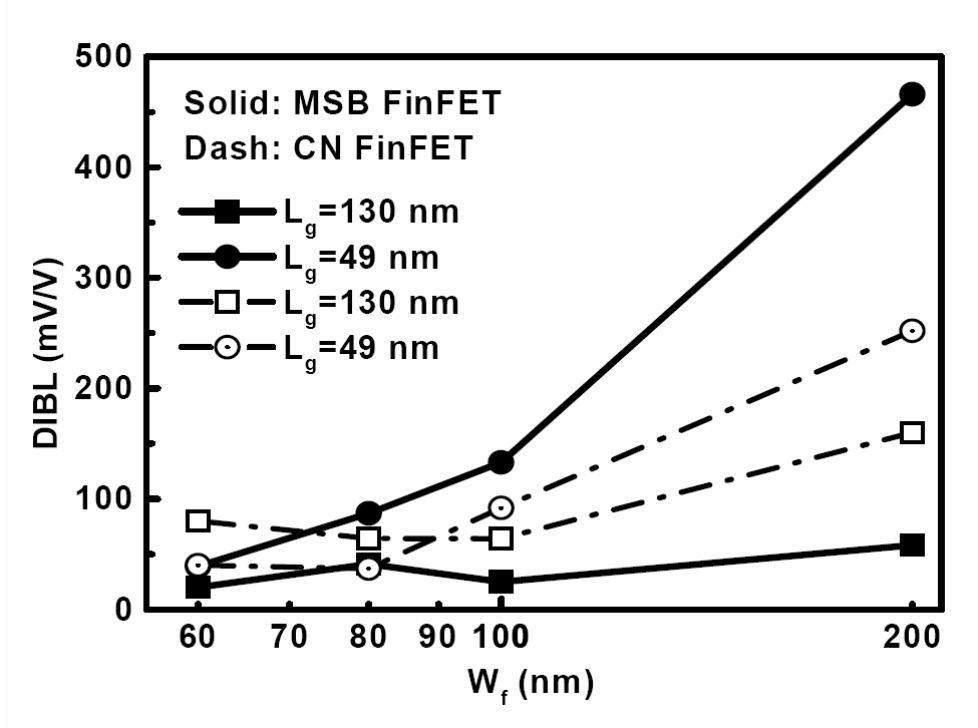


Fig.4-11. Drain-induced-barrier-lowering of MSB and CN FinFETs with different fin thicknesses (W_f) as L_g = 130 nm and 49 nm.

Appendix

Published Journal Papers

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[2]. Bing-Yue Tsui and Chih-Feng Huang, “Structure of Metal Oxide Semiconductor Field Effect Transistor,” U.S. patent, No. 6,835,611 B1, 2004.07.24-2023.07.23, May 30, 2005.

Pending Patents

[1]. Bing-Yue Tsui and Chih-Feng Huang, “ＭＯＳＦＥＴ及びその製造方法,” Japan patent pending.

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