行政院國家科學委員會專題研究計畫　成果報告

次 100 奈米 SOI CMOS 的 RF/Analog 特性分析與模式建立(I)

計畫類別： 個別型計畫
計畫編號： NSC93-2215-E-009-042-
執行期間： 93 年 08 月 01 日至 94 年 07 月 31 日
執行單位： 國立交通大學電子工程學系暨電子研究所

計畫主持人： 蘇彬

報告類型： 精簡報告
報告附件： 出席國際會議研究心得報告及發表論文
處理方式： 本計畫可公開查詢

中　華　民　國 94 年 10 月 31 日

次 100 奈米 SOI CMOS 的 RF/Analog 特性分析與模式建立 (I)
RF/Analog Modeling and Characterization of Scaled SOI CMOS (I)

計畫編號 : NSC 93-2215-E-009-042
執行期限 : 93 年 08 月 01 日　至　94 年 07 月 31 日
主持人 : 蘇彬　　國立交通大學電子工程學系

一、中文摘要

在本計畫中我們將對次 100 奈米 SOI CMOS 的 RF/analog 特性作深入研究與模式建立。利用我們早先完成的統整 SOI 低頻元件模型為基礎，我們在本計畫中所將發展的 RF SOI 元件模型將有益於 RF 電路模擬以及 SOI CMOS 在 SOC 的應用。在本計畫中我們對於前瞻 SOI 元件在高頻時的閘極漏電流、閘極電阻、基極電阻以及浮動基體等效應的實驗分析與探討，也將有助於使用數位 SOI CMOS 技術的 RF/analog 元件設計的最佳化。

關鍵詞 :
RF/analog ； SOI CMOS ； SOC ； 元件設計；電路模擬；實驗分析與模式

Abstract

In this project we investigate sub-100-nm SOI CMOS with emphasis on RF/analog characteristics. Using our previously established unified SOI model as the low frequency core, our developed RF SOI SPICE model will enable RF circuit design and facilitate SOI CMOS for SOC applications. Our physical characterization and modeling including gate tunneling, gate input resistance, substrate resistance and floating body effects for scaled SOI CMOS operated at high frequency will also enhance the device design of digital SOI CMOS technology for RF/analog applications.

Keywords :
RF/analog, SOI CMOS, SOC, device design, circuit simulation, characterization and modeling

二、計畫緣由及目的

The growing demand of mobility and the rapid progress in the wireless industry make the ubiquitous connection possible in today's world. In the past, the Radio Frequency (RF) market was dominated by GaAs or silicon bipolar technology due to their high speed. However, the continual scaling of CMOS technology has raised the cutoff frequency of the deep-submicron MOSFET significantly and made this technology sufficient to build GHz RF circuit blocks. The main advantage of CMOS technology for wireless communication is the integration of RF and analog functionality into the advanced digital CMOS technology to yield the cost-effective System-On-Chip (SOC) solution.

With the scaling of CMOS, SOI (Silicon-On-Insulator) CMOS is emerging as an important IC technology due to the following four technological trends: (1) *High performance*. SOI provides a performance gain of 20 to 35 percent over bulk CMOS [1] due to the reduction of junction capacitance and the absence of the body-bias effect in series connected devices, e.g. in NAND and NOR gates. (2) *Low power*. With the same performance SOI can operate at a lower voltage and therefore lower power. Notice that the primary measures of analog performance such as G_m, f_T and f_{max} also improve at a low supply voltage. (3) *Process simplicity*. SOI may reduce some future bulk-technology's manufacturing difficulties such as isolation,

shallow junction, and latchup sensitivity. (4) *Mixed Technologies.* SOI devices have good immunity to substrate noise due to the isolation provided by the buried oxide layer and to the high-resistivity substrate, which also improves the performance of passive elements such as high-Q inductors and transmission lines commonly used in analog and RF circuits. It may also be useful to embedded DRAM because of good signal isolation from the logic circuit blocks.

Therefore, besides the high performance microprocessor and low power logic, SOI offers advantages over the bulk silicon to realize an SOC by integrating high-performance digital and analog/RF circuits. As a matter of fact, the SOI CMOS technology with f_{max} up to 100 GHz has penetrated into the RF SOC applications [2-4].

However, the main barrier to full exploitation of SOI CMOS performance is that the design of an SOI chip is a relatively risky process because a relative lacking of design experience makes it difficult to achieve fast turnaround and high probability of first-pass success. To surmount this barrier, a robust and physically accurate SPICE (compact) model is needed. SPICE modeling is the standard approach for precise design of standard cell libraries and critical-path sub-circuits in all large systems, as well as the basis for computing the look-up tables used in higher-level timing simulators. IP blocks are in turn designed using the speedier simulations. The existing SOI SPICE models [5-7] are inadequate for GHz frequency operation since they were initially developed for low-frequency applications and mainly focused on DC and transient behavior. The parasitic components ignored at low frequency become very important for predicting device performance at high frequency.

Therefore, we propose to conduct research on RF/analog characterization and modeling for scaled SOI CMOS. In this project, state-of-the-art sub-100-nm SOI MOSFETs will be characterized by DC, AC and S-parameter measurements at frequencies up to 50 GHz. A new model which considers gate tunneling, gate input resistance, body/substrate resistance and floating body effects for scaled SOI CMOS operated at high frequency will be developed. Our investigation will further enhance the device design of digital SOI CMOS technology for RF/analog applications. The developed SPICE model will also facilitate RF/analog circuit simulation/design using advanced SOI CMOS.

三、研究方法

Since the device behavior is continuous as the frequency goes from low to high, a physically accurate SOI SPICE model at low frequency is crucial to compact RF SOI modeling. For sub-100-nm SOI CMOS [8-9], the modeling challenge at low frequency lies in the fact that an SOI model continuously spanning PD (Partial-Depletion) and FD (Full-Depletion) is required due to the following considerations. (1) The need for multiple V_T/T_{OX} transistors for low active/standby power requirement in a single chip may result in the coexistence of both PD and FD devices in the same circuit by design. (2) The laterally non-uniform channel doping (halo/pocket implant) may lead to PD nominal devices and FD long-channel devices with continuous variations in between. (3) The influence of the gate field may encroach from the isolation edges and result in FD narrow-width devices. (4) The coexistence of PD and FD behaviors in a single device, depending on bias conditions.

In our previous NSC project (NSC93-2215-E-009-029), "A Unified Model for Partial-Depletion and Full-Depletion SOI Circuit Designs: Investigation of Geometry-Dependent Body-Source Built-In Potential Lowering for 65-nm SOI CMOS," we have used the concept of body-source built-in potential lowering (ΔV_{bi}) [10] to solve the

problem of the coexistence of PD/FD devices in a single chip as well as the coexistence of PD/FD behavior in a single device for scaled SOI CMOS [22-23]. In this project, we will use this unified model as our low frequency core and further extend this model in the AC and high frequency regime.

Since the self-biasing of SOI floating body may impact the transistor current gain (h_{21}), unilateral gain (U) and the cutoff frequency, it is crucial to investigate/solve the following floating-body related issues for the RF/analog modeling of sub-100-nm SOI CMOS. (1) The measurement of ΔV_{bi} [10] becomes difficult with the SOI-thickness scaling because of the reduction of the efficiency of body contacts. To extract ΔV_{bi} for floating-body SOI devices without body contacts, we have proposed a methodology based on the correlation between ΔV_{bi} and threshold voltage (V_T) recently [21]. (2) The gate-body-tunneling induced floating-body effect [24] becomes significant with the oxide-thickness scaling and is responsible for the second peak present in the G_m-V_{GS} characteristics (Fig. 1(a)) as well as the frequency dependence of G_m (Fig. 1(b)). Moreover, it induces excess shot noise in the low-frequency noise spectrum (Fig. 1(c)) and therefore needs to be modeled. Notice that low-frequency noise is an important figure of merit for analog circuits because it may impact the jitter of VCOs and the charge pump of PLLs [11].

For extremely scaled SOI CMOS, multiple-gate device has been widely proposed [12-13]. The sizes of state-of-the-art multiple-gate devices can be well below 50nm in all of the three dimensions. For devices with geometries so small, quantum-mechanical effects may be present. Reference 14-18 demonstrated that conductance oscillations, one important consequence of quantum effects, may occur in small devices with novel test structures or at very low temperature. For advanced CMOS transistors under room temperature, however, this phenomenon has rarely been investigated. In this project, we have investigated the phenomenon of transconductance (G_m) oscillations in advanced multiple-gate FinFET SOI transistors with 1.6nm gate oxide near room temperature [19]. The results of our investigation will be detailed in this report.

Gate input capacitance is one important figure of merit for high-frequency analog transistor performance. As the gate dielectric thickness is reduced and gate tunneling current increases, the measurement of gate capacitance becomes difficult due to the attenuated capacitance (Fig. 2 [20]) caused by the coexistence of inductance, series resistance and gate tunneling current in MOS test structures. Although several models have been proposed to capture the measured C-V characteristics, they are not physically accurate enough for both DC and AC to provide satisfactory scalability. In this project, we have investigated the distorted C-V characteristics for MOSFETs with ultra-thin gate oxide and proposed a scalable model to simulate the anomalous C-V behavior. The results of our investigation have been published in Ref. 20.

The substrate network is important for RF application because the substrate resistance will degrade output resistance as the impedance of the drain junction capacitance drops at high frequency. A wide range of topologies of substrate network has been proposed in the RF CMOS modeling. For scaled SOI CMOS with quasi-neutral body (i.e., PD), the body resistance together with the junction capacitance provides a shunt branch from the output to ground. This effect may impact the RF SOI modeling.

For example, an accurate determination of gate/source/drain resistance (R_g/R_s/R_d) for RF SOI MOSFETs is an important modeling issue. Reference 25-27 have presented extrinsic resistance extraction methodologies for RF CMOS. Among these approaches, the

zero method [25,28] developed under the *zero* condition (i.e., V_{GS}=V_{DS}=0V) is attractive because it may simplify the corresponding equivalent circuit and avoid the error caused by the NQS (non-quasi-static) effect [26]. Based on the equivalent circuit built for bulk MOSFETs under the *zero* condition [28], the following frequency-independent resistance expressions have been derived to directly determine R_s, R_d and R_g, respectively.

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s \quad (1)$$

$$\mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}) = R_d \quad (2)$$

$$\mathrm{Re}(Z_{11}) - \mathrm{Re}(Z_{12}) = R_g \quad (3)$$

For PD SOI MOSFETs, however, Eq. (1)-(3) may not be valid due to the existence of the quasi-neutral body. In this project, we have investigated the RF extrinsic resistance extraction for PD SOI MOSFETs [29]. The results of our investigation will be detailed in this report.

四、結果與討論

1. Transconductance oscillation in multiple-gate SOI MOSFETs [19]:

In this work, our multiple-gate SOI devices (Fig. 3) were fabricated on p-type SIMOX SOI wafers using optical lithography. The Si-body thickness, H_{fin}, was thinned down to 40 nm by thermal oxidation. The fin-width, W_{fin}, was defined by wet-etching and ranges from about 15 to 25 nm. After W_{fin} was developed, the 1.6-nm gate oxide was thermally grown. The ultra-thin gate oxide contributes to not only the suppression of short-channel effects, but also the gate coupling strength of the transistor [30].

The gate length, L_g, was defined by in-situ heavily-doped N^+ poly-silicon gate and ranges from 30 to 40 nm. Without the LDD implantation, the composite spacer of silicon oxide and nitride was deposited and anisotropically etched. The un-doped regions under the spacers separate the inversed carriers from source/drain and act as electrostatic tunnel barriers [31]. Finally, heavily-doped N^+ source/drain was made. It is worth noting that the parasitical source/drain resistance, which may determine the tunnel barrier [32], depends on H_{fin} and W_{fin} in this multiple-gate SOI structure.

Figure 4 shows the G_m-V_G characteristics measured by HP4156B in a low-noise probe station at room temperature (T = 20 ^oC) for the device with L_g = 30 nm and W_{fin} = 25 nm. A fine periodic oscillation in G_m, an indication of the Coulomb blockade oscillation (CBO) [14], can be seen starting from V_G ~ 0.2V. We have noted that the fine periodic oscillations can be reproduced from sample to sample, and the peaks of each period for the same devices may be repeated at the same gate bias. It can be seen from the inset of Fig. 4 that the oscillating period is 17 mV. For devices with large dimensions under the same measurement system, nevertheless, only the thermal noise can be seen. In addition, we have confirmed that the effect of source accuracy is not responsible for the observed periodic oscillation.

To further analyze the periodic oscillation in G_m, both the discrete Fast Fourier Transform (FFT) and the histogram of the directly counted peak-to-peak spacing (ΔV_G) in the G_m-V_G characteristics can be applied. The power spectrum density of FFT, shown in Fig. 5(a), may represent the intensity of the corresponding periodic signal plus the period counts of ΔV_G (Fig. 5(b)). It can be confirmed from Fig. 5 that the observed conductance oscillation in Fig. 4 indeed has a period of 17 mV.

According to the CBO theory, the period of conductance oscillation (ΔV_G) represents the charging energy and is related to the gate capacitance, $C_g = qn_sW_{eff}L_{eff}/(V_G-V_T)$, where q is 1.6×10^{-19} C, W_{eff} is the effective channel width, L_{eff} is the effective channel length, V_T is the threshold voltage of the MOSFET and n_s is the carrier density of the inversion layer. n_s can

be estimated by the weak-interference (WI) effect [15], which usually coexists with CBO [15,31] and can also be observed in our device. As indicated in Fig. 6, the transmission maximum of carriers due to the WI effect occurs when [15] $L_{eff} = n\lambda_F/2$, where n is an integer and λ_F is the Fermi wavelength. Once λ_F is experimentally determined by Fig. 6, n_s can be calculated by $n_s = q4\pi/\lambda_F^2$ if we assume the valley degeneracy is equal to 2 [15]. Once n_s is known, we may estimate C_g, which is about 20 aF for the device under study. The ideal Coulomb charging energy (e/C_g), therefore, should be about 8mV. The discrepancy between our observed ΔV_G (17 mV) and e/C_g may stem mainly from the junction capacitances. In other words, the quantum dot in our single-electron-like transistor may no longer be considered as a disk-like island but rather a three-dimensional box.

Figure 7 shows the G_m-V_G characteristics for the device with L_g = 40 nm and W_{fin} = 15 nm at various temperature. Clear G_m oscillation can be seen as the temperature is decreased (T = -40 ^oC). We have noted that the oscillating period, ΔV_G, is about 13 mV for all the devices with this size. The observed geometrical dependence of ΔV_G is different from the finding in Ref. 16, where the formation of dots was referred to random fixed charges. It is also worth noting that split-peak separations can be seen in Fig. 7. This may be caused by the coupling effect [18] between the carriers confined in the two separated channels of the narrow W_{fin} device, as depicted in the inset of Fig. 7.

In conclusion, we have investigated the phenomenon of conductance oscillations in state-of-the-art multiple-gate FinFET SOI devices with 1.6nm gate oxide. Both the weak-interference effect and the fine periodic oscillations in G_m have been observed near room temperature in our devices. Since multiple-gate SOI device with 3D structure could be one candidate for extremely scaled CMOS transistor, this quantum-mechanical phenomenon may become increasingly important with device scaling.

2. Impact of quasi-neutral body on RF SOI modeling [29]:

In this work, the thicknesses for gate oxide, SOI layer and buried oxide of our SOI MOSFETs are 1.4nm, 40nm and 200nm, respectively. The presence of kinks in Fig. 8 shows that the devices under test are partially depleted. These RF devices were laid out in the multi-finger and multi-group structure with various finger number *NF*, group number *NG* and finger length W_f for a given gate length L_f. On-wafer 2-port S parameters up to 20 GHz were measured, de-embedded, and then transformed to Z parameters to obtain the resistance vs. frequency characteristics.

To further minimize possible substrate resistive loss through the buried oxide layer [33], a bias-network connected to the probe station's chunk was used to provide the substrate DC ground (i.e., back-gate voltage V_E=0) with RF floating. In fact, as shown in Fig. 9, no matter the substrate RF ground is provided or not, the resistance curves are almost unchanged. This indicates that the substrate effect is negligible in this experiment.

Figure 9 also compares the resistance vs. frequency characteristics for PD SOI MOSFET and its bulk counterpart with identical layout structure and geometry. All of these curves more or less are frequency-dependent. The poor shapes for the bulk MOSFET may result from the complicated and significant substrate resistive loss [34-35]. For the SOI MOSFET, however, the substrate loss may not be responsible for this frequency-dependent behavior because the thick buried oxide layer in the SOI transistor may provide good isolation from the substrate.

Figure 10 shows a cross-sectional view of the PD SOI MOSFET under the *zero* condition. The neutral-body coupling path in Fig. 10 is

constituted by source- and drain-side junction capacitances ($C_{j,bs}$ and $C_{j,bd}$) and body conductances (G_{bs} and G_{bd}). Its corresponding equivalent circuit without substrate RF ground is depicted in Fig. 11. Here the neutral-body coupling path is represented by a lumped junction capacitance C_b (= $(1/C_{j,bs} + 1/C_{j,bd})^{-1}$) together with a lumped body conductance G_b (= $(1/G_{bs} + 1/G_{bd})^{-1}$). Based on this equivalent circuit, the following resistance expressions regarding R_s, R_d and R_g can be derived:

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s + A/(\omega^2 + B) \quad (4)$$

$$\mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}) = R_d + A/(\omega^2 + B) \quad (5)$$

$$\mathrm{Re}(Z_{11}) - \mathrm{Re}(Z_{12}) = R_g - 0.5 \times A/(\omega^2 + B) \quad (6)$$

where

$$A = 2C_b^2 G_b / D \quad (7)$$

$$B = G_b^2 (4C_{ds}^2 + C^2 + 4C_b^2 + 4CC_{ds} + 8C_{ds}C_b + 4CC_b)/D \quad (8)$$

$$D = (C^2 C_b^2 + 4C_{ds} CC_b^2 + 4C_{ds}^2 C_b^2) \quad (9)$$

Note that we have assumed $C_{gs} = C_{gd} = C$ in the derivation because of the symmetry of geometry and bias. Eq. (4)-(6) predict that the existence of neutral body may cause the resistance curves regarding R_s, R_d and R_g frequency-dependent and explain the SOI behavior in Fig. 9.

Using this new model, a physical RF extrinsic resistance extraction methodology for PD SOI MOSFETs can be developed. The model-data comparison for the extraction of R_s, R_d and R_g with various layout geometries are shown in Fig. 12 to 14, respectively. It can be seen that the measured curves are indeed frequency-dependent, and can be well predicted by our model (Eq. (4)-(9)). The extracted extrinsic resistances and fitting parameters A and B for each SOI device are listed in Table 1. Since all the involved device conductance and capacitances in Eq. (7)-(9) are proportional to the total gate electrical width W_{total} ($\approx W_f \times NF \times NG$), the parameter A should increase as W_{total} decreases. As shown in Fig. 12 to 14, the resistance curves for the device with smaller W_{total} indeed have a larger deviation from its high-frequency asymptote in the lower frequency regime. Therefore, one may minimize the extraction error resulted from the SOI neutral body by using the wide device.

In conclusion, we have investigated the extrinsic resistance extraction for PD SOI MOSFETs. Although the thick buried oxide in SOI devices can block the complicated substrate network, the SOI neutral-body coupling effect may become significant for RF applications. An equivalent circuit considering this effect has been proposed. Based on the equivalent circuit, a new model capturing the frequency dependence of extrinsic resistances has been derived. After considering the presence of floating body, we have developed a physically accurate RF extrinsic resistance extraction methodology for PD SOI MOSFETs.

五、計畫成果自評

In this project, we have investigated sub-100-nm SOI CMOS with emphasis on RF/analog characteristics. Our investigation has included critical modeling issues regarding floating body effects [21], quantum-mechanical G_m oscillation in multiple-gate SOI [19], gate input capacitance extraction for ultra-thin oxide [20] and the body/substrate resistance effect for PD SOI MOSFETs operated at high frequency [29].

Our investigation will be instrumental in early anticipation of the potentials of digital SOI CMOS technology for RF/analog applications and enhancing the device design so as to effectively utilize the tremendous intrinsic speed resulting from further scaling of sub-100-nm SOI CMOS. The developed SPICE model and model parameter extraction procedure based on our investigation will enable early RF/analog circuit design and facilitate SOI CMOS for SOC applications.

The results of the project have been disseminated through research reports in international journals [21,36] and conferences

[19-20,29] as well as used in education of our graduate students to become leading researchers in the areas of compact modeling, device design and circuit simulation for SOI CMOS.

六、參考文獻

[1] G. G. Shahidi et al., 1999 IEEE International Solid-State Circuits Conference, Feb. 1999, p. 426.
[2] J. Kim et al., IEEE 2004 Custom Integrated Circuits Conference, pp. 541-548.
[3] J.-O. Plouchart, IEEE 2003 SOI Conference.
[4] T. Douseki et al., IEEE 2003 Custom Integrated Circuits Conference, pp. 163-168.
[5] P. Su et al., IEEE 2000 Custom Integrated Circuits Conference, pp. 197-200.
[6] J. B. Kuo, Digest of Hong Kong Electron Device Meeting Conference (HKEDM), Hong Kong, June 2000.
[7] P. Su et al., IEEE 2003 Custom Integrated Circuits Conference, pp. 241-244.
[8] F.-L. Yang et al., Tech. Digest of 2003 Symposium on VLSI Technology.
[9] F.-L. Yang et al., IEDM Technical Digest, December 2003.
[10] P. Su et al., "On the body-source built-in potential lowering of SOI MOSFETs," IEEE EDL, vol. 24, no.2, pp. 90-92, February 2003.
[11] J. Kim et al., ISLPED, pp. 434-439, August 2003.
[12] Z. Krivokapic et al., SSDM (2003) p. 760.
[13] F.-L. Yang et al., SSDM (2004) p. 772.
[14] Y. Takahashi et al., IEEE TED., vol.43, no.8, 1996.
[15] Y. Omura et al., IEEE EDL, vol.18, no.5, 1997.
[16] M. G. Peters et al., JAP, vol.84, no.9, Nov. 1998.
[17] J. Scott-Thomas et al., Phys. Rev. Lett., vol.62, p.583, 1989.
[18] F.R. Waugh et al., Phys. Rev. Lett., vol.75, p.705, 1995.
[19] W. Lee, P. Su et al., "An assessment of single-electron effects in multiple-gate SOI MOSFETs with 1.6-nm gate oxide near room temperature," Proceedings of 2005 International Semiconductor Device Research Symposium (ISDRS), Washington D.C., Dec. 2005.
[20] W. Lee, K. Su, C. Chiang, S. Liu and P. Su, "Inversion MOS capacitance extraction for ultra-thin gate oxide using BSIM4," Proceedings of the IEEE 2005 VLSI-TSA International Symposium on VLSI Technology, Hsinchu, Taiwan, April 2005, pp. 62-63.
[21] P. Su et al., "On the prediction of geometry-dependent floating-body effect in SOI MOSFETs," IEEE Transactions on Electron Devices, vol. 52, no. 7, pp. 1662-1664, July 2005.
[22] P. Su et al., "Modeling geometry-dependent floating-body effect using body-source built-in potential lowering for scaled SOI CMOS," SSDM, Sep. 2004, pp. 510-511.
[23] P. Su et al., "Modeling geometry-dependent floating-body effect using body-source built-in potential lowering for SOI circuit simulation," Jpn. J. Appl. Phys., vol. 44, no. 4B, pp. 2366-2370, April 2005.
[24] P. Su et al., Proceedings of the 2002 International Symposium on Quality Electronic Design, San Jose, CA, March 2002, pp. 487-491.
[25] J.-P. Raskin et al., Proc. Electrochem. Soc., Los Angeles, CA, 1996, vol. 96-3, pp. 225–231.
[26] A. Bracale et al., Analog and Integrated Circuits and Signal Processing. Norwell, MA: Kluwer, 2000.
[27] H. Liao et al., International Conference on Solid-State and Integrated Circuit Technology (ICSSICT), pp. 913-915, 2001.
[28] D. Lovelace et al., IEEE MTT-S International Microwave Symp. Digest, pp. 865-866, 1994.
[29] S.-C. Wang, P. Su et al., "RF extrinsic resistance extraction considering neutral-body effect for partially-depleted SOI MOSFETs," submitted to the IEEE 2006 VLSI-TSA International Symposium on VLSI Technology.
[30] Y.-M. Wan et al., IEEE 5th Conf. on Nanotech., 2005.
[31] F. Boeuf et al., IEEE Trans. on Nanotech. vol. 2(3), p.144, 2003.
[32] X. Jehl et al., IEEE Trans. on Nanotech. vol. 2(4), p.308, 2003.
[33] C. L. Chen et al., IEEE EDL, vol.21, pp. 497–499, Oct. 2000.
[34] W. Liu et al., Proc. IEDM, Dec. 1997, pp. 309–312.
[35] R. T. Chang et al., IEEE TED, vol.51, no.4, pp. 421–426, Mar. 2004.
[36] W. Lee, P. Su et al., "An assessment of single-electron effects in multiple-gate SOI MOSFETs with 1.6-nm gate oxide near room temperature," submitted to IEEE EDL.

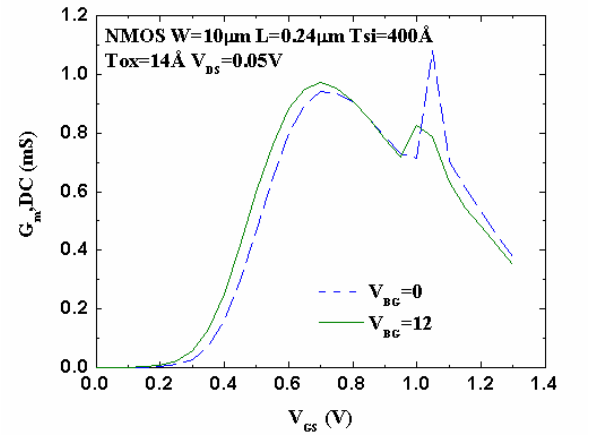

Fig. 1(a). Impact of gate-body tunneling on transconductance (G_m). G_m is extracted from the I_{DS}-V_{GS} characteristics. Notice the second peak around V_{GS} = 1.1V and the backgate-bias (V_{BG}) effect.

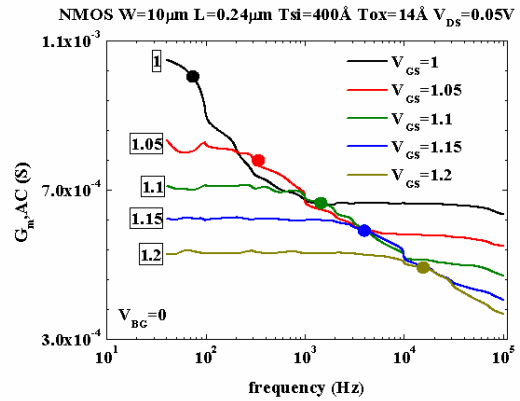

Fig. 1(b). Frequency dependence of G_m when the SOI device is biased in the second-peak regime. Notice that the corner frequency increases with the gate bias.

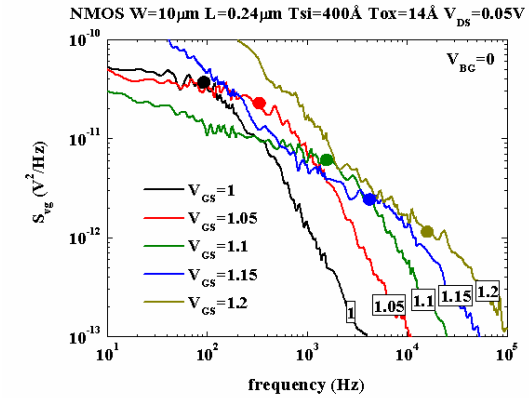

Fig. 1(c). Impact of gate-body tunneling on low frequency noise. Notice that the corner frequency of the Lorentzian-like noise spectrum increases with the gate bias.

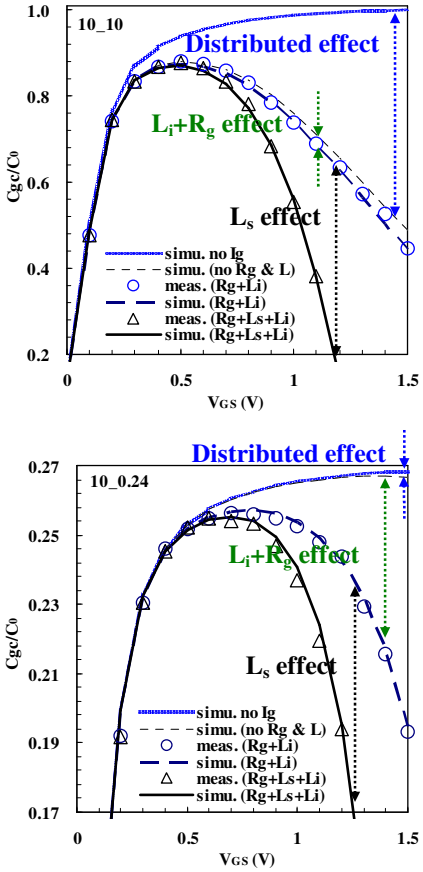

Fig. 2. A comparison between (a) long-channel (L=10µm) and (b) short-channel (L=0.24µm) devices regarding the C_{gc} characteristics. W=10µm. L_i is the parasitic inductance within the test structure. L_s is the cable inductance. R_g is the gate resistance.

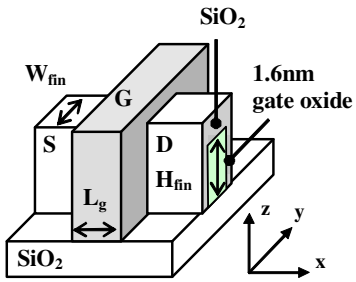

Fig. 3. Multiple-gate FinFET SOI structure investigated in this work.

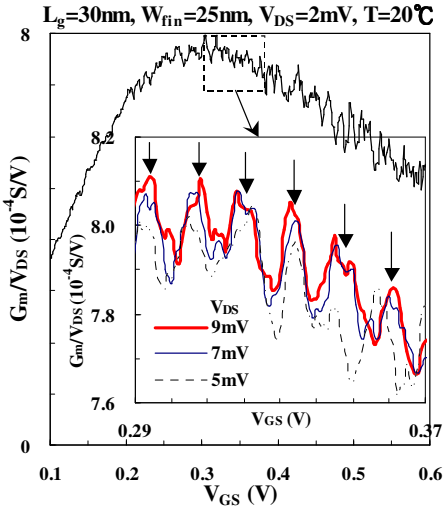

Fig. 4. Periodic Coulomb blockade oscillations occur in G_m/V_{DS}. G_m is extracted by dI_D/dV_G and shows a period of 17 mV.

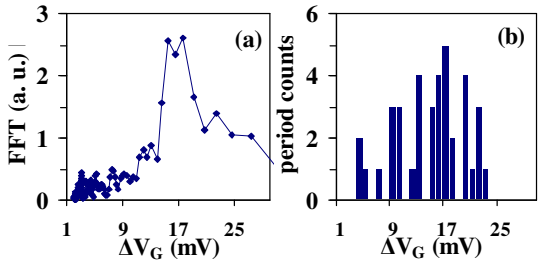

Fig. 5. Both (a) the Fast Fourier Transform (FFT) and (b) the histogram of the directly counted peak-to-peak spacing (ΔV_G) confirm that the period in Fig. 4 is 17 mV.

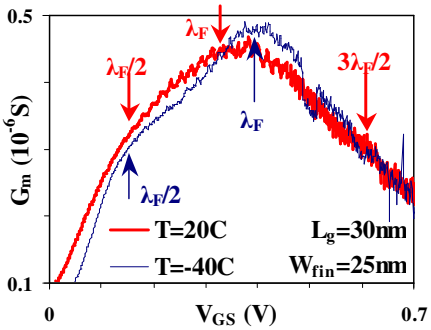

Fig. 6. The weak-interference effect can be observed in our device. The transmission maximum occurring at $\lambda_F/2$, λ_F, and $3\lambda_F/2$ corresponds to V_G = 0.15V, 0.32V and 0.61V, respectively, at T = 20 °C.

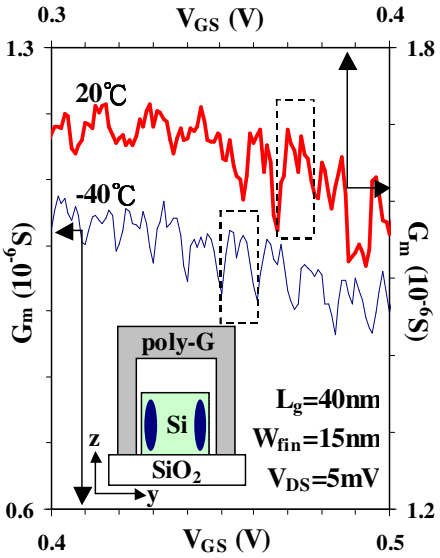

Fig. 7. Split peak separations can be seen in the narrow W_{fin} device.

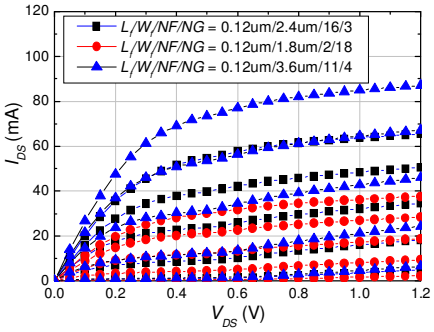

Fig. 8. I_{DS} versus V_{DS} curves for PD SOI MOSFETs used in this study. V_{GS} is from 0.4 to 1.2 V with step 0.2 V.

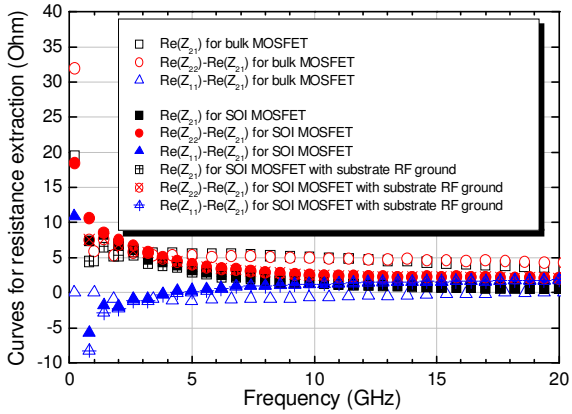

Fig. 9. Resistance curves for the bulk and PD SOI MOSFET with $L_f/W_f/NF/NG$= 0.12µm/2.4µm/16/3.

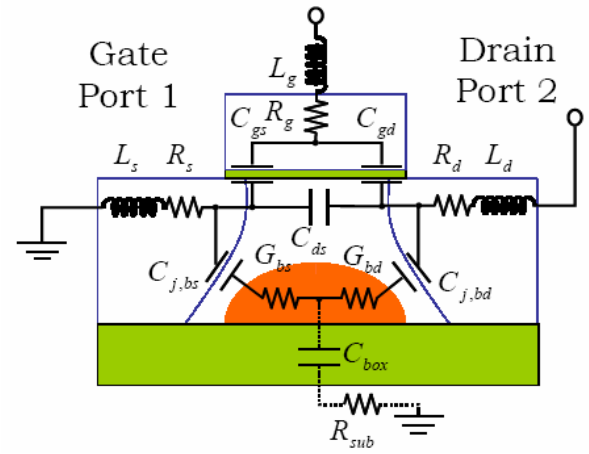

Fig. 10. Cross-sectional view of the *zero* PD SOI MOSFET.

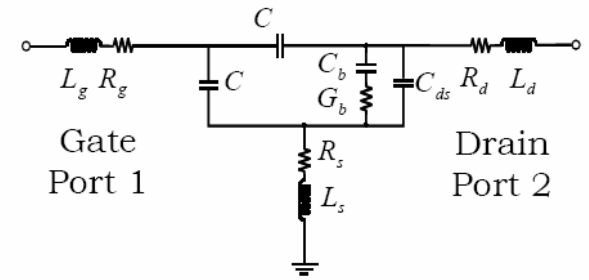

Fig. 11. Equivalent circuit for *zero* PD SOI MOSFETs.

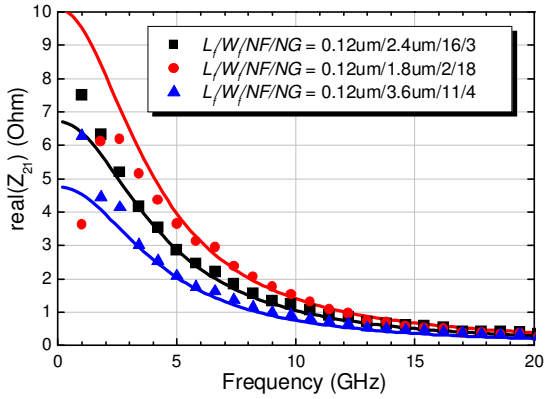

Fig. 12. Curve fitting results for R_s extraction (points: measured data. lines: model)

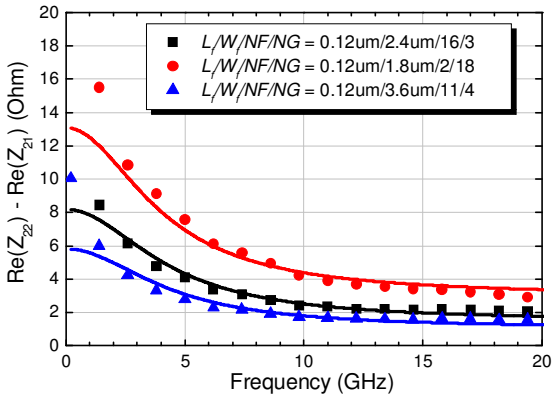

Fig. 13. Curve fitting results for R_d extraction (points: measured data. lines: model)

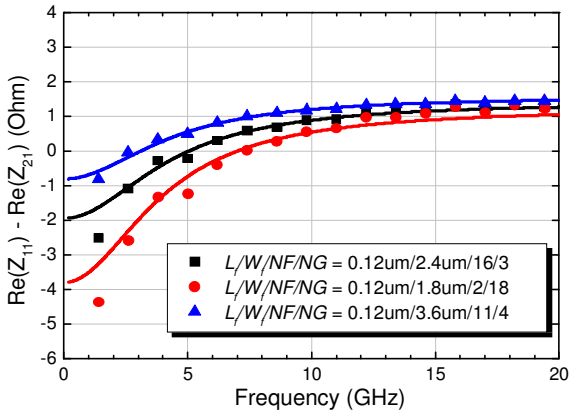

Fig. 14. Curve fitting results for R_g extraction (points: measured data. lines: model)

Table 1. Extracted values for fitting parameters A, B and extrinsic resistances (The values of L_f/W_f/NF/*NG* for FET1, FET2 and FET3 are 0.12µm/2.4µm/16/3, 0.12µm/1.8µm/2/18 and 0.12µm/3.6µm/11/4, respectively.)

	W_{total} (µm)	A ($\times 10^{21}$ $F^{-1}.s^{-1}$)	B ($\times 10^{20}$ s^{-2})	R_s (Ω)	R_d (Ω)	R_g (Ω)
FET1	115.2	4.9	7.2	<0.1	1.5	1.4
FET2	64.8	6.4	6.4	<0.1	3	1.3
FET3	158.4	3.5	7.4	<0.1	1	1.5