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<center><112></center>
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2.

Thin-film transistors fabricated by <111> and <112> needle grains have been investigated. They were fabricated by Ni-metal-induced lateral crystallization method and Ni-metal imprint method. It is found that the performance of 112-TFT was far superior to that of 111-TFT. The device transfer characteristics of 112- TFT is 2.6 times increased in field-effect mobility (μ_{FE}), and 4 times improved on/off current ratio (I_{on}/I_{off}), and 2.4 times diminish in leakage current (I_{off}) that compared with the 111-TFT.

Low-temperature polycrystalline-silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest owing to their use in the active matrix liquid crystal displays (AMLCDs) due to its higher carrier mobility compared with amorphous Si (α-Si) and can be used to integrate circuit on the glass substrate. Many kinds of techniques have been used to crystallize the α-Si on the inexpensive glass substrate. Among many crystallization methods, excimer laser crystallization (ELA) of α-Si film appears to be very promising method due to its lower thermal budget, shorter processing time, and ability to produce

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poly-Si film with better quality than others. However, the equipment cost is high and uniformity is poor. As for the solid phase crystallization (SPC) method, it is a well-established poly-Si formation technique with several advantages over ELA, including smoother surfaces, superior uniformity, and batch process in furnace annealing.[1,2] However, there are several drawbacks of SPC poly-Si: (1) grain size is small, (2) carrier mobility is low, and (3) α-Si needs to be annealed for about 24h at temperature over 600°C.[3] The temperature is higher than the strain temperature of a normal glass substrate. In comparison, the Ni-metal-induced crystallization (NIC) and Ni-metal-induced lateral crystallization (NILC) method has a lower equipment cost than ELA, and a lower thermal budget than SPC. In NIC and NILC, a thin Ni[4-7] metal layer is selectively deposited on the top of α-Si film, which is followed by annealing at a temperature lower than 600°C. Three stages have been identified in the process: (1) the formation of $NiSi_2$ precipitates, (2) the nucleation of crystalline Silicon (c-Si) on $NiSi_2$ precipitates, and (3) the subsequent migration of $NiSi_2$ precipitates and growth of c-Si.[8] The poly-Si forming below the metal film is called "NIC", as forming outside the metal coverage is called "NILC". The first stage, the formation of $NiSi_2$ precipitates, is a diffusion-controlled process. As for stages (2) and (3), the nucleation and growth of c-Si, they are mediated by $NiSi_2$ precipitates. Crystalline Si nucleates on {111} faces. The crystallization of needlelike Si grains proceeds via the migration of nickel silicides through α-Si. The orientation of needle grain is <111>. Unfortunately, the NILC poly-Si film has intragrain defects and some uncrystallized regions between poly-Si grains. In this study, these defects were reduced by Ni-metal imprint induced crystallization method. In

Ni-metal imprint method, a thin Ni metal layer was deposited on the imprint mold. The mold and α-Si film were then pressed together and annealed at 550°C. The orientation of Ni-metal imprint needle grains is <112>, which differed from that of NILC needle grains <111>.Therefore, the principal goal of this research has been to investigate the performances of TFTs fabricated by <112> and <111> needle grains.

As shown in Table I, two kinds of TFT were used in this study. Samples designated as "111-TFT" were TFTs fabricated from traditional NILC method, whose growth direction of poly-Si grain is <111>, while samples as "112-TFT" were from Ni-metal imprint method, whose growth direction is <112>. The basic processes of 112-TFT were the same as that of 111-TFT.[3] Silicon (100) wafers were used as the substrates. Wet oxide films of 500 nm thickness were grown using a H_2/O_2 mixture at a substrate temperature of 1050°C. Silane-based α-Si films with a thickness of 100 nm were then deposited using a low-pressure chemical vapor deposition (LPCVD) system at 550°C.

For the fabrication of 111-poly-Si, a 2-nm-thick Ni film was selectively deposited on the top of α-Si film, which is followed by crystallization at 550°C. The fabrication of 112-poly-Si is illustrated in Fig. 1. P-type (100) orientation silicon wafers were used to fabricate imprint molds. Stripe patterns were introduced into the molds by etching it with photolithographically generated patterns. The molds were prepared by wet chemical etching using potassium hydroxide (45 wt%) solution at 70°C.[9] A 2-nm-thick Ni film was then deposited on the imprint mold. A 2-nm-thick Ni film was then deposited on

the imprint mold.   The imprint mold and α-Si film were then pressed in a differential thermal expansion apparatus,[10] which was followed by annealing at 550°C for 24 h in argon ambient. The OM image of 112-poly-Si is shown in Fig. 2, the light region is the poly-Si area; the grain growth is very uniform at each imprint site.

  The TFTs were then fabricated by defining the active areas on these two poly-Si films. Channels of TFTs were parallel to the longitudinal grain boundaries. A 100 nm thick SiO_2 film for gate insulator was deposited using plasma-enhance chemical vapor deposition (PECVD). Subsequently, 150 nm poly-Si for gate electrode was deposited using high-density plasma chemical vapor deposition (HDP-CVD). After defined the gate, a self-aligned 35 kev phosphorus ions at the dosage of 5×10^{15} ions/cm^2 were implanted to form source/drain and gate. The implanted dopants were activated by thermal annealing at 600°C for 24h. Finally, a 500-nm-thick SiO_2 film was deposited using PECVD to serve as a passivation layer. Contact holes were opened through the oxide layer, and 500 nm of aluminum (Al) was then deposited as the interconnection. And hydrogen plasma was performed after the TFT devices were fabricated.

Figure 3 shows the SEM and TEM images of 111-poly-Si. Not all α-Si film was transformed to c-Si. Some regions between the needlelike Si grains remained uncrystallized. Lots of branch grains were found. The growth rate was about 4.6 μm/h and the growth direction of needle grain was <111>. The SEM and TEM images of 112-poly-Si are shown in Fig. 4. The diffraction pattern of the grains reveales that the grain orientation (perpendicular to the

film plane) is <111> and the growth direction (parallel to the film plane) of needle grains is <112>. Most of the grains were parallel to each other. Compare with 111-poly-Si, 112-poly-Si had fewer branch grains and less uncrystallized α-Si region, which had been etched away by Secco solution. The growth rate of 112-poly-Si was about 5.3 μm/h, which was higher than that of 111-poly-Si.

After comparison, the different poly-Si growth mechanisms used should be the main cause of the different results. In 111-poly-Si grains, the α-Si right under the Ni layer was completely crystallized to very fine grain sizes (15–20 nm) due to the NIC mechanism.[11, 12] At the edges of Ni layer, Ni silicide nodules moved laterally into the α-Si region and induce the crystallization of α-Si. As for the 112-poly-Si, the Si crystallization mechanism was also mediated by $NiSi_2$ precipitates, which were found in front of the 112-needle grains. However, as illustrated in Fig. 5, there was no need for the formation of NIC grains. Therefore, the 112-poly-Si had faster growth rate. When samples were annealed at 550ºC, lots of the Ni silicides were formed on the faces of the imprint-stripe patterns. These silicide nodules moved into the α-Si region and any α-Si along the path would be crystallized. Therefore, as shown in Fig. 3, not much uncrystallized α-Si region was left. Thus, the growth of branch grains was suppressed by the neighbor major needlelike grains. These extra constrains of NILC growth mechanism might be the reason why the growth direction of our Ni-metal imprint needle grains were along <112>.

Figure 6 and Table II show the transfer characteristics of 111-TFT and 112-TFT. The performance of 112-TFT was far superior to that of 111-TFT. Compared with 111-TFT, the field-effect mobility (μ_{FE}) were increased by a

factor of 2.6 from 44 to 117 cm^2/V-s, and the on/off current ratio (I_{on}/I_{off}) by a factor of 4 from 2.29×10^5 to 9.23×10^5. The leakage current (I_{off}) was reduced from 13 to 5.47 pA/μm.

As mentioned earlier, some α-Si regions remained among the poly-Si grains. These regions trap charge carriers and constitute potential barriers to the flow of carriers. The presence of the potential barriers and the additional scattering at the boundaries degrade the mobility.[13,14] As shown in Figs. 3 and 4, 112-poly-Si had less α-Si region than 111-poly-Si. Therefore, 112-TFT had higher μ_{FE}, higher I_{on}/I_{off}, smaller subthreshold slope (S) and lower threshold voltage (V_{th}) than 111-TFT.

Besides the effect of α-Si region, the orientation of grain boundaries will also affect the performance of TFTs. In a previous study, Chao *et al.*[3] found that NILC-TFT (111-TFT) exhibit enhanced performance compared with SPC-TFT. This was because that SPC poly-Si had a columnar grain structure with grain boundaries randomly oriented with respect to the direction of drain current (I_d).[14] These grain boundaries trapped charge carriers and built up potential barriers to the flow of carriers. The presence of these grain boundaries degraded μ_{FE}, S and V_{th}. This degradation could be improved by using 111-poly-Si because lots of its longitudinal grains and their boundaries were parallel to I_d hence less impeding to carrier flow. In this study, as illustrated in Fig. 7, the arrangement of 112-poly-Si grains was even better than that of 111-poly-Si grains. All 112-poly-Si grains and their boundaries were parallel to each other with the exception of very few branch grains between them. Therefore, the performance of 112-TFT was far superior to that of 111-TFT.

Thin-film transistors fabricated by <111> and <112> needle grains have been investigated. 111-poly-Si grains were fabricated by NILC method, while 112-poly-Si by Ni-metal imprint method. It is found the performance of 112-TFT was far superior to that of 111-TFT. Compared with 111-TFT, the field-effect mobility (μ_{FE}) was increased by a factor of 2.6 from 44 to 117 cm^2/Vs, and the on/off current ratio (I_{on}/I_{off}) by a factor of 4 from 2.29×10^5 to 9.23×10^5. The leakage current (I_{off}) was reduced from 13 to 5.47 pA/µm. This improvement is because that 112-poly-Si had fewer branch grains and less uncrystallized α-Si region than 111-poly-Si. Besides, all 112-poly-Si grains and their boundaries were parallel to each other with the exception of very few branch grains between them.

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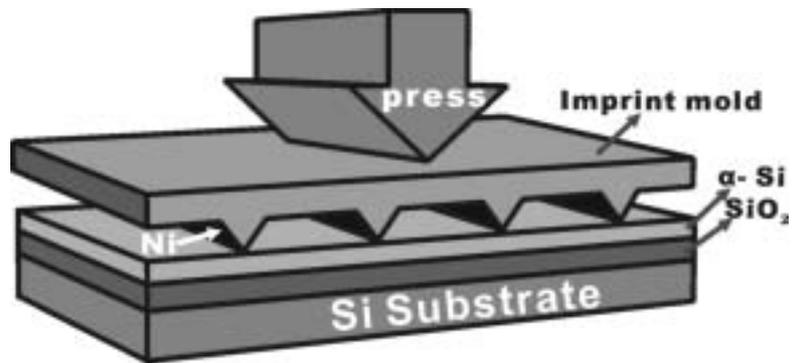
Fig. 1 Schematic illustration of Ni-metal imprint method.
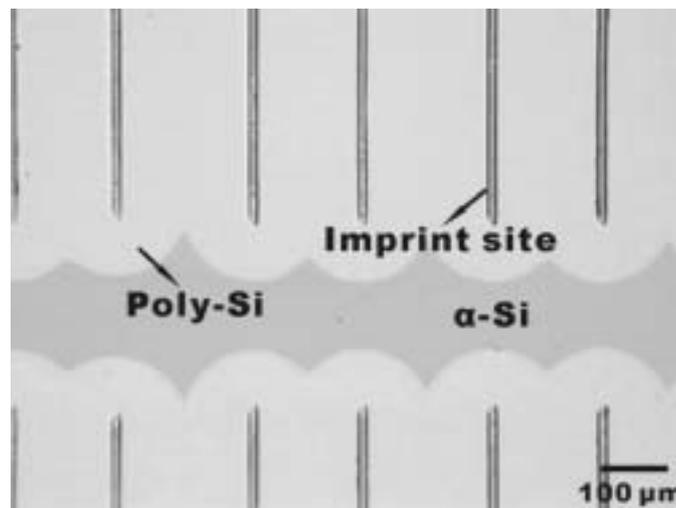
Fig. 2. Optical microscopy image of 112 - poly-Si annealed at 550°C for 24 h.
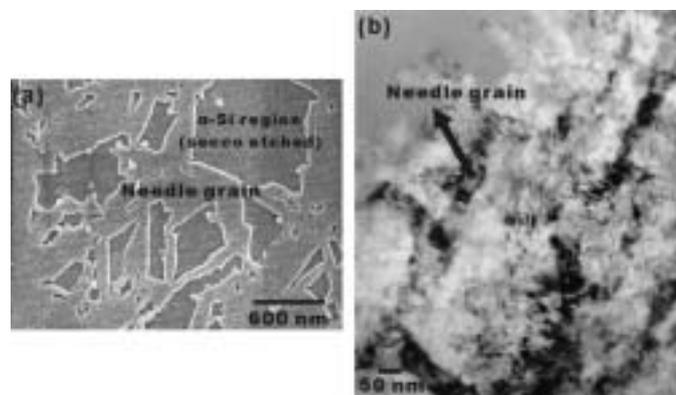
Fig. 3 (a) SEM image of Secco-etched 111-poly-Si film and (b) TEM image of 111-poly-Si film.
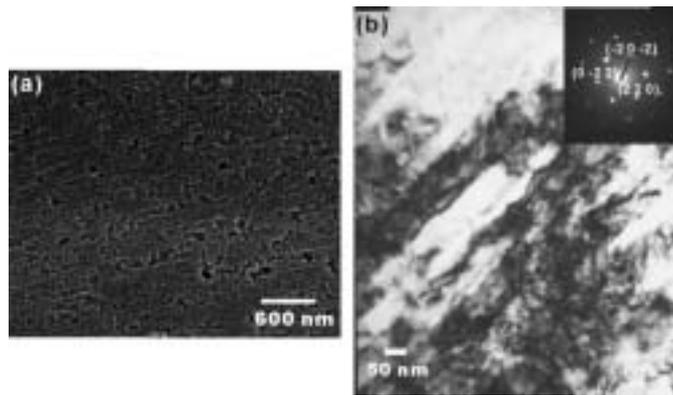
Fig. 4 (a) SEM image of Secco-etched 112-poly-Si film and (b)TEM image of 112-poly-Si film. Compared with 111-poly-Si, 112-poly-Si had fewer branch grains and less uncrystallized α-Si region. The preferred direction of needle grain was <112>, which differed from that of 111-poly-Si grains <111>.
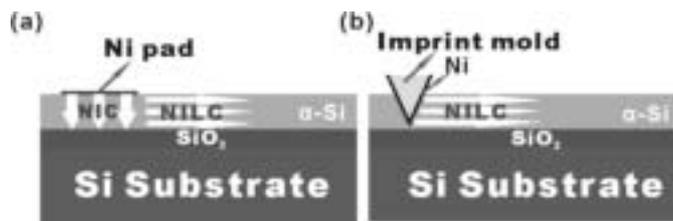
Fig. 5 Schematic illustration of the growth mechanisms of (a) 111 - poly-Si and (b) 112 - poly-Si grains.
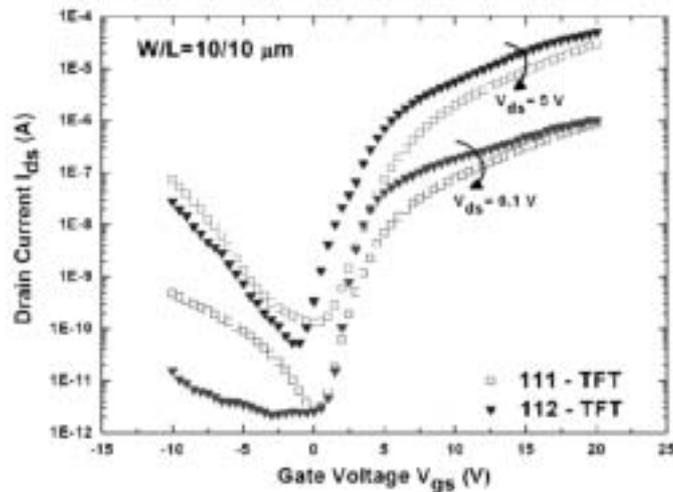
Fig. 6 Typical I_{DS}-V_{GS} transfer characteristic of 111 - TFT and 112 - TFT.
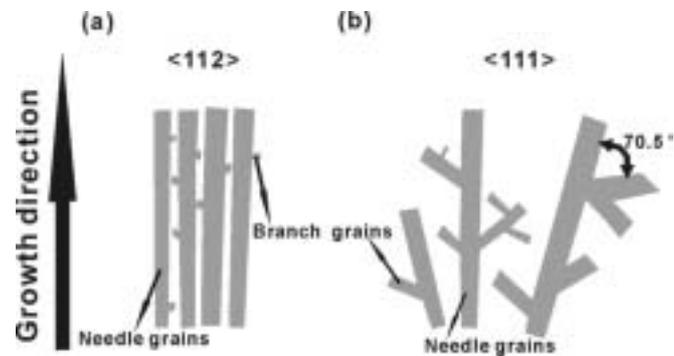
Fig. 7 Schematic illustration of the growth of needle grains: (a) 112 – poly-Si and (b) 111-poly-Si grains. All 112-poly-Si grains were parallel to each other with the exception of very few branch grains between them.

Table I The specification and fabrication method of 111-TFT and 112-TFT.

	Fabrication method
111- TFT	Traditional NILC
112- TFT	Ni-metal imprint

Table II Device characteristics of 111-TFT and 112-TFT.

W/L=10/10	111 - TFT	112 - TFT
Mobility(cm^2/V-s)	44	117
on/off current ratio (10^5)	2.29	9.23
Minimum leakage current /channel width(pA/µm)	13	5.47
Subthreshold slop (V/dec)	0.56	0.33
Threshold voltage (V)	3.36	2.54

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