行政院國家科學委員會專題研究計畫　期中進度報告

運用掃描式探針顯微鏡研製與分析矽奈米電子元件(2/3)

計畫類別：個別型計畫
計畫編號：NSC93-2215-E-009-080-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學奈米科技研究所

計畫主持人：許鉦宗

報告類型：精簡報告
報告附件：出席國際會議研究心得報告及發表論文
處理方式：本計畫可公開查詢

中　華　民　國 94 年 5 月 23 日

國家科學委員會研究計畫--期中精簡報告

運用掃描式探針顯微鏡研製與分析矽奈米電子元件(2/3)

Fabrication and Characterization of Silicon Nanoelectronic Devices with Scanning Probe Microscope

計畫編號：**NSC 93—2215-E-009-080**
執行期限：93 年 8 月 1 日至 94 年 7 月 31 日

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一、中文摘要

本研究擬利用掃描式探針顯微鏡在(100)絕緣矽(SOI)矽晶基材上研製矽奈米電子元件：奈米記憶元件與奈米電晶體。奈米記憶元件的主結構是用掃描式探針顯微鏡將矽轉換成奈米級矽氧化物，以此矽氧化物做為蝕刻罩幕(Mask)進行非等向性溼式蝕刻後產生矽奈米線為基礎。由於掃描式探針顯微鏡在<110>方向產生氧化物後，經非等向性溼式蝕刻會產生錐形(taper)矽奈米線，而在<100>方向產生的氧化物經非等向性溼式蝕刻後，會產生垂直(vertical) 側邊矽奈米線。依此特性我們控制探針先在<110>方向產生氧化物，之後改變探針氧化方向到<100>晶向，然後再改回<110>方向繼續氧化矽基材。經由非等向性溼式蝕刻後可得到矽奈米線，而矽奈米線中段部分是擁有垂直側邊的。之後在矽奈米線覆蓋上一層數十奈米的多晶矽(polysilicon)，用乾式進行間隔層蝕刻(spacer etching)，在<100>晶向矽奈米線的兩側會產生多晶矽奈米點，我們便可以利用電子穿隧進出這兩個懸浮的多晶矽奈米點來操控奈米記憶元件。而奈米電晶體也是以矽奈米線為基石，我們利用其中一條矽奈米線做為通道(channel)，兩條垂直於通道的矽奈米線做為閘極，當這兩個閘極矽奈米線的間距很小時，由於閘極外加電場將通道形成兩個空乏(depletion)區可以夾出一矽奈米點，我們即可以控制通道兩端的電壓來操作電子的穿隧。我們將觀察不同溫度(12K~300K) 時矽奈米電子元件的存取穩定性、電流/電壓特性、穿隧現象等等。。

關鍵詞：掃描式探針顯微鏡、絕緣矽、矽奈米線、奈米電子元件、非等向性溼式蝕刻、間隔層蝕刻、穿隧現象。。

Abstract

This research project focuses on fabrication and measurement of silicon nanoelectronic devices, including nanomemory device and single electron transistor (SET), on (100) SOI silicon wafer. The main structure of nanoelectronics is fabricated with scanning probe microscope (SPM); the hydrogen terminated silicon surface can be transferred into silicon oxide when a bias is applied between the SPM tip and the substrate. The oxide was then used as mask in orient dependent wet etching to generated silicon nanowires (SiNWs). When oxide nanopatterns were generated along <110> then <100> and back to <110>, nanowire with taper sidewall is obtained for <110> direction and nanowire with vertical sidewall in <100> direction after anisotropic wet etching. Deposition of thin poly silicon film of tenth of nanometers on the nanowires followed by the spacer etching, two polysilicon floating nanodots on the side of nanowire in <100> direction is expected. The tunneling of electrons into the nanodots gives us the control of the device as the “flash memory” in nanometer scale. The SET is also formed with SiNWs. When one of SiNW is uased as channel, two perpaticular SiNWs with bias are used as

side gates. Control of the pitch between two side gates will generate two depletion regions and a silicon nano island. With the control of source/drain voltage and the gate voltage, tunneling of electrons through depletion regions into nano island can be observed. In this study, memory read/write propteries, I-V characteristics and tunneling phenomenon will all be observed.

Keywords: Scanning probe microscope, SOI, silicon nanowire, nanoelectronics, anisotropic etching, spacer etching, tunneling.

二、Background and objective

依據莫爾定律(Moore's Law)和國際半導體技術(ITRS)的推估，到公元 2015 年時，以矽基材為主的積體電路技術，無論是記憶體元件或是中央處理器元件，均將進入 30 奈米或更小的世代。除了有機材料、分子電子元件、與 III-V 族材料在奈米光電的研究之外，矽材料在奈米光電元件發展的遠景似乎持續吸引著絕對多數研究者的目光。在主觀上這主要來自下列兩大原因：首先是 CMOS 製程技術在廿一世紀將走入 100 奈米以下，而多樣且推陳出新的奈米製作技術提供了先進矽奈米光電元件衍生的平台。其二是矽奈米光電元件和原來 CMOS 製程技術間的匹配沒有太多問題，而強大的軟、硬體製程架構(Infrastructure)更是其他技術無法比擬。尤其是要製造出 Tera 數量級的積體電路，矽技術可能是唯一較有經驗的。從技術與材料特性的角度來看，矽擁有下列符合奈米元件製造的優點：

1. 矽/二氧化矽介面能提供有效且高品質的位能障，即使在常溫也能有效將電子限制在矽奈米結構中。
2. 矽/二氧化矽的介面十分穩定，能讓玫奈米單電子元件的操作避開移動電荷(mobile charge) 產生的 offset 問題。這是許多其它材料很難解決的。
3. 矽的奈米結構大小很容易用熱氧化的方式加以控制。
4. 眾多且完整的矽奈米製作技術可供使用，與 VLSI 技術匹配。

當半導體元件達到 25 奈米時，中央處理器(CPU)的工作速度可以推到 100GHz，記憶體儲存容量可達 1000GB。半導體導線的寬度縮小到幾十奈米時，原先電阻的觀念因電導(Conductance)量子化而不再適用；當半導體元件導線長度縮小到幾十奈米時，因電子在行徑上和晶格缺陷撞擊的機會變得非常小，使得電子在導線中的傳導十分迅速。另外，當材料被製成長、寬、高都在幾十奈米時，因能階形成量化現象，只要少數的電子就會將其填滿，因此元件工作與操控只需要少數的電子即可。因此，目前的半導體元件無論技術本身或是元件模型均會遭遇問題，因此從元件製作、元件模擬模型建立到奈米積體電路設計等等都變得十分重要。

奈米電子元件製造技術的開發，一直為許多研究單位的研究重心，1994 年 Stanford 大學固態研究室的 H. I. Liu，利用電子束微影蝕刻技術與高溫氧化方式，首先製造出線寬 5 奈米單晶結構矽奈米線，但是缺乏電特性的分析。[1] 1998 年 Cambridge 大學利用相同的微影蝕刻技術製造出縣線寬 60 奈米的多晶矽奈米線，再進一步使用高溫氧化，使得奈米線線寬微縮至 30 奈米，而電流特性隨兩側閘電極的電壓變化而變化。[2] 利用相同技術，1999 年德國研究單位，於絕緣層上矽晶片(SOI)，製作出線寬 15 奈米的單晶矽奈米線，並且加上上方閘電極，使得此矽奈米線，出現 Coulomb- blockade 電流特性，此電流特性為單電子電晶體(SET)重要性質。[3]

另一項製造奈米線的技術為汽態-液態-固態三態轉變方式(Vapor–Liquid-Solid, VLS method)成長單晶矽奈米線，成長機制

理論於 1964 年，由 R. S. Wanger 等人提出，2000 年 UCLA 利用 VLS 方法製造線寬約 15 奈米的奈米線，並且發現電流特性與先前技術差異。[4] 1997/998 年 Princeton 和 Cambridge 大學，分別利用 Nanoimprint 和電子束微影技術，製做出類似 SET 與 CMOS 結構的單電子記憶體元件。[5,6] 2001/2002 年韓國研究團隊，利用空乏的結構，製做出具有 Coulomb- blockade 電流特性的單電子元件。[7,8] 2002 Princeton 電機系的研究團隊以 nanoimprint 的技術研製超快矽奈米元件。[9] 雖然奈米級的電子元件，已經可以製造，絕大多數在奈米電子方面的研究或是製作方式都是採用立體方式，也就是說其控制閘或懸浮閘均位於載子通道的正上方，研製過程十分困難，同時多數只能夠於低溫時操做。因此，如何將元件推向室溫操作，新結構的量子元件設計，與新奈米製程技術的開發，將為奈米級電子元件突破的重點。

三、Experiments and Results

The substrate used in the experiment was a p-type SOI (100) wafer that was ion implanted with boron at 15 keV with a dose of 10^{14} atoms/cm^2. To activate the boron implanted layer the wafer was annealed at 950 ˚C for 4 h. The result was a p-type SOI sample where the top 30 nm was boron implanted. Lithography was carried out by first passivating the silicon surface with hydrogen by dipping the sample in 5% diluted HF solution for 20-30 s. This passivation was typically effective for at least 1 h. The average surface roughness of the H-passivated films measured by AFM is around 0.5 nm. Scanning probe lithography was performed in ambient with the cantilevers coated with PtIr. The relative humidity kept at ~60 % and at room temperature. The nano-oxidation masks were formed by applying a bias voltage of -6.5 V on the tip with respect to the sample [5, 6]. Typical set point force and writing speed are 1 nN and 1 μm/sec, respectively.

After AFM nano-oxidation, the sample is etched in 25 wt % TMAH at temperature 40 ˚C [7]. The oxide serves as an etch mask and the surrounding unprotected silicon is etched off leaving the silicon nanowire. An etching time of 3 min was chosen to ensure that the surrounding silicon etched away without attacking the pattern itself significantly. An AFM image of a silicon nanowire is shown in Figure 1 (a). The height of the structure is 30 nm and the linewidth is 60 nm.

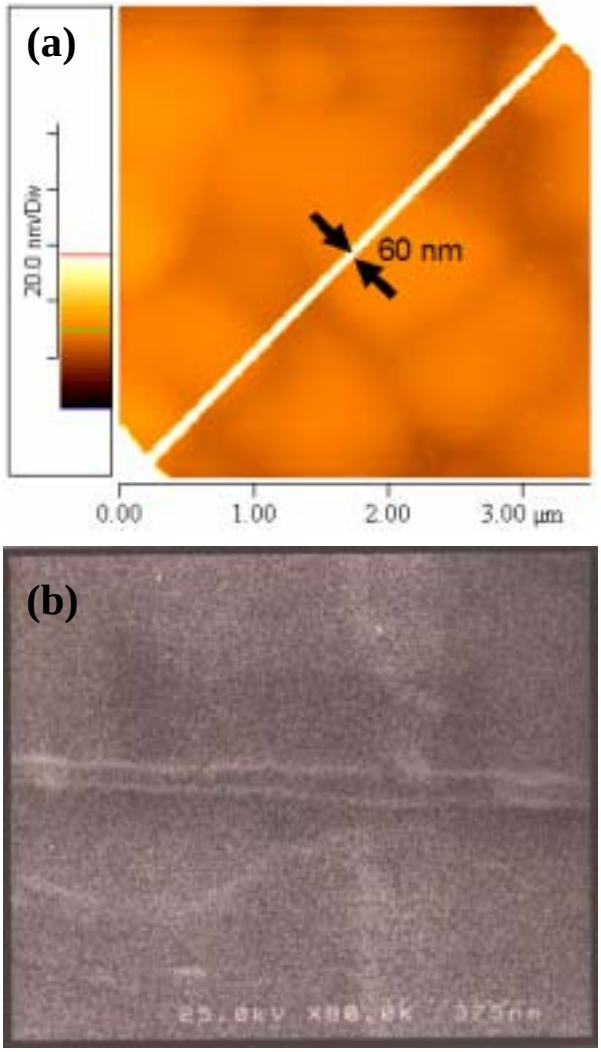

Figure 1: (a) The AFM image of the silicon nanowire which is 30 nm in height, 60 nm in width, 4 μm in length after 25 wt % TMAH etching at temperature 40 ˚C for 3 min with oxide mask generated by SPL. (b) The SEM image of the silicon nanowire.

A 500 Å thick Nickel films were deposited on silicon nanowire using electron-beam evaporation. The samples were etched with 5% diluted HF solution to remove the native oxide on silicon nanowire

before loading into the evaporation chamber. The evaporation rate was about 5 Å/s in a vacuum of 3×10^{-6} Torr. After the metal deposition, the NiSi nanowire was formed by rapid thermal annealing (550 ˚C for 120s) in nitrogen ambient [8]. The unreacted metal on oxide was removed by a selective etching solution (HNO_3:H_2O=7:1) at room temperature for 3 min, to aviod attacking the silicide, oxide or silicon. Three kinds of nanowires were formed in our experiment: silicon nanowire without depositing Ni, silicon nanowire with half NiSi, and NiSi nanowire. Finally, the electrode was deposited: Ti/Au. The Ti/Au electrodes were made with 20 nm of Ti adhesive layer and a 250 nm of Au. The metal electrodes were formed by a lift-off process.

1 RESULTS AND DISSUSION

Before forming the silicide nanowire, we optimize the conditions of annealing temperature, thickness of Ni film, and silicon consumption rate, which are all very important for the formation of NiSi. Table 1 shows the sheet resistance and film resistivity of Ni film and NiSi film, respectiveily. It is observed that the NiSi film has the lowest sheet resistance and film resistivity. This result is consistent with the previous reports (14~20 μΩ-cm) [3]. The 2.22 nm NiSi needs to consume 1 nm Ni and 1.84 nm silicon [9], so a 50-nm-thick Ni films is deposited on silicon nanowire and SiNW is transfered into NiSi nanowire by annealing.

	Si	Ni	NiSi
Rs(Ω/□)	4.55 K	4.62	2.27
ρ(Ω-cm)	194.8 m	38.6 μ	19μ

Table 1: The sheet resistance and film resistivity by the four point probe analysis

To assess the electrical characteristics of the p-type silicon nanowire, FET devices were fabricated using standard procedures with back gate geometry [10]. In addition, the metal/semiconductor contact plays a key issue in studying the electrical properties of semiconducting nanowire. To reduce the contact resistance, Ti is deposited to remove intrinsic SiO_x on silicon nanowire and to form the low resistive $TiSi_2$ above 600 ˚C and has been proven to have good contact with both p- and n-type silicon nanowire. Figure 2(a) shows the typical I_{ds} versus V_{ds} characteristics obtained from a p-type SiNW-FET with Ti/Au electrods. The two-terminal I_{ds}-V_{ds} measurements are linear for different bias values of V_{gs}, which indicates that the metal/semiconductor interfaces are ohmic contacts. In the measurement, we observed that the positive V_{gs} almost induces no current, and the current increases dramatically when appling negative V_{gs} (V_{gs} from 5V to -5V). In Figure 2(b), sweep of the V_{gs} demonstrates that the silicon nanowire is p-type.

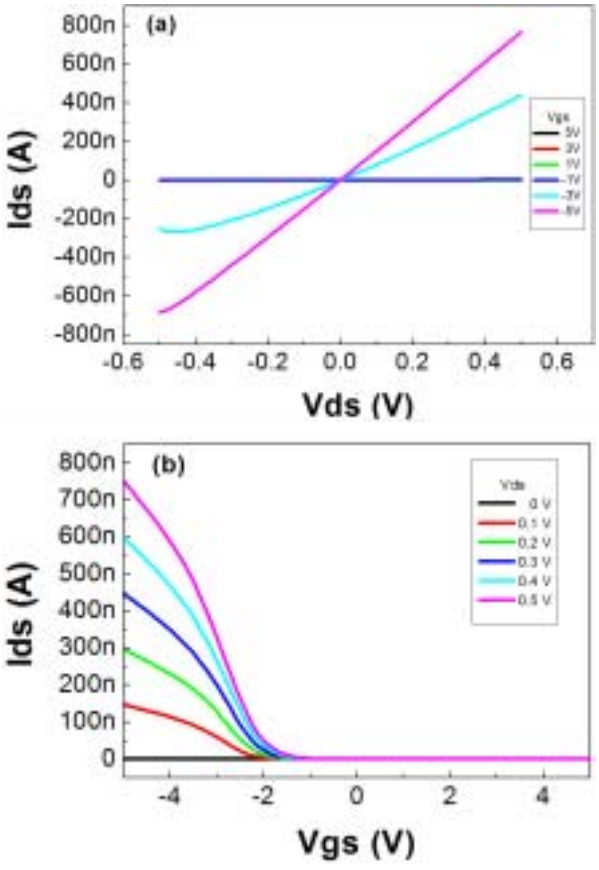

Figure 2: (a) Typical I_{ds} versus V_{ds} curves of a 60 nm wide p-type silicon nanowire device. The gate voltage for each I_{ds}–V_{ds} curve is indicated. (b) I_{ds} versus V_{gs} curves recorded

on the same silicon nanowire device with V_{ds} swept from 0V to 0.5V.

Although some groups report an integrated contact and interconnection solution that overcome this size constraint through selective transformation of silicon nanowires into metallic nickel silicide nanowire [11]. Previous investigation of metal silicides can exhibit low resistivity, compatibility with conventional silicon manufacturing, and the ability to form contacts to both p- and n-type silicon. For this reason, we produce the NiSi nanowire by annealing the Ni-metal-coated silicon nanowire at 550 ˚C for 120s in nitrogen ambient. In Figure 3, electrical properties of a 60 nm diameter NiSi nanowire shows highly linear current on I_{ds} versus V_{ds} in two-terminal measurement. The current of NiSi nanowire is high in comparison to the silicon nanowire; indicating that the NiSi nanowire has a very low resistivity. In addition, the back gating effects are not clearly visible for the NiSi nanowire when we applying different gate voltages (0V to -5V). These results show that the NiSi nanowire exhibits metallic characteristic. Finally, we also fabricated nanoscaled-Schottky barrier junction by forming a NiSi/Si heterojunction in silicon nanowire. A half of silicon nanowire was coated with photoresist. The sample was deposited with an e-beam evaporator for a 60 nm Ni film. After lift-off, the samples were annealed and etched as described above. The Figure 4 shows the I_{ds} versus V_{ds} characterictics by two-terminal measurement. Current rectification has been observed clearly in NiSi/Si heterojunction, and nanoscaled-Schottky barrier junction can be formed through proposed technique. The result indicates that nanoscaled-Schottky diodes have an on-off current ratio of nearly 10^3, which exhibits a very similar behavior to bulk Schottky barrier junctions.

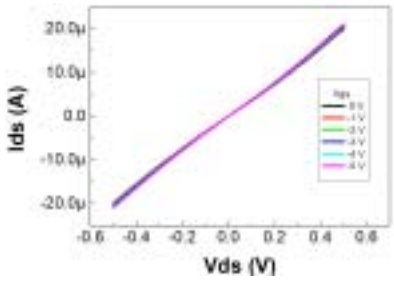

Figure 3: Typical I_{ds} versus V_{ds} curves of the 60 nm wide NiSi nanowire device. The gate voltage for each I_{ds}–V_{ds} curve is indicated.

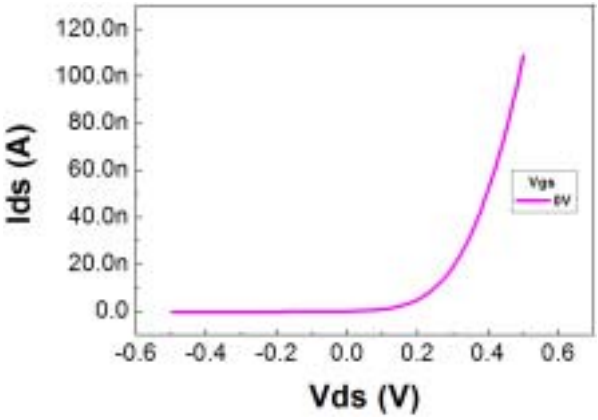

Figure 4: Typical characteristics of I_{ds} versus V_{ds} of the Schottky barrier junction (NiSi/Si) in a 60 nm wide nanowire.

2 SUMMARY

We have successful fabricated the 60-nm wide silicon nanowire by using the scanning probe lithography and followed by TMAH wet etching. And, low resistivity NiSi (19μΩ-cm) was confirmed with the condition at 550 ˚C for 120s in nitrogen ambient. Then, the nickel silicide nanowires show very low resistivity and large conductive current in comparison to the silicon nanowires were observed. Finally, the nanowire with nanoscaled-Schottky barrier junction (NiSi/Si) was formed by above approach and exhibits rectifying transport property. It is believed that the nanoscaled-Schottky junction is very useful in many future

applications of nanoelectronics.

四、Acknowledgements

This program is supported by the National Science Council under the contract number NSC 93-2215-E-009-080.

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