行政院國家科學委員會專題研究計畫　期中進度報告

高度微縮金氧半場效電晶體機械應力效應之研究(2/3)

計畫類別：個別型計畫
計畫編號：NSC93-2215-E-009-024-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學電子工程研究所

計畫主持人：陳明哲

計畫參與人員：許義明，林盈秀，陳榮廷

報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 94 年 5 月 25 日

行政院國家科學委員會補助專題研究計畫期中進度報告

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計畫類別：▒個別型計畫　　□整合型計畫

計畫編號：NSC 93-2215-E-009-024-

執行期間：93/08/01 ~ 94/07/31

計畫主持人：陳明哲

計畫參與人員：許義明, 林盈秀, 陳榮廷

成果報告類型(依經費核定清單規定繳交)：▒精簡報告　□完整報告

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執行單位：國立交通大學電子工程學系

中　華　民　國　94　年　5　月　25　日

行政院國家科學委員會補助專題研究計畫期中進度報告

高度微縮金氧半場效電晶體機械應力效應之研究(2/3)

The Impact of Mechanical Stress in Highly Scaled MOSFETs (2/3)

執行期限: 93/08/01 ~ 94/07/31

計畫編號: NSC 93-2215-E-009-024-

主持人：陳明哲教授　　國立交通大學電子工程學系

一、中文摘要

本計畫探索下世代場效電晶體機械應力效應之嶄新領域，將配合當年度互補式金氧半場效電晶體製程技術演進同時執行八大項目：

1．以當年度最先進製程製作 n- and p-型 高度微縮金氧半場效電晶體元件，以金氧半場效電晶體微縮尺寸和閘極至淺槽隔離邊緣距離二者為圖案變動參數。 進行電流電壓/電容電壓量測。以自行發展的一維量子力學模擬器與實驗比較以萃取重要製程參數。

2． 執行二維製程及機械應力之模擬以萃取張力之分佈，大小並決定其性質。

3． 定義不同機械應力條件即將萃取得到的張力大小表達為不同製程參數，不同場效電晶體微縮尺寸，和不同閘極至淺槽隔離邊緣距離的函數。

4．以自行發展的量子力學模擬器計算不同機械應力條件下反置通道二維電子(洞)氣及次能帶分佈，以獲得遷移率等重要參數。建立機械應力之理論架構並導出張力解析模式。

5．低溫實驗萃取通道彈道傳輸係數以與機械應力作一關聯。

6．二維量子力學彈道傳輸模擬器之程式撰寫,除錯及執行。

7．低頻雜訊及電報雜訊量測以偵測機械應力之細微變化。

8．機械應力效應置入電路模擬器場效電晶體模式並進行電路功能方塊模擬。

本計畫目的即為藉著上述執行項目以肇清機械應力對下世代場效電晶體元件性能之效應及介觀物理機制，另方面將機械應力效應置入電路模擬器場效電晶體模式以進行正確的積體電路設計，進而使得系統單晶片積體電路設計複雜化及高密度化能有效解除機械應力之威脅。

關鍵詞：場效電晶體；機械應力；張力；二維電子氣；二維電洞氣；通道彈道傳輸；低頻雜訊；電報雜訊；模式；積體電路設計。

英文摘要

The project explores the mechanical stress issue on the highly scaled MOSFETs. Following are the eight main items to be conducted along with state-of-the-art CMOS scaled technologies:

1. Fabricate n- and p-type highly scaled MOSFETs by advanced process technologies, followed by I-V/C-V characterization as well as our developed 1-D quantum mechanical I-V/C-V simulation to extract key process parameters.
2. Perform a two-dimensional process/mechanical stress simulator to extract the magnitude and distribution of strain and determine its property.
3. Experimentally define mechanical stress conditions in terms of strain expressed as function of process parameters, FET scaling factor, and distance between gate to STI (shallow trench isolation) edge.
4. Perform our developed 1-D quantum mechanical simulators to assess 2-dimensional electron (hole) gas and sub-band distributions, leading to extraction of relevant parameters like mobility. Establish theoretical framework of mechanical stress and develop analytic model of strain.
5. Perform low-temperature experiment to extract channel backscattering coefficients and relate them to mechanical stress.
6. Establish 2-D quantum mechanical ballistic simulators.
7. Perform low frequency noise and random telegraph signal experiment to detect some change in mechanical stress.
8. Incorporate mechanical stress into SPICE MOSFET model and perform simulation on functional circuit blocks.

The goal of the project is to clarify the impact of mechanical stress on next generation MOSFETs and the underlying mesoscopic physical mechanisms. Meanwhile, incorporation of mechanical stress into SPICE MOSFET model enables correct IC design and as a result, we can reach a a complex, highly dense SOC design effectively free of the harmful mechanical stress.

Key Words：*MOSFET; Mechanical Stress; Strain; 2-Dimensional Electron Gas; 2-Dimensional Hole Gas; Channel Ballistic Transport; Low-Frequency Noise; Random Telegraph Signal; Model; IC Design*

二、緣由與目的

依照 International Technology Roadmap for Semiconductors，在下世代 Silicon CMOS 製程技術演進過程當中， MOSFET 尺寸持續微縮且 Gate 極亦持續更為靠近 STI(Shallow Trench Isolation)邊緣，衍生的機械應力(Mechanical Stress)已有文獻報告對元件推動電流產生衰減或其他影響，此問題對於積體電路設計複雜化及高密度化之趨勢(尤其是系統單晶片設計 SOC)不利，故以機械應力效應為議題的研究最近在國際上受到高度重視。

我們過去數年經驗的累積反映出一個有系統的嚴謹性的機械應力效應研究是十分緊迫的，此為本計畫提出之背景：

1 在我們最近發表的創見性的一超大型級之測試載具晶片，內含有一連串高敏感度之測試結構，用以偵測超大型晶片在不同製程技術製造下之可靠度分析，並提出一新的應力模組理論，來估算晶片故障分布與故障機構模式。結果呈現超大型晶片故障之韋博統計分布與晶片幾何大小，封裝材料相關。此外由應力分析模擬和針壓實驗，我們找到一最佳抗應力緩衝層鍍於輸出入墊片上方。再將靜電放電保護元件及環狀振盪電路置於輸出入墊片下方。在傳輸線脈衝高壓測試下,輸出入墊片下之靜電放電保護元件的二次崩潰電壓和電流曲線仍具優秀的特性。而在直流與交流實驗測試下，輸出入墊片下之環狀振盪電路的傳播延遲時間仍然保留在大約 20 微微秒左右。

2．本研究群這幾年已自行發展出 1-D 量子力學(Quantum Mechanical) I-V/C-V numerical 模擬器， 能計算出 Inversion Channel 因 Quantum Confinement 效應引致的二維電子氣(2DEG)或二維電洞氣(2DHG)及其 Sub-bands 分佈大小等。本計畫將此基礎延伸至 2-D Quantum Mechanical Ballistic 模擬器程式撰寫,除錯及執行以反映最近趨勢。

3.萃取 Channel Backscattering Coefficients 的低溫實驗方法已在 2002 IEDM 發表。

4.本研究群亦已成功建立高度靈敏低頻雜訊量測系統及時域擾動量測系統。

本計畫目的即肇清機械應力對下世代 FET 元件性能之效應及介觀物理機制，另方面將機械應力效應置入 SPICE MOSFET Model 以進行正確的 IC Design，進而使得 SOC 積體電路設計複雜化及高密度化之同時，能有效解除機械應力之威脅。

三、研究方法與成果

1.我們在 Highly Scaled MOSFETs (即以 MOSFET 微縮尺寸和 Gate 極至 STI 邊緣距離二者為 Layout 變動參數)上量測不同機械應力條件下之 I-V 特性，實驗發現機械應力確會降低 n-Channel MOSFETs 元件推動電流但增加 p-Channel MOSFETs 元件推動電流，與文獻上發表者 不同。

2.完成量子力學 I-V/C-V 模擬與實驗比較並萃取重要參數如 poly doping, substrate doping, flatband voltage，有效氧化層厚度。

3.完成二維製程及機械應力之模擬並萃取決定 Strain 之分佈，大小，性質。

4.完成萃取得到的 Strain 大小表達為不同製程參數，不同 MOSFET 微縮尺寸，和不同 Gate 極至 STI 邊緣距離的函數。

5.Currently we are calculating 量子力學模擬計算不同機械應力條件下 Inversion Channel 二維電子(洞)氣及 Sub-bands 分佈，並獲得 Mobility 等重要參數。

6. Currently we are improving Mechanical Stress 之理論架構建立並導出 Strain 解析模式。

7. Currently we are conducting scattering 實驗萃取 Channel Backscattering Coefficients 並與 strain 應力作一 Correlation。

四、結論與討論

1. Mechanical stress effects in highly scaled MOSFETs currently are examined both experimentally and theoretically。

2. Process-device coupled simulations have been used as probe of mechanical stress for a wide range of process and device parameters。

3. Striking linkage between experiment and simulation has been successfully established。

4. Self-consistent Schroedinger-Poisson solver has been developed to study the mechanical stress and strain related issues。

5. Now the mechanical stress issue has been extended to the re-distribution of underlying doping profile。(The tensor effect is a key factor!!)

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2. Y. M. Sheu, Kelvin Y. Y. Doong, C. H. Lee, M. J. Chen, C. H. Diaz, "Study on STI Mechanical Stress Induced Variation in 90-nm CMOSFETs," *IEEE International Conference on Microelectronic Test Structures*, pp. 205-208, 2003.
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6. 未來數月將進入系列成果產出階段，請拭目以待。

Important Figures and Tables

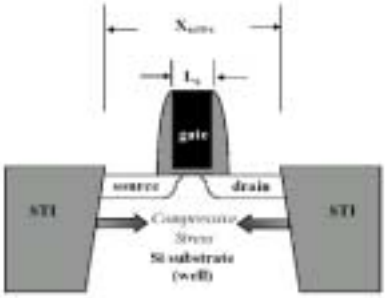


Fig. 1. Schematic cross section of the device along channel length direction with active area size X_{active} and gate length L_g both as parameters. The stress condition is compressive mainly because of the lower thermal expansion rate of STI oxide compared to silicon, and the thermal gate oxidation-induced volume expansion at the STI edge.

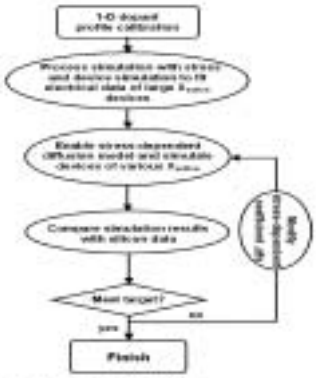


Fig. 2. Flow chart of the modeling procedure.

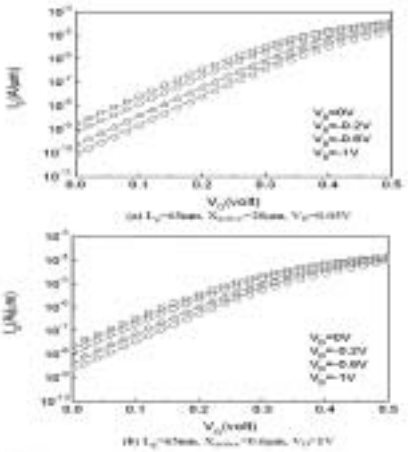


Fig. 3. I–V calibration result of a short-channel nMOSFET with large X_{active} for (a) V_D = 0.05 V and (b) V_D = 1 V. L_g = 65 nm and X_{active} = 10 μm. Symbols stand for the silicon data. Solid lines are the calibrated simulation result.

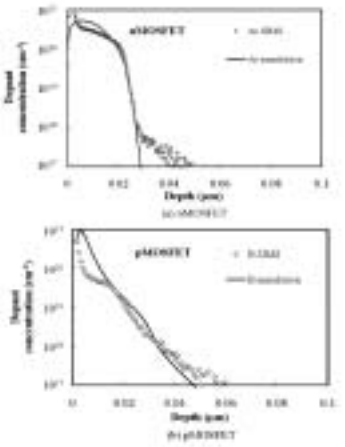


Fig. 4. SIMS and calibration results of 1-D dopant profile for (a) nMOSFET and (b) pMOSFET.

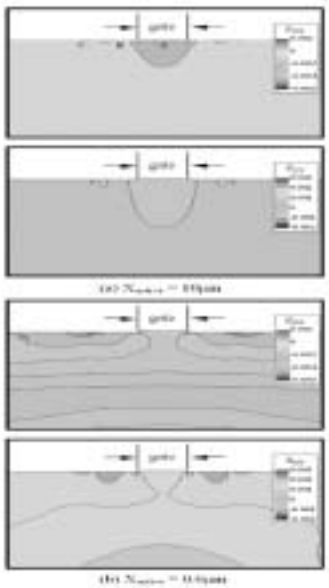


Fig. 5. Simulated strain distribution in the silicon of entire front-end process for 4-μm 65 nm (a) X_{active} = 10 μm (b) X_{active} = 0.6 μm. A small X_{active} causes a much higher strain.

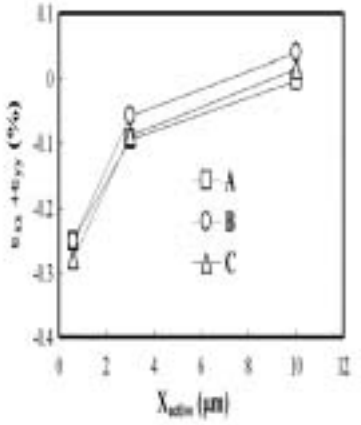
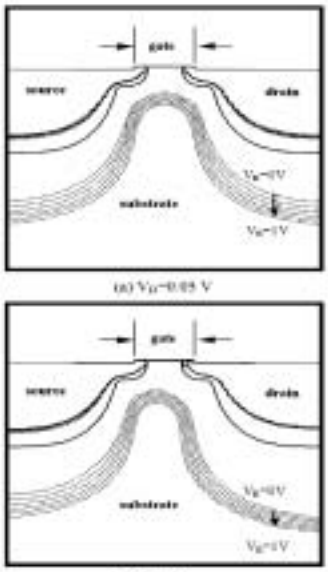


Fig. 6. Magnitude of strain versus X_{active} corresponding to three points A, B, and C in Fig. 4.



(a) V_D=0.05 V

(b) V_D=1 V

Fig. 7. Depletion region boundaries with substrate bias V_B for 65-nm nMOSFET at (a) V_D = 0.05 V and (b) V_D = 1 V.

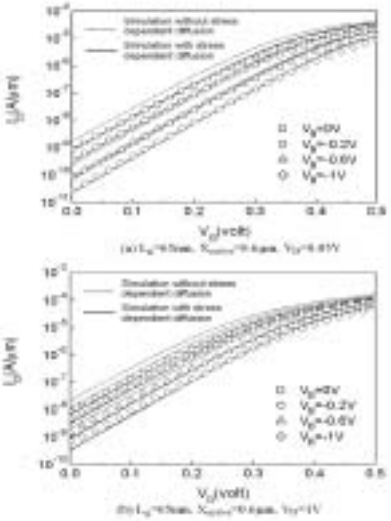


Fig. 8. *I–V* comparison among experimental data, simulation without stress-dependent diffusion model, and simulation with stress-dependent diffusion model for a small X_{active} MOSFET at (a) V_D = 0.05 V and (b) V_D = 1 V. L_g = 65 nm and X_{active} = 0.6 μm. Symbols stand for the silicon data. Dashed lines are the simulation without stress-dependent diffusion model. Solid lines are the simulation with stress-dependent diffusion model.

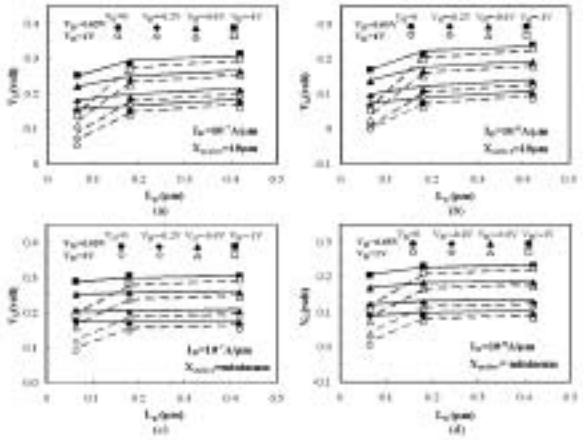


Fig. 9. Comparison of experimental and simulated nMOSFET V_{th} at different I_{th} level for various L_g and X_{active}. Minimum X_{active} for L_g = 65 nm is 0.6 μm, for L_g = 0.10 μm is 0.74 μm, and for L_g = 0.42 μm is 1 μm. Fitted set of dopant diffusion parameters can model MOSFETs of different X_{active} under various drain voltages and substrate biases. Symbols stand for silicon data. Solid lines represent simulations with stress-dependent diffusion model. (a) I_{th} = 10^{-7} A/μm, X_{active} = 10 μm. (b) I_{th} = 10^{-8} A/μm, X_{active} = 10 μm. (c) I_{th} = 10^{-7} A/μm, X_{active} = minimum. (d) I_{th} = 10^{-8} A/μm, X_{active} = minimum.

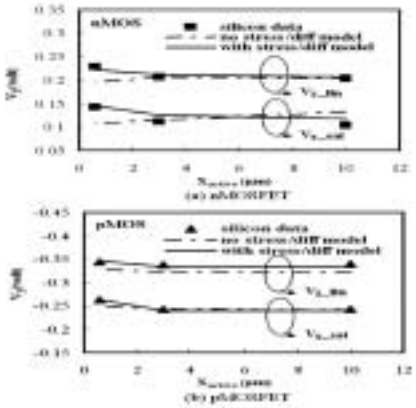


Fig. 10. Experimental and simulated threshold voltage dependence on X_{active} of (a) nMOSFET and (b) pMOSFET. NMOSFET threshold voltage V_T is more dependent on X_{active} than the p-type counterpart. Simulation with stress-dependent diffusion model is able to describe stress-induced V_T shift.

TABLE I

IMPURITY ΔE_C VALUES EXTRACTED IN THE STUDY

Impurity	Boron	Phosphorus	Arsenic
ΔE_C (eV/volumetric shift ratio)	-7	-20	-14

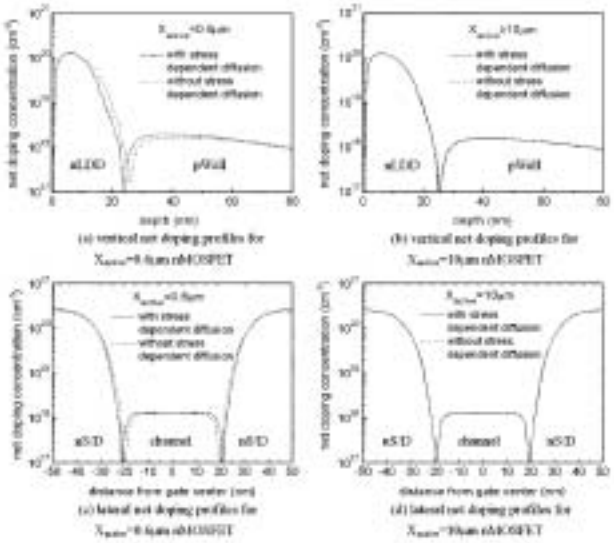
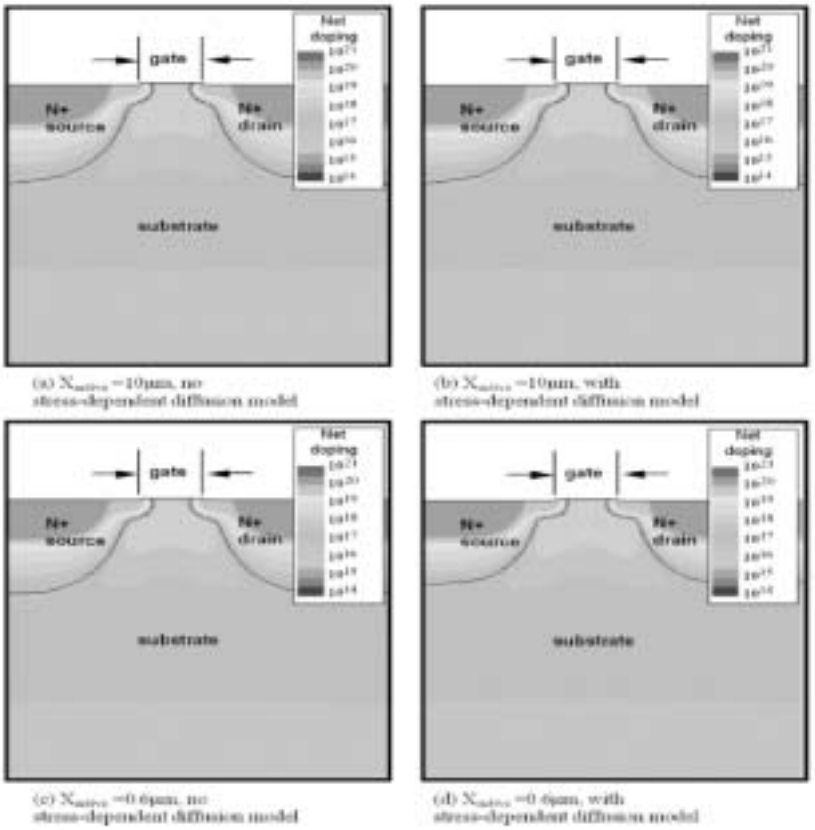


Fig. 12. Dopant profiles of (a) vertical direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET, (b) vertical direction for $X_{\rm active} = 10\ \mu$m nMOSFET, (c) lateral direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET, and (d) lateral direction for $X_{\rm active} = 0.6\ \mu$m nMOSFET. The vertical profiles are taken at gate edge and the lateral profiles are taken at 15-nm-deep cutlines of the device. Solid lines are simulation with stress-dependent diffusion model and dashed lines are without stress-dependent diffusion model. $X_{\rm active} = 0.6\ \mu$m with stress-dependent model device exhibits significant retardation of dopant diffusion.



(a) $X_{\rm active}$ =10μm, no stress-dependent diffusion model

(b) $X_{\rm active}$ =10μm, with stress-dependent diffusion model

(c) $X_{\rm active}$ =0.6μm, no stress-dependent diffusion model

(d) $X_{\rm active}$ =0.6μm, with stress-dependent diffusion model

Fig. 11. Net doping contours for (a) $X_{\rm active} = 10\ \mu$m, no stress-dependent model, (b) $X_{\rm active} = 10\ \mu$m, with stress-dependent model, (c) $X_{\rm active} = 0.6\ \mu$m, no stress-dependent model, and (d) $X_{\rm active} = 0.6\ \mu$m, with stress-dependent model. For $X_{\rm active} = 0.6\ \mu$m, the source/drain junction is significantly shallower in the MOSFET core region when the stress-dependent diffusion model is turned on. The gate length is 65 nm.