行政院國家科學委員會專題研究計畫　成果報告

矽 VLSI 之射頻與光學無線內接線(3/3)

計畫類別：個別型計畫
計畫編號：NSC93-2215-E-009-001-
執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立交通大學電子工程學系暨電子研究所

計畫主持人：荊鳳德

報告類型：完整報告
報告附件：出席國際會議研究心得報告及發表論文
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中　華　民　國 94 年 9 月 22 日

行政院國家科學委員會補助專題研究計畫

■ 成果報告 □期中進度報告

（計畫名稱）
高性能混合訊號式介面積體電路-
子計畫一：矽VLSI之射頻與光學無線內接線(3/3)

計畫類別：□ 個別型計畫 ■ 整合型計畫
計畫編號：NSC 93－2215－E－009－001－
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計畫主持人：荊鳳德
共同主持人：
計畫參與人員：
成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

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行政院國家科學委員會研究計畫成果報告

計畫題目: 高性能混合訊號式介面積體電路-
子計畫一：矽VLSI之射頻與光學無線內接線(3/3)

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主持人：荊鳳德 教授 執行單位：交通大學電子工程系

中文摘要

在小於 100 nm 之高密度深次微米積體電路 IC 的基本限制是 DC 與 AC power 的消耗。其中 DC POWER 可以藉由使用 high K dielectric 材料於 MOSFET 中來降低 3~4 個 order,但是動態 DC POWER 的 Power 消耗很難去降低。AC Power 消耗於後段製程的金屬連接線之中較於 MOSFET 中為嚴重。而後者可以藉由 SOI 的基板來降低之。這個議題已經在 IEDM 2004 被當作 plenary talk 來討論了。因為在先進 IC 之中,譬如微處理器,增加操作頻率以及增加內連接線的密度(ex:以較大的電容)。 最近我們發表 3D 積體技術去達到這些 AC Power consumption issue 藉由使用低溫製程 metal gate/high-K dielectric/ Ge-on-insulator(GOI) CMOS 於以標準 0.18μm 的製程之多層內連接線技術之中。於此我們發表有關 AC power consumption 而且使用 3D 元件結構的一些研究。這種 3D 結構具有較短的內連接線距離,因此可以降低 AC Power 的損耗。另外,雖然高組抗的 Silicon (HRS)基板會有 coupling loss 的發生,我們仍然可以使用之。於減少 AC Power consumption 以及 coupling loss 的最好的選擇就是,將 3D structure 與 HRS 積體化,以此方法可以於 20GHz 以上獲得大於 1~2 個 order 的改善。

一、簡介

The primary limitation of highly-scaled sub-100 nm VLSI IC is the large DC and AC power consumption in high density ICs. The DC power consumption can be reduced by 3-4 orders of magnitude by using high-κ gate dielectric MOSFETs, but the dynamic AC power dissipation ($\propto CV^2f$) is more difficult to reduce due. The AC power consumption from the backend interconnect capacitance is more severe than from the MOSFETs. The latter can be reduced by using SOI substrates. These issues have been discussed in plenary talks in IEDM 2004 [1]-[2]. They are important because the trend is to increasing frequencies (f) and interconnect densities (thus larger capacitance, C) in modern ICs such as microprocessors. Recently we reported three-dimension (3D) integration technology to address this AC power consumption issue [3], by using low-temperature-processed metal-gate/high-κ/Ge- on-Insulator (GOI) CMOS [4] above the multi-layer interconnects on standard 0.18 μm CMOSFETs. Here we report a study of the AC power consumption and coupling using the 3D structure. This 3D structure, with its shorter interconnect distances, can reduce the AC power loss. So too can High-Resistivity Si (HRS) substrates, although using an HRS substrate increases the coupling loss. The best choice to reduce both AC power and coupling losses is to combine 3D integration with HRS, which gives > 1-2

orders of magnitude improvement, up to 20 GHz.

二、實驗步驟

We used two parallel metal lines, represented in Fig. 1, to mimic the parasitic capacitance effects in the complicated interconnects which limit the circuit speed. The AC power ($1-|S_{21}|^2-|S_{11}|^2$) loss and coupling loss (S_{21}) of the local or global interconnects were obtained by measuring the S-parameters of two parallel lines, with co-planar waveguide (CPW) or microstrip transmission line structure. These were made using a foundry Si technology's M1 or M6 layer, with metal thicknesses of 0.7 or 6 μm, respectively. Because of the distributed nature of the interconnects, the use of an Electro-Magnetic (EM) method for the AC power loss is more efficient and accurate than conventional modeling of the intricate equivalent circuit. Here we also used an HRS substrate (1.5×10^4 Ω-cm) to reduce the AC power loss.

三、結果與討論

Fig. 2 shows the power loss of 1-mm long, 2 μm-spaced parallel CPW lines using M6. The 3D integration [3] is equivalent to folding the 2D IC to reduce the interconnect length by ~ ½ or ¼ (folding twice). The power loss increases monotonically with increasing frequency, following a $\sim CV^2f$ relation, and decreases with decreasing interconnect length. The decreased interconnect distance also reduces the signal coupling, as shown in Fig. 3. Fig. 4 shows the power loss of two parallel lines having a microstrip line structure. This has a vertical EM field rather than it being horizontal as for a CPW line (Fig. 3). Because the line-spacing is small compared with the substrate thickness (300μm), the horizontal power loss is more important than the vertical one. Hence we focused only on the CPW case. Fig. 5 depicts the power loss of local parallel lines, using M1, where the loss is more severe than for the loss of global lines, shown in Fig. 3 using M6. This is due to the smaller separation from the low resistivity Si substrate, where more AC power is lost through the substrate loss network. This is confirmed by the reduced power loss when using an HRS substrate. Fig. 6 shows the coupling of parallel lines using M1. Using the HRS substrate increases the unwanted coupling. This can be understood from the equivalent circuit model (insert in Fig. 5), where the reduced loss in the substrate RC network increases the forward transmission. Figs. 7 and 8 show the coupling and power loss of local interconnect lines using M1, with different gap widths and line lengths. The HRS gives the worst coupling loss and, furthermore, decreasing the line spacing makes it worse. The most effective way to reduce the coupling loss is to shorten the interconnecting lines e.g. by 3D integration. On the other hand the best way to reduce the power loss is to use an HRS substrate, although the shorter lines given by 3D integration help. Hence the best solution is to combine 3D integration with HRS technology, to give 1-2 orders of magnitude lower power and coupling loss (see Figs. 7-8).

四、結論

More than 10X reduction of both AC power and coupling loss in ICs can be realized by 3D technology.

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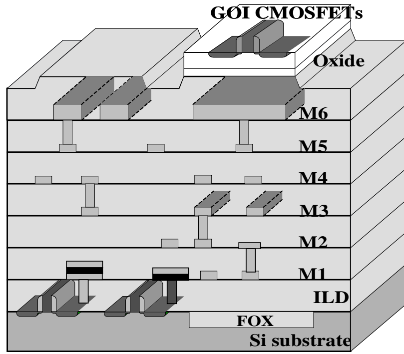

Fig. 1. Schematic diagram of VLSI backend interconnects with parallel lines. 3D integration with GOI MOSFETs can reduce the power and coupling loss.

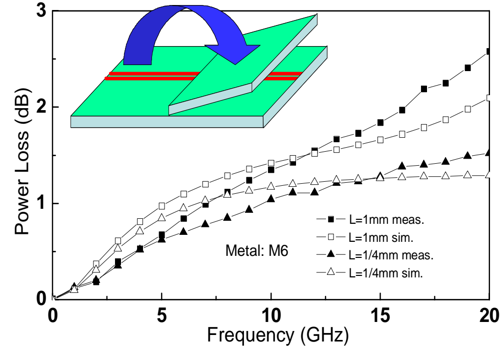

Fig. 2. Power loss of 1-mm long 2μm-spaced parallel lines. 3D integration can reduce the line length by ½ (1 GOI) or ¼ (2 GOI layers) and reduce the power loss.

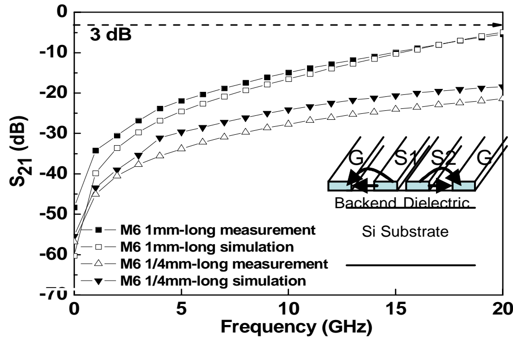

Fig. 3. Coupling loss of 1-mm long 2μm-spaced parallel lines. The loss decreasing with line length.

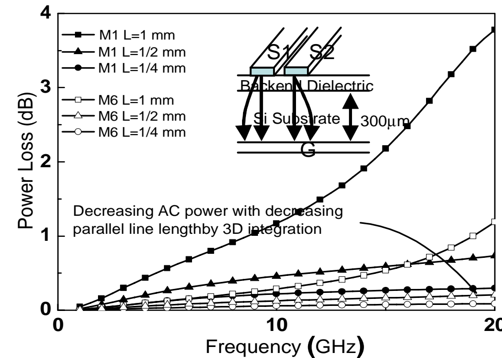

Fig. 4. Power loss of 1-mm long 2μm-spaced parallel lines. Metal: M6. Vertical field in microstrip structure is different from the horizontal field in the CPW case.

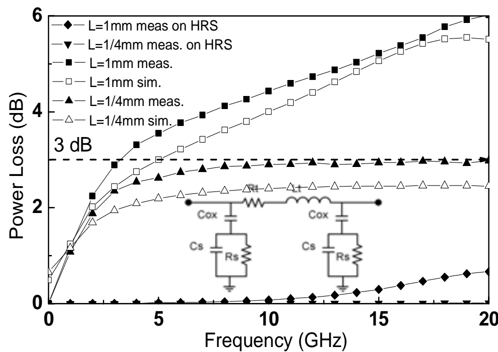

Fig. 5. Power loss of 1-mm long 2μm-spaced parallel lines. Reducing the line length or using an HRS substrate reduces the power loss. Metal: M1

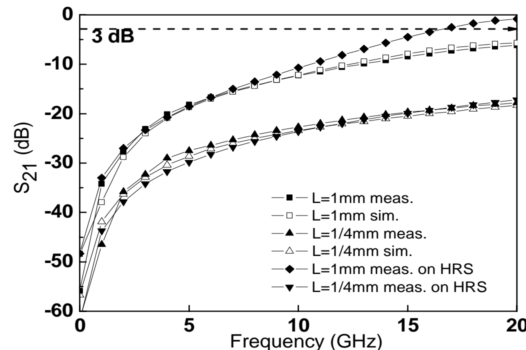

Fig. 6. Coupling loss of 1-mm long 2μm-spaced parallel lines. HRS substrate increases the unwanted coupling but reduces the power loss. Metal: M1

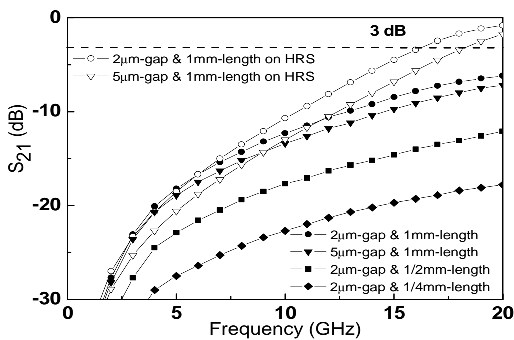

Fig. 7. Coupling loss of two parallel interconnect lines, with different lengths, widths substrates.

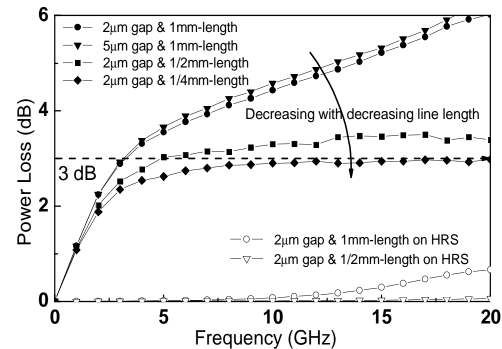

Fig. 8. Power loss of two parallel interconnect lines, with different lengths, widths and substrates.