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Electrical performance and thermal stability of MIC poly-Si TFTs improved using drive-in nickel induced crystallization

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ABSTRACT

Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) has been used to fabricate low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs). The current crystallization technology, however, often leads to trap Ni and $NiSi_2$ precipitates, which degrade the device performance. In this study, a new manufacturing method for poly-Si TFTs using drive-in Ni induced crystallization (DIC) was proposed. In DIC, F^+ implantation was used to drive Ni in the α-Si layer. It was found that the electrical performance (especially leakage current) and thermal stability of DIC-TFTs were improved due to the reduction of Ni concentration and passivation of trap states near the SiO_2/poly-Si interface.
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1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for their use in active-matrix liquid crystal displays (AMLCDs) because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [1]. Intensive studies have been carried out to lower the crystallization temperature of amorphous silicon (α-Si) films. The solid phase crystallization (SPC) method is a well-established poly-Si formation technique [2]. The major drawback of SPC is that the α-Si films need to be annealed for about 24 h at 600 °C, which is higher than the strain temperature of a normal glass substrate. In contrast, metal induced crystallization (MIC) and metal induced lateral crystallization (MILC) methods require a lower thermal budget and present a great on-state of electrical performance than SPC [3–5]. In MILC, Ni islands are selectively deposited on top of α-Si films and allowed to crystallize at a temperature below 600 °C. Unfortunately, the uniformity is poor, annealing time is long, and extra mask is needed to define the Ni window. In contrast, MIC method is much simple for commercial manufacturing. No extra mask is needed, the annealing time is short (0.5–5 h), and the uniformity is good. However, Ni and $NiSi_2$ precipitates were trapped in the poly-Si grain boundaries, which increase the leakage current and shift the threshold voltage [5–8]. Therefore, Ni concentration in MIC poly-Si films should be reduced. Several Ni-gettering methods have been employed to reduce the amount of undesired metal impurity [9–11]. Nevertheless, the crystallinity of poly-Si films was decline after the gettering process, thus decreasing on current of character of poly-Si TFTs [10]. Recently, fluorine ion (F^+) implantation was employed to improve the electrical performance of TFTs [12,13]. Unfortunately, the minimum off currents were nearly unchanged. This might because the Ni concentration was unchanged.

In this study, F^+ implantation was used to drive Ni in the α-Si layer to induce crystallization (DIC) process to reduce the Ni concentration and minimize the trap-state density of MIC-TFTs. The devices characteristics and thermal stability of fluorinated MIC-TFT were investigated.

2. Experimental

N-type self-alignment poly-Si TFTs were investigated in this study. The preparation of DIC poly-Si began with four-inch Si wafer. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. A 5-nm-thick Ni film was then deposited. Samples were subjected to F^+ implantation to drive Ni in the α-Si layer, as shown in Fig. 1(a). The projection range was set at the 15 nm of depth near surface of the α-Si layer. In this study, two dosages of F+ were used, 2×10^{13} and 2×10^{14} cm^{-2}. They were denoted as DIC-13 and DIC-14, respectively. The ion-accelerating energy was 10 keV. To reduce the Ni contamination, the remained Ni film was then removed by a mixed solution of H_2SO_4 and H_2O_2 (Fig. 1(b)), and subsequently annealed at 500 °C for 1 h in N_2.

For the purpose of comparison, conventional MIC poly-Si was prepared. The basic processes of MIC poly-Si were almost the same as those of DIC poly-Si. The major difference was that the surfaces of MIC poly-Si did not undergo any F^+ implantation. A 5-nm-thick Ni film was deposited on α-Si/buffer oxide/Si wafer. After annealed at 500 °C, the remained Ni was removed.

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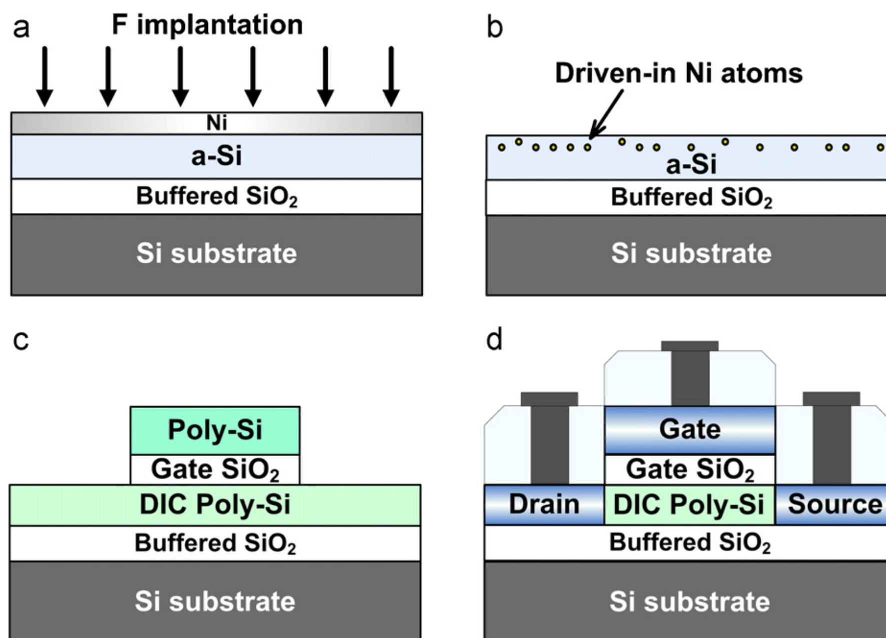

Fig. 1. Schematic illustration of DIC-TFT fabrication process: (a) F^+ implantation to drive Ni in the α-Si layer, (b) removing of remained Ni film, (c) fabrication of TFT devices by standard IC processes, and (d) formation of source/drain and gate.

TFT devices were fabricated by standard IC processes. As shown in Fig. 1(c), the islands of poly-Si regions on the wafers were defined by reactive ion etching (RIE). Next, a 100-nm-thick tetraethylorthosilicate/O_2 oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned 35 keV phosphorous ions were implanted at a dose of 5×10^{15} cm^{-2} to form the source/drain and gate. Dopant activation was performed at 600 °C in N_2 ambient for 12 h. After dopant activation, a 500-nm-thick SiO_2 layer was deposited by PECVD as passivation layer. Contact holes were formed and a 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode as shown in Fig. 1(d). Sintering process was performed at 400 °C for 30 min in N_2 ambient. It is worthy to note that this DIC process does not need any additional annealing step and is compatible with MIC processes.

3. Results and discussion

The grains of MIC were crystallized from top to down and formed needle-like MIC grains [14]. The plane-view images of transmission electronic microscopy (TEM) were shown in Fig. 2. The grain diameters of MIC, DIC-13 and DIC-14 were 8–10 nm, 10–12 nm and 10–12 nm, respectively. The variation of grain size was attributed to the different Ni concentration during MIC annealing process. Fig. 3 shows the secondary-ion mass spectrometry (SIMS) depth profiles of Ni and F in the structure of poly-Si films. As a result, Ni concentration in DIC was much lower than that in MIC. In other words, the amount of nucleation site of $NiSi_2$ in MIC is higher than that in DIC due to large content of Ni. Therefore, the grain size of MIC was less than that of DIC. Raman spectra around the wave-number of 510 cm^{-1} was shown in Fig. 4. The intensity of MIC was lower than that of DIC. The full width at half maximum of DIC was smaller than that of MIC. In other words, the crystallinity of DIC was better than that of MIC.

Fig. 5 displays the I_D–V_G transfer characteristics of TFTs. The measured and extracted key device parameters are summarized in Table 1. The device parameters were extracted at $W/L = 10/10$ μm, and 10 TFTs were measured in each case to investigate the device-to-device variation. The average values with standard deviations in parentheses were shown in Table 1. The threshold voltage (V_{th}) is defined at a normalized drain current of $I_{DS} = (W/L) \times 100$ nA at $V_{DS} = 5$ V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at $V_{DS} = 0.1$ V. It was found that the electrical characteristics (especially leakage current and on/off current ratio) of TFTs were improved by DIC processes. Compared with MIC-TFTs, DIC-TFTs shows a 2.98-fold decrease in the minimum leakage current and a 2.89-fold increase in the on/off current ratio. It was great

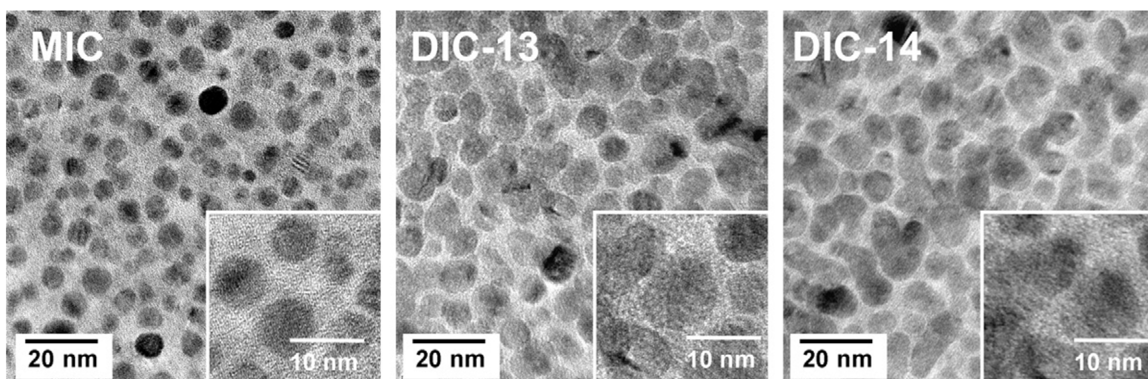

Fig. 2. TEM plane-view images of MIC and DIC poly-Si films.

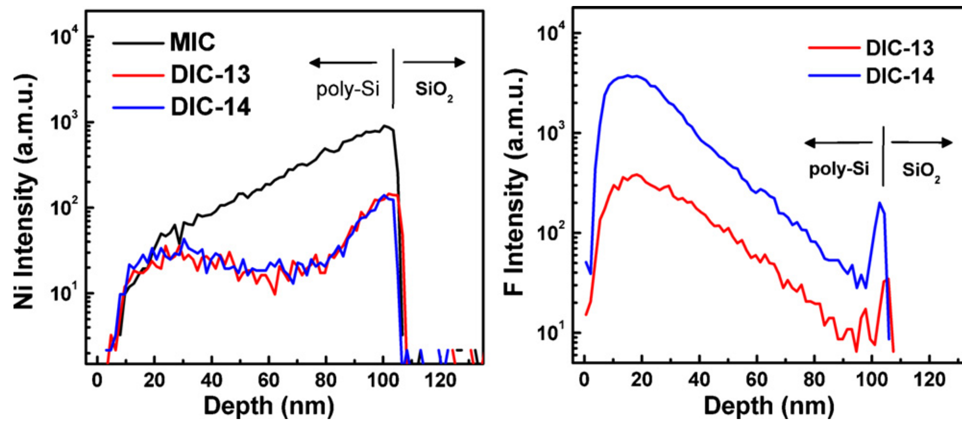

Fig. 3. SIMS depth profiles of (a) nickel and (b) fluorine in the structure of MIC and DIC poly-Si films.

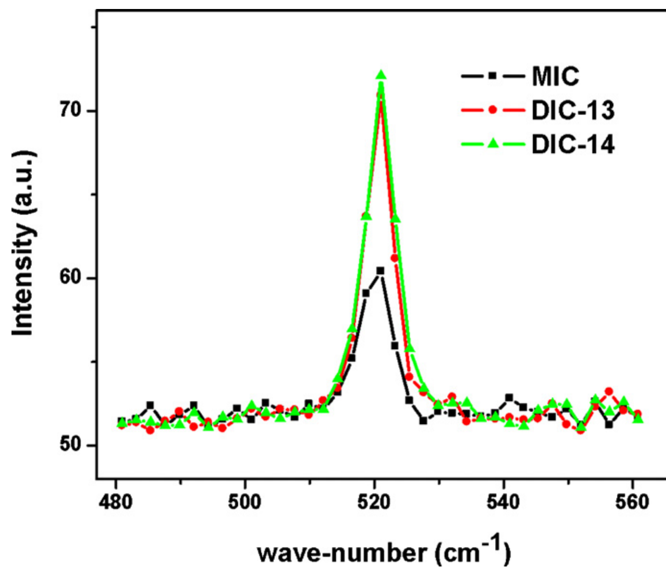

Fig. 4. Raman spectra of MIC and DIC poly-Si films around the wave-number of 510 cm^{-1}.

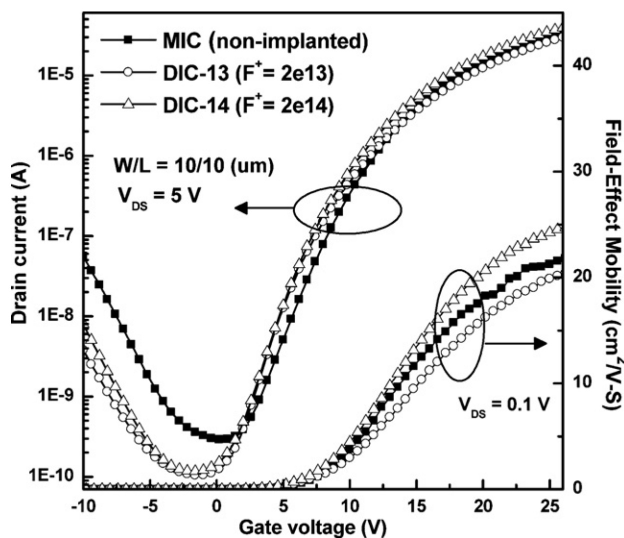

Fig. 5. Typical I_{DS}–V_{GS} transfer characteristics and field-effect mobility of DIC-TFTs and MIC-TFT (W/L = 10/10 μm).

improved in off-state which is the most importance of MIC-TFT.

The leakage current improvement was attributed to the reduction of Ni concentration in the poly-Si films. This is because, in the poly-Si film, Ni residues serve as deep level traps, which promote thermionic emission-dominated leakage current in the low-gate and drain voltage region [15–17]. Ni content in DIC was much lower than that in MIC as shown in Fig. 3(a). The DIC process did reduce Ni content in poly-Si films. With the reduction of the Ni concentration in DIC, the minimum leakage current was reduced and therefore the on/off current ratio was increased.

Besides, as shown in Fig. 3(b), F content in DIC-14 was much higher than that in DIC-13. High F content is present at the DIC/oxide interface, meaning F atoms have diffused to the interface to terminate defects. The effective interface trap states densities (N_{it}) near the SiO_2/poly-Si interface can be calculated as follows:

$$N_{it} = \left[\left(\frac{S.S.}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right)$$

where C_{ox} is the capacitance of the gate insulator [18]. As shown in Table 1, the value of N_{it} was decreased with increase in dosage of F^+. Therefore, DIC-TFT presents good S.S. and V_{th} in the performance.

Since F atoms can passivate dangling bonds and strain bonds [19], the on currents of DIC-TFTs were expected to be higher than those of MIC-TFTs. As shown in Fig. 5, the on current of DIC-14 was higher than that of MIC-TFTs. However, the on current of DIC-13 was lower than that of MIC-TFTs. The degradation of on current of DIC-13 might due to the damage of the channel, which was caused by ion implantation [20]. The roughness of the poly-Si surfaces (after the remained Ni was removed) was measured by atomic force microscopy (AFM). The roughness can reflect the degree of damage since the grain size of MIC, DIC-13 and DIC-14 were almost. At the same Si layer, AFM can demonstrate degree of collision at surface by

Table 1
Average device characteristics of DIC-TFTs and MIC-TFTs with standard deviations in parentheses.

Device perimeters W/L = 10 μm/10 μm	MIC	DIC-13	DIC-14
Field-effect mobility μ_{FE} ($cm^2 V^{-1} s$)	23.0 (1.38)	22.2 (1.12)	25.6 (0.82)
Threshold voltage V_{th} (V)	8.09 (1.23)	7.46 (0.33)	7.07 (0.24)
Subthreshold slope S.S. ($V dec^{-1}$)	2.00 (0.09)	1.83 (0.05)	1.75 (0.11)
I_{min} ($pA \mu m^{-1}$)	3.31 (0.54)	1.11 (0.05)	1.23 (0.07)
Max on/off ratio ($\times 10^5$)	1.57 (0.47)	3.72 (0.41)	4.54 (0.38)
Interface trap density N_{it} ($10^{12} cm^{-2}$)	7.03 (0.32)	6.42 (0.19)	6.10 (0.39)

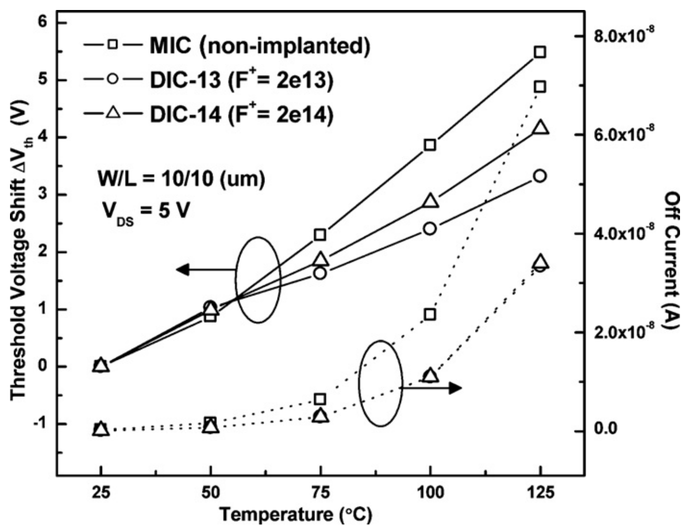

Fig. 6. The degradations of threshold voltage and off current versus temperature at V_{DS} = 5 V.

implantation. Therefore, it can verify increasing defect indirectly. As the results, the root mean square (rms) roughnesses of MIC, DIC-13 and DIC-14 films were 0.618, 0.731 and 0.846 nm, respectively. The damage (rms roughness) did increase with the dosage of F^+. In other words, in this DIC study, there were three major kinds of defects related to the MIC-TFT performance: (1) Ni concentration (Ni-related defects), (2) grain boundaries and (3) channel damages/defects. In DIC process, F^+ implantation was used to drive Ni in the α-Si layer. Compared with MIC process, DIC process can reduce the Ni concentration, thus reducing the (1) Ni concentration. Besides, in DIC process, F atoms can passivate dangling bonds and strain bonds, thus reducing the effects of (2) grain boundaries defects and (3) channel damages/defects. Since the F content in DIC-14 was much higher than that in DIC-13, the improvement of DIC-14 were expected to be much better than that of DIC-13. On the other hand, the damage (rms roughness) of the channel surface increased with the dosage of F^+. As a result, DIC-13 has the lowest on current since its F passivation effect was not good enough to compensate the degradation from surface damage. As for the DIC-14, the effect of F passivation was higher than that of channel damages. As a result, DIC-14 has the highest on current.

The other important issue of poly-Si TFTs is the thermal stability, which was examined at elevated temperatures. As shown in Fig. 6, the threshold voltage and the off current of TFTs were degraded with increase in annealing temperature from 25 to 125 °C. This is because when temperature increased, nickel related donor-like defects were easy to release electrons, thus increasing the leakage current and the negative shift of V_{th} [21]. Compared with those of MIC-TFTs, the thermal stability of DIC-TFTs was improved by DIC processes, which is due to the reduction of Ni concentration in TFTs as shown in Fig. 3(a). The other factor that might affect the thermal stabilities is the bonding energy. The bonding energy of the Si–F bond is greater than that of the Si–Si and Si–H bonds [22]. As a result, the increase of the leakage current and the negative shift of V_{th} of DIC-TFTs was less than that of MIC-TFTs.

4. Conclusions

MIC method has been used to reduce the crystallization time and temperature of α-Si. The annealing time is short and the uniformity is good. However, Ni-related defects and grain boundaries would degrade the TFT performance. In this study, an investigation of poly-Si TFTs using DIC process had led to the development of a simple process for LTPS TFTs manufacturing.

In DIC, F^+ implantation was used to drive Ni in the α-Si layer. Compared with MIC process, DIC process can effectively reduce the Ni concentration, thus reducing the Ni-related defects. F atoms can passivate dangling bonds and strain bonds, thus reducing the effects of grain boundaries and channel damages/defects. However, the damage of the channel surface increased with the dosage of F^+. As a result, DIC-14 TFTs exhibit higher field-effect mobility, lower subthreshold slope, lower threshold voltage, higher on/off current ratio, and lower interface trap-state density (N_{it}) compared with conventional MIC-TFTs. It was also found that DIC process can greatly alleviate the degradations of threshold voltage and off current at elevated temperatures. This is attributed to the reduction of Ni concentration in TFTs, and the weaker Si–H and Si–Si bonds were replaced by stronger Si–F bonds.

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